A5G19H605W19N

Airfast RF Power GaN Transistor

Rev. 1 — 20 March 2024 **Product data sheet**

1 General description

This 85 W asymmetrical Doherty RF power GaN transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1930 to 1995 MHz.

This part is characterized and performance is guaranteed for applications operating in the 1930 to 1995 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

2 Features and benefits

- High terminal impedances for optimal broadband performance
- Advanced high performance in-package Doherty
- Improved linearized error vector magnitude with next generation signal
- Able to withstand extremely high output VSWR and broadband operating conditions
- Plastic package

3 Typical performance

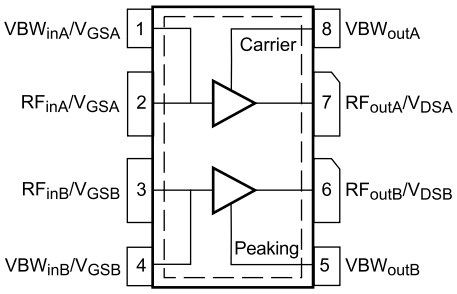
Table 1. 1900 MHz — Typical Doherty single-carrier W-CDMA production test fixture performance

V_{DD} = 48 Vdc, I_{DQA} = 300 mA, V_{GSB} = –5.0 Vdc, P_{out} = 85 W Avg., input signal PAR = 9.9 dB @ 0.01% probability on CCDF[1]

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
1930 MHz	16.3	54.3	8.9	–29.2
1960 MHz	16.7	55.1	8.6	–30.2
1995 MHz	17.0	55.7	8.2	–31.2

[1] All data measured with device soldered to NXP production test fixture.

4 Pinning information



(Top view)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin configuration

5 Ordering information

Table 2. Ordering information

Device	Tape and reel information	Package
A5G19H605W19NR3	R3 suffix = 250 units, 44 mm tape width, 13-inch reel	OM-780-4S4S

6 Product marking

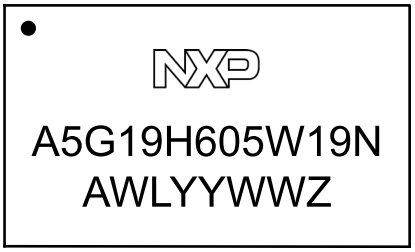


Figure 2. Product marking

Table 3. Product marking trace code

Identifier	Description
A	Assembly location
WL	Wafer lot indicator
YYWW	Date code
Z	Assembly lot

7 Limiting values

Table 4. Limiting values

Rating	Symbol	Value	Unit
Drain-source voltage	V_{DSS}	125	Vdc
Gate-source voltage	V_{GS}	–16, 0	Vdc
Operating voltage	V_{DD}	55	Vdc
Maximum forward gate current, $I_{G(A+B)}$, @ T_C = 25°C	I_{GMAX}	95	mA
Storage temperature range	T_{stg}	–65 to +150	°C
Case operating temperature range	T_C	–55 to +150	°C
Maximum channel temperature	T_{CH}	225	°C

8 Recommended operating conditions

Table 5. Recommended operating conditions

Characteristic	Symbol	Value	Unit
Operating voltage	V_{DD}	48	Vdc

9 Thermal characteristics

Table 6. Thermal characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance by infrared measurement, active die surface-to-case (Case temperature 124°C, $P_{D\text{-}Global}$ = 107 W)	$R_{\theta SC}$ (IR)	0.61[1]	°C/W
Thermal resistance by finite element analysis, channel-to-case Carrier (Case temperature 124°C, P_D = 75.3 W) Peaking (Case temperature 114°C, P_D = 19.0 W)	$R_{\theta CHC}$ (FEA)	 1.3[1][2] 0.9[1][2]	°C/W

[1] Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to http://www.nxp.com/RF and search for AN1955.

[2] $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where T is the channel temperature in degrees Celsius, A = –11.6 and B = 9129.

10 ESD protection characteristics

Table 7. ESD protection characteristics

Test methodology	Class
Human Body Model (per JS-001-2023)	1C
Charge Device Model (per JS-002-2022)	C3

11 Moisture sensitivity level

Table 8. Moisture sensitivity level

Test methodology	Rating	Package peak temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	245	°C

12 Electrical characteristics

12.1 DC characteristics — off characteristics

Table 9. DC characteristics — off characteristics

(T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off characteristics[1]					
Off-state drain leakage (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc) Carrier (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc) Peaking	$I_{D(BR)}$	 — —	 — —	 13.2 26.4	mAdc

[1] Each side of device measured separately.

12.2 DC characteristics — on characteristics

Table 10. DC characteristics — on characteristics

(T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
On characteristics — Side A, Carrier					
Gate threshold voltage (V_{DS} = 10 Vdc, I_D = 30 mAdc)	$V_{GS(th)}$	–4.6	–2.6	–1.9	Vdc
Gate quiescent voltage (V_{DD} = 48 Vdc, I_{DA} = 300 mAdc, measured in functional test)	$V_{GSA(Q)}$	–3.1	–2.6	–2.1	Vdc
On characteristics — Side B, Peaking					
Gate threshold voltage (V_{DS} = 10 Vdc, I_D = 60 mAdc)	$V_{GS(th)}$	–4.6	–2.5	–1.9	Vdc

12.3 Functional tests

Table 11. Functional tests

(In NXP Doherty production test fixture, T_A = 25°C unless otherwise noted, 50 ohm system)[1] V_{DD} = 48 Vdc, I_{DQA} = 300 mA, V_{GSB} = (V_t – 2.25) Vdc, P_{out} = 85 W Avg., f = 1960 MHz, single-carrier W-CDMA, IQ magnitude clipping, input signal PAR = 9.9 dB @ 0.01% probability on CCDF. ACPR measured in 3.84 MHz channel bandwidth @ ±5 MHz offset.

Characteristic	Symbol	Min	Typ	Max	Unit
Power gain	G_{ps}	13.8	15.1	18.5	dB
Drain efficiency	η_D	45.0	53.8	—	%
Saturated power (Pulsed CW, 5% duty cycle)	P_{sat}	55.8	57.2	—	dBm
Adjacent channel power ratio	ACPR	—	–31.9	–25.7	dBc

[1] Internally matched part.

12.4 Wideband ruggedness

Table 12. Wideband ruggedness

(In NXP Doherty production test fixture, T_A = 25°C unless otherwise noted, 50 ohm system) I_{DQA} = 300 mA, V_{GSB} = –5.0 Vdc, f = 1960 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR

Characteristic	Test results
ISBW of 400 MHz at 55 Vdc, 105 W Avg. modulated output power (3 dB input overdrive from 85 W Avg. modulated output power)	No device degradation

12.5 Typical performance

Table 13. Typical performance

(In NXP Doherty production test fixture, T_A = 25°C unless otherwise noted, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 300 mA, V_{GSB} = –5.0 Vdc, 1930–1995 MHz bandwidth

Characteristic	Symbol	Min	Typ	Max	Unit
Pulsed CW, 10% duty cycle					
Saturated power[1]	P_{sat}	—	624	—	W
AM/PM[1] (Phase deviation from rated power to saturated power. Maximum number measured across the 1930–1995 MHz bandwidth.)	Φ	—	–14	—	°
Gain variation @ Avg. power over temperature (–40°C to +85°C)	ΔG	—	0.014	—	dB/°C
Output power variation @ saturated power over temperature (–40°C to +85°C)	ΔP_{sat}	—	0.003	—	dB/°C
Single-carrier W-CDMA, unclipped					
Gain flatness in 65 MHz bandwidth @ P_{out} = 85 W Avg.[1]	G_F	—	0.7	—	dB
2-tone CW					
VBW resonance point[1] (IMD third order intermodulation inflection point)	VBW_{res}	—	210	—	MHz

[1] All data measured with device soldered to NXP production test fixture.

Correct biasing sequence for GaN depletion mode transistors in a Doherty configuration

Bias ON the device

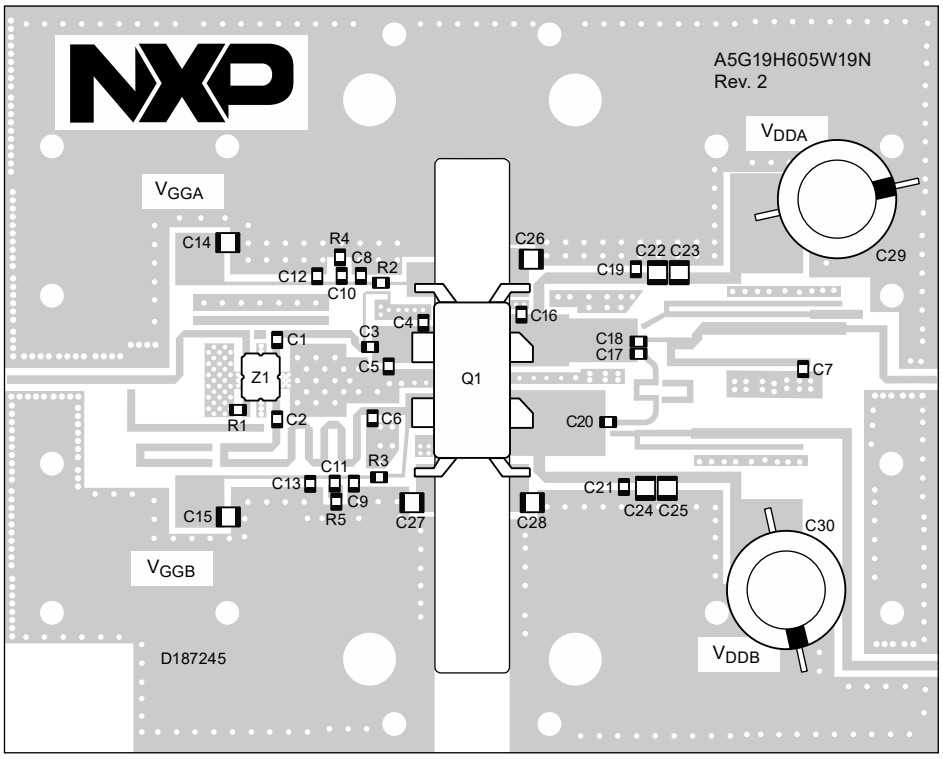
1. Set gate voltage V_{GSA} and V_{GSB} to –5 V.
2. Set drain voltage V_{DSA} and V_{DSB} to nominal supply voltage (+48 V).
3. Increase V_{GSA} (carrier side) until I_{DQA} current is attained.
4. Increase V_{GSB} (peaking side) to target bias voltage.
5. Apply RF input power to desired level.

Bias OFF the device

1. Disable RF input power.
2. Adjust gate voltage V_{GSA} and V_{GSB} to –5 V.
3. Adjust drain voltage V_{DSA} and V_{DSB} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Disable V_{GSA} and V_{GSB}.

13 Component layout and parts list

13.1 Component layout



Note: All data measured with device soldered to NXP production test fixture.

aaa-054102

Figure 3. A5G19H605W19N production test fixture component layout

13.2 Component designations and values

Table 14. A5G19H605W19N production test fixture component designations and values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C8, C9, C19, C20, C21	10 pF chip capacitor	GQM2195C2E100GB12D	Murata
C4	3.3 pF chip capacitor	GQM2195C2E30GB12D	Murata
C5	1.5 pF chip capacitor	GQM2195C2E15GB12D	Murata
C6	1.2 pF chip capacitor	GQM2195C2E12GB12D	Murata
C7	3.3 pF chip capacitor	GQM2195C2E33GB12D	Murata
C10, C11	10 nF chip capacitor	C0805C103K5RACTU	Kemet
C12, C13	1 µF chip capacitor	GJ821BR1H105KA12L	Murata
C14, C15, C22, C23, C24, C25, C26, C27, C28	4.7 µF chip capacitor	C4532X7R1H475K	TDK
C16	0.8 pF chip capacitor	GQM2195C2E5GB12D	Murata
C17, C18	1 pF chip capacitor	GQM2195C2E1R0CB12D	Murata
C29, C30	220 µF, 100 V electrolytic capacitor	UVY2A221MHD	Nichicon
R1	50 Ω, 10 W chip resistor	C10A50Z4	Anaren
R2, R3	2.2 Ω, 1/8 W chip resistor	CRCW08052R20JNEA	Vishay
R4, R5	1.5 Ω, 1/8 W chip resistor	CRCW08051R50JNEA	Vishay
Q1	RF power GaN transistor	A5G26H605W19N	NXP
Z1	1700–2000 MHz, 90º, 3 dB hybrid coupler	X3C19P1-03S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D187245	MTL

14 Package information

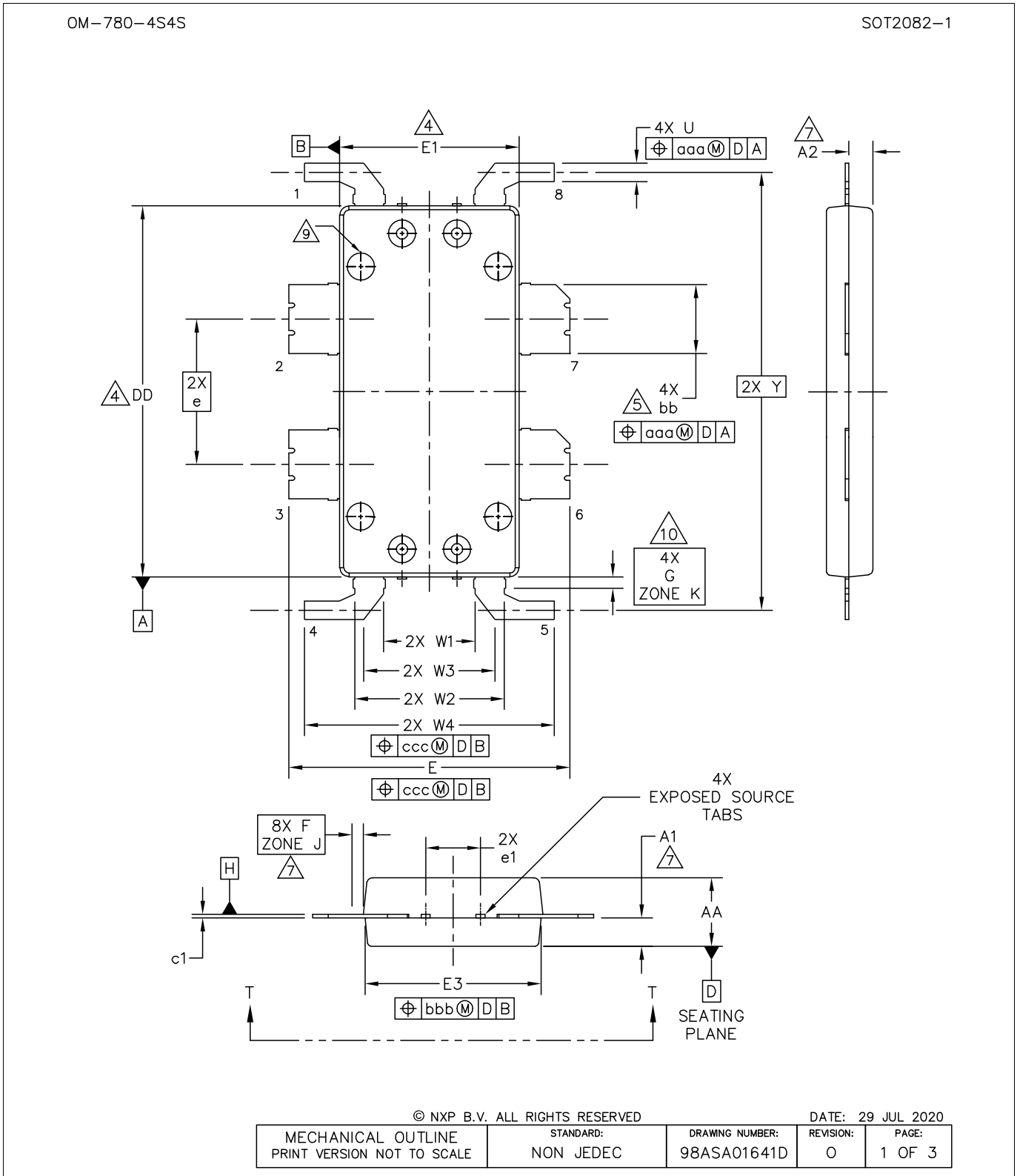


Figure 4. Package outline (OM-780-4S4S)

OM−780−4S4S SOT2082−1

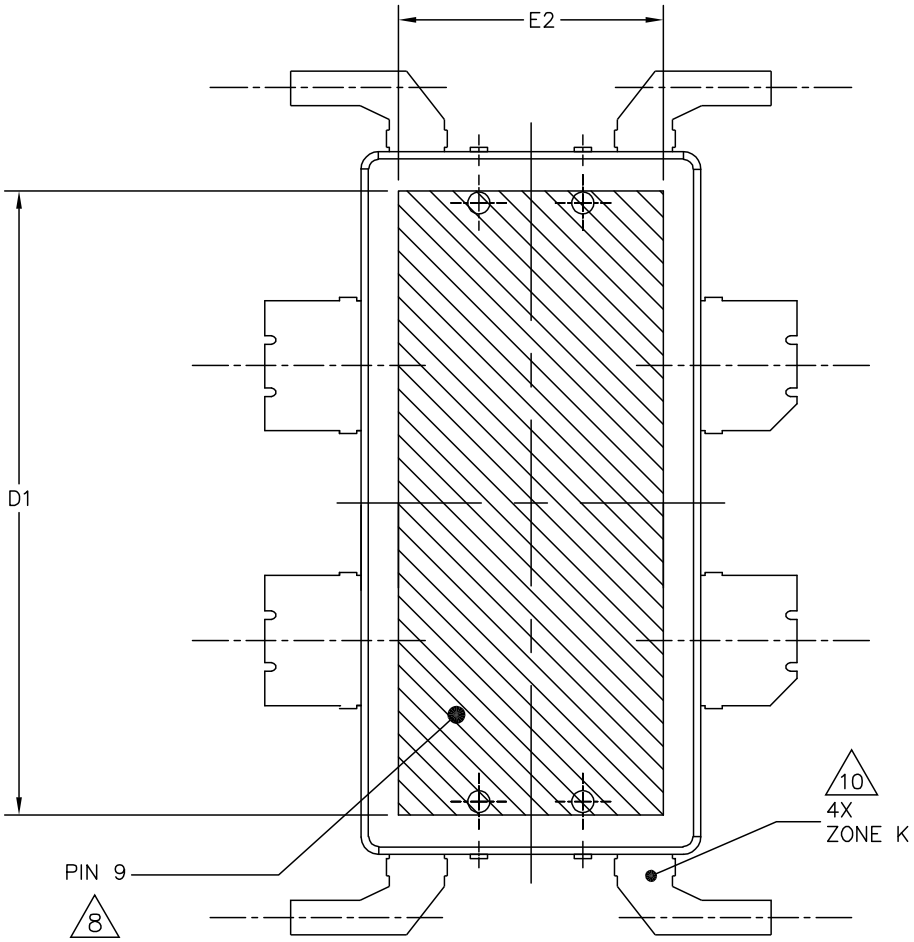


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Figure 5. Package outline (OM-780-4S4S) — bottom view

OM−780−4S4S SOT2082−1

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSIONS A1 AND A2 APPLIES WITHIN ZONE J ONLY. A1 APPLIES TO PINS 2, 3, 6 AND 7. A2 APPLIES TO PINS 1, 4, 5 AND 8.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

9. DIMPLED HOLE REPRESENTS INPUT SIDE.

10. ZONE K REPRESENTS NON−SOLDERABLE REGION WHERE MOLD FLASH AND RESIN BLEED ARE PERMITTED ON BOTH SIDES OF THE LEADS.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.148	.152	3.76	3.86	W2	.321	.331	8.15	8.41
A1	.059	.065	1.50	1.65	W3	.281	.291	7.14	7.39
A2	.056	.068	1.42	1.73	W4	.538	.554	13.67	14.07
DD	.808	.812	20.52	20.62	U	.037	.043	0.94	1.09
D1	.720	----	18.29	----	Y	.956 BSC		24.28 BSC	
E	.610	.618	15.49	15.70	bb	.147	.153	3.73	3.89
E1	.390	.394	9.91	10.01	c1	.007	.011	0.18	0.28
E2	.306	----	7.77	----	e	.317 BSC		8.05 BSC	
E3	.383	.387	9.73	9.83	e1	.116	.124	2.95	3.15
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
G	.030 BSC		0.76 BSC		bbb	.006		0.15	
W1	.195	.205	4.95	5.21	ccc	.010		0.25	

DATE: 29 JUL 2020

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Figure 6. Package outline (OM-780-4S4S) — notes, dimensions

15 Product documentation, software and tools

Refer to the following resources to aid your design process.

Application notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p file

Development tools

- Printed circuit boards

16 Revision history

The following table summarizes revisions to this document.

Table 15. Revision history

Document ID	Release date	Description
A5G19H605W19N Rev. 1	20 March 2024	• Initial release of product data sheet

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet'' is explained in section "Definitions".
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Date of release: 20 March 2024
Document identifier: A5G19H605W19N