

# RF Power LDMOS Transistor

## N-Channel Enhancement-Mode Lateral MOSFET

This 71 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 1805 to 1880 MHz.

### 1800 MHz

- Typical Doherty Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Vdc,  $I_{DQA} = 800$  mA,  $V_{GSB} = 0.8$  Vdc,  $P_{out} = 71$  W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

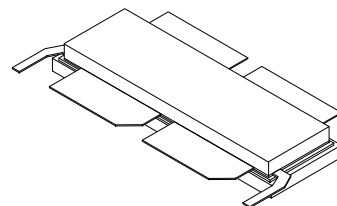
Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)
1805 MHz	17.4	51.2	7.9	-34.5
1840 MHz	17.5	50.1	8.3	-36.9
1880 MHz	17.6	49.3	8.0	-36.8

### Features

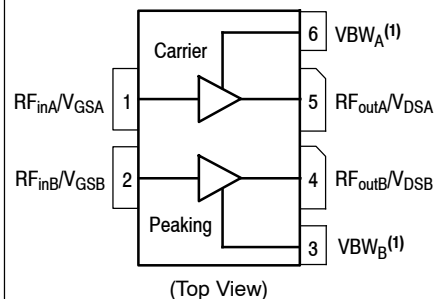
- Advanced High Performance In-Package Doherty
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems

## A2T18H410-24SR6

**1805-1880 MHz, 71 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR**



NI-1230S-4L2L



**Figure 1. Pin Connections**

- Device cannot operate with the  $V_{DD}$  current supplied through pin 3 and pin 6.

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature Range	$T_C$	-40 to +150	°C
Operating Junction Temperature Range (1,2)	$T_J$	-40 to +225	°C
CW Operation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	CW	282 1.5	W W/°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature $72^\circ\text{C}$ , 71 W Avg., W-CDMA, 28 Vdc, $I_{DQA} = 800\text{ mA}$ , $V_{GSB} = 0.8\text{ Vdc}$ , 1840 MHz	$R_{\theta JC}$	0.24	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics (4)**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 32\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics - Side A (Carrier)**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 160\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.4	1.5	2.3	Vdc
Gate Quiescent Voltage ( $V_{DD} = 28\text{ Vdc}$ , $I_{DA} = 800\text{ mAdc}$ , Measured in Functional Test)	$V_{GS(Q)}$	2.2	2.6	3.0	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 1.6\text{ Adc}$ )	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

**On Characteristics - Side B (Peaking)**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 270\ \mu\text{Adc}$ )	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 2.7\text{ Adc}$ )	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf/calculators>.
3. Refer to [AN1955](#), *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf> and search for AN1955.
4. Each side of device measured separately.

(continued)

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Functional Tests</b> <sup>(1,2)</sup> (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQA} = 800\text{ mA}$ , $V_{GSB} = 0.8\text{ Vdc}$ , $P_{out} = 71\text{ W Avg.}$ , $f = 1805\text{ MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	$G_{ps}$	16.5	17.4	19.5	dB
Drain Efficiency	$\eta_D$	47.0	51.2	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.4	7.9	—	dB
Adjacent Channel Power Ratio	ACPR	—	-34.5	-28.0	dBc

**Load Mismatch** <sup>(2)</sup> (In Freescale Doherty Test Fixture, 50 ohm system)  $I_{DQA} = 800\text{ mA}$ ,  $V_{GSB} = 0.8\text{ Vdc}$ ,  $f = 1840\text{ MHz}$ 

VSWR 10:1 at 32 Vdc, 440 W CW <sup>(3)</sup> Output Power (3 dB Input Overdrive from 376 W CW <sup>(3)</sup> Rated Power)	No Device Degradation
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**Typical Performance** <sup>(2)</sup> (In Freescale Doherty Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQA} = 800\text{ mA}$ ,  $V_{GSB} = 0.8\text{ Vdc}$ , 1805–1880 MHz Bandwidth

$P_{out}$ @ 1 dB Compression Point, CW	P1dB	—	355 <sup>(3)</sup>	—	W
$P_{out}$ @ 3 dB Compression Point <sup>(4)</sup>	P3dB	—	457	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz frequency range)	$\Phi$	—	-12.4	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	$VBW_{res}$	—	90	—	MHz
Gain Flatness in 75 MHz Bandwidth @ $P_{out} = 71\text{ W Avg.}$	$G_F$	—	0.1	—	dB
Gain Variation over Temperature (-30°C to +85°C)	$\Delta G$	—	0.0056	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C) <sup>(3)</sup>	$\Delta P1dB$	—	0.0077	—	dB/°C

**Table 5. Ordering Information**

Device	Tape and Reel Information	Package
A2T18H410-24SR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	NI-1230S-4L2L

- Part internally matched both on input and output.
- Measurements made with device in an asymmetrical Doherty configuration.
- Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
- $P3dB = P_{avg} + 7.0\text{ dB}$  where  $P_{avg}$  is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

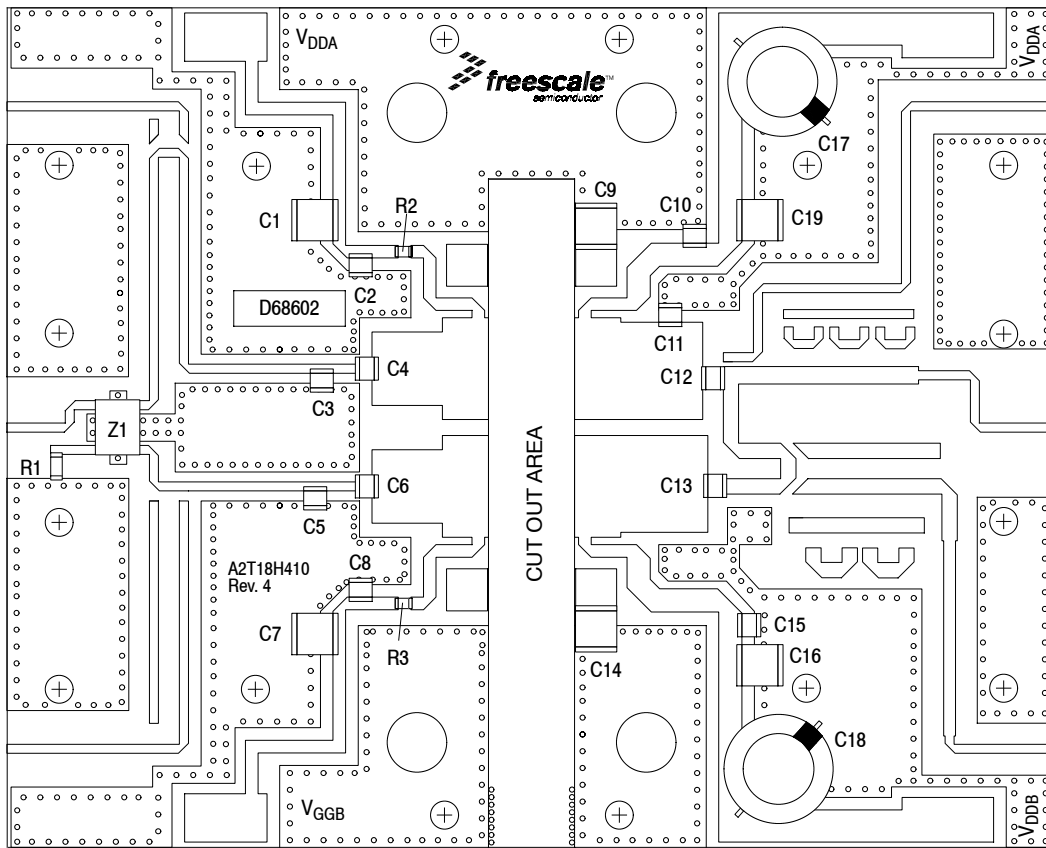
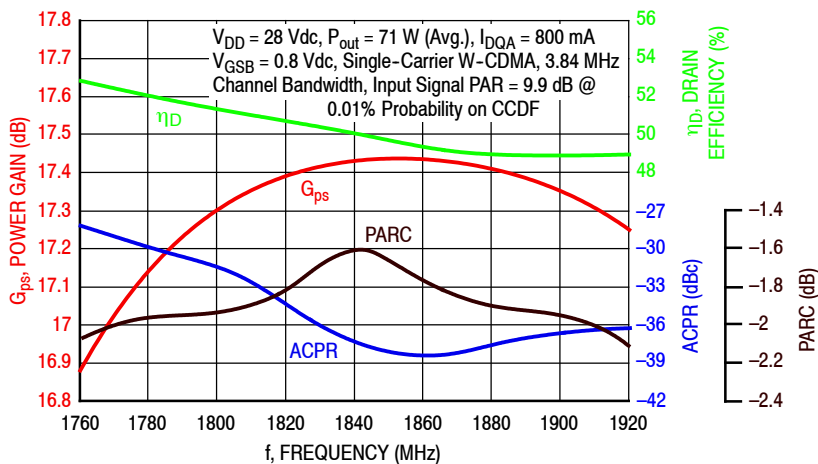


Figure 2. A2T18H410-24SR6 Test Circuit Component Layout

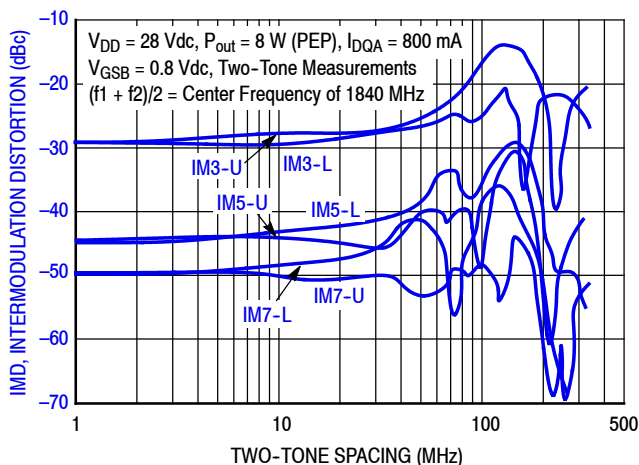
Table 6. A2T18H410-24SR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C7, C9, C14, C16, C19	10 uF Chip Capacitors	C5750X7S2A106M230KB	TDK
C2, C8, C10, C15	12 pF Chip Capacitors	ATC100B120JT500XT	ATC
C3	1.2 pF Chip Capacitor	ATC100B1R2BT500XT	ATC
C4, C6	6.2 pF Chip Capacitors	ATC100B6R2BT500XT	ATC
C5, C11	1.0 pF Chip Capacitors	ATC100B1R0CT500XT	ATC
C12	5.1 pF Chip Capacitor	ATC100B5R1CT500XT	ATC
C13	4.7 pF Chip Capacitor	ATC100B4R7CT500XT	ATC
C17, C18	470 uF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26	Multicomp
R1	50 Ω Termination	CW12010T0050GBK	ATC
R2, R3	2.7 Ω, 1/4 W Chip Resistors	CRCW12062R7FKEA	Vishay
Z1	1700–2000 MHz Band, 5 dB Directional Coupler	X3C19P1-05S	Anaren
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D68602	MTL

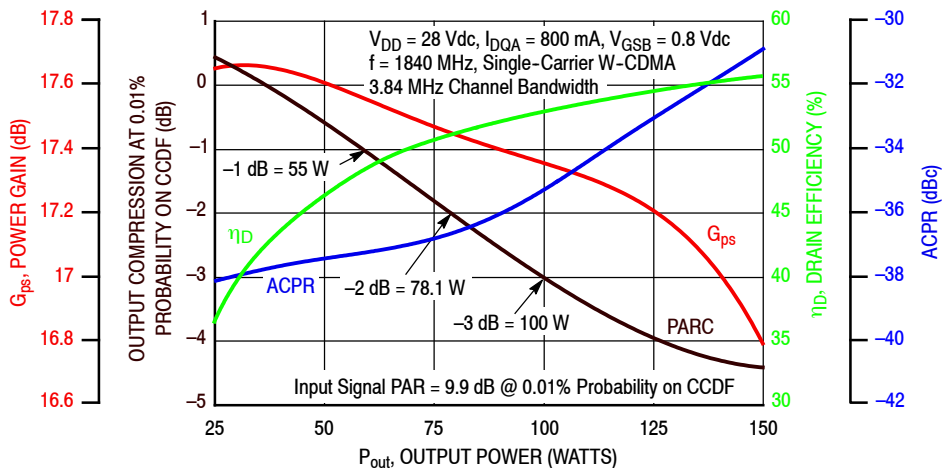
### TYPICAL CHARACTERISTICS



**Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 71$  Watts Avg.**

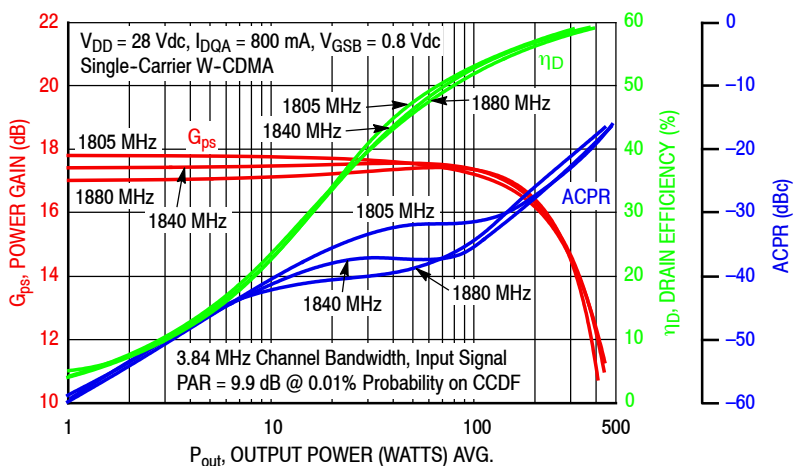


**Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing**

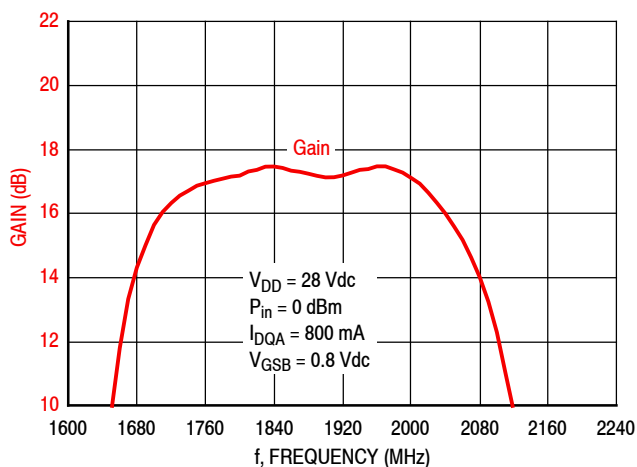


**Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

### TYPICAL CHARACTERISTICS



**Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**



**Figure 7. Broadband Frequency Response**

**Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning**

$V_{DD} = 28$  Vdc,  $I_{DQA} = 785$  mA, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
1805	1.32 – j3.98	1.36 + j3.59	1.01 – j3.41	18.7	52.6	181	58.4	–12
1840	1.57 – j4.28	1.50 + j3.86	0.98 – j3.56	18.7	52.6	183	58.3	–12
1880	2.23 – j4.77	1.99 + j4.16	0.98 – j3.75	18.6	52.6	181	57.2	–12

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
1805	1.32 – j3.98	1.22 + j3.74	1.02 – j3.56	16.5	53.3	215	59.4	–15
1840	1.57 – j4.28	1.37 + j4.04	0.99 – j3.72	16.5	53.4	217	59.2	–15
1880	2.23 – j4.77	1.87 + j4.43	1.00 – j3.90	16.4	53.3	214	58.3	–16

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

$Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$  = Impedance as measured from gate contact to ground.

$Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 8. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning**

$V_{DD} = 28$  Vdc,  $I_{DQA} = 785$  mA, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Drain Efficiency					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
1805	1.32 – j3.98	1.35 + j3.89	2.22 – j2.08	22.4	49.9	98	72.1	–19
1840	1.57 – j4.28	1.55 + j4.11	2.07 – j2.49	22.0	50.3	108	71.1	–17
1880	2.23 – j4.77	2.11 + j4.44	1.93 – j2.67	21.8	50.4	109	70.0	–18

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Drain Efficiency					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
1805	1.32 – j3.98	1.20 + j3.91	2.04 – j2.31	20.1	51.1	128	73.3	–25
1840	1.57 – j4.28	1.38 + j4.21	1.96 – j2.52	19.9	51.2	130	72.5	–24
1880	2.23 – j4.77	1.94 + j4.64	1.93 – j2.64	19.9	51.0	127	71.4	–24

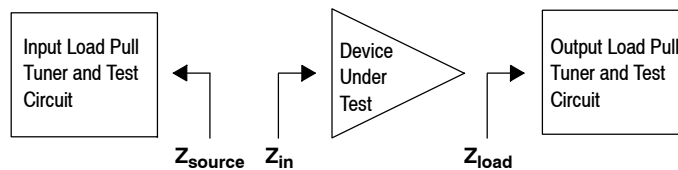
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

$Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$  = Impedance as measured from gate contact to ground.

$Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.



**Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $V_{GSB} = 0.8 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
1805	1.32 – j3.98	1.55 + j4.16	1.38 – j3.61	15.9	54.9	312	57.4	–33
1840	1.84 – j4.30	1.90 + j4.53	1.22 – j3.80	15.6	55.1	321	54.6	–32
1880	2.67 – j4.46	2.83 + j4.90	1.40 – j3.92	16.0	55.0	315	56.4	–33

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
1805	1.32 – j3.98	1.59 + j4.36	1.35 – j3.73	13.7	55.7	370	59.3	–40
1840	1.84 – j4.30	2.01 + j4.79	1.19 – j3.91	13.4	55.8	380	57.1	–39
1880	2.67 – j4.46	3.20 + j5.21	1.38 – j4.21	13.6	55.7	372	57.3	–39

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 $Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

 $Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

 $Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 10. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $V_{GSB} = 0.8 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
1805	1.32 – j3.98	1.39 + j4.15	3.59 – j2.93	17.2	53.0	201	69.3	–41
1840	1.84 – j4.30	1.67 + j4.51	3.49 – j2.75	17.2	53.1	204	69.4	–40
1880	2.67 – j4.46	2.45 + j4.92	3.12 – j2.36	17.3	53.0	199	68.8	–41

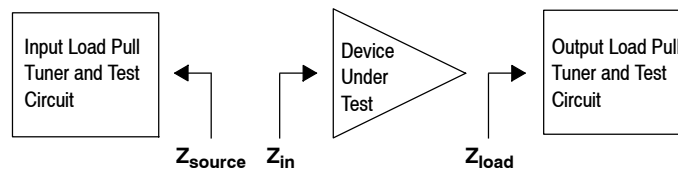
f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
1805	1.32 – j3.98	1.52 + j4.38	3.30 – j3.71	14.8	53.9	248	66.3	–47
1840	1.84 – j4.30	1.91 + j4.81	2.68 – j3.69	14.8	54.7	292	66.2	–45
1880	2.67 – j4.46	2.96 + j5.27	2.97 – j3.26	15.0	54.3	269	66.9	–47

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 $Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

 $Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

 $Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.




### P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1840 MHz

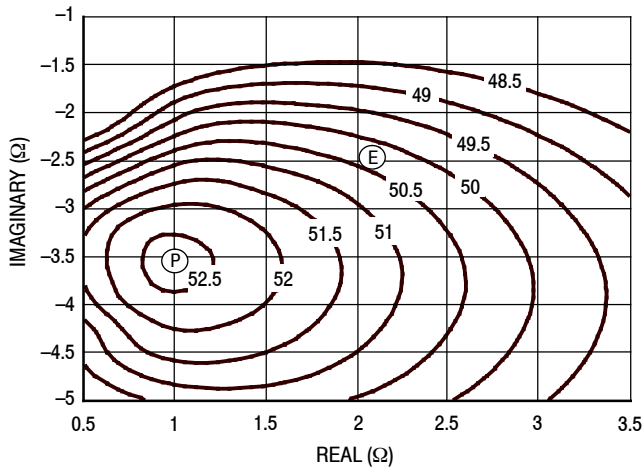


Figure 8. P1dB Load Pull Output Power Contours (dBm)

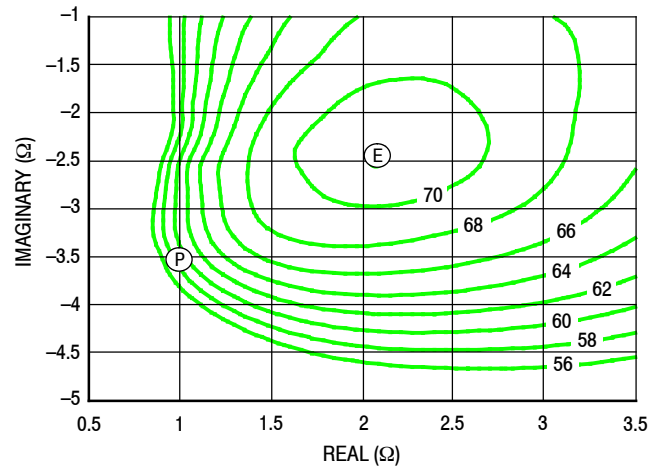


Figure 9. P1dB Load Pull Efficiency Contours (%)

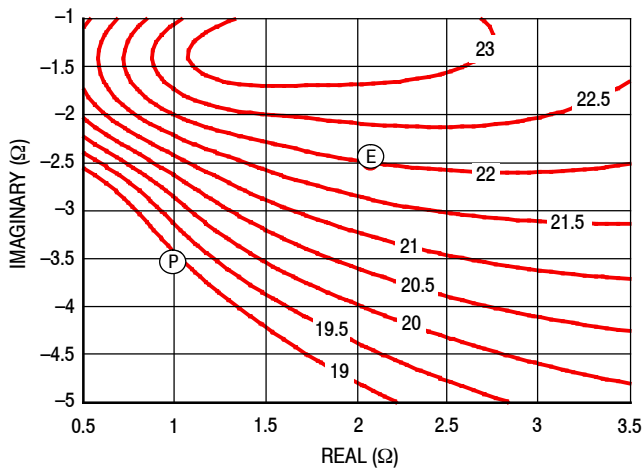


Figure 10. P1dB Load Pull Gain Contours (dB)

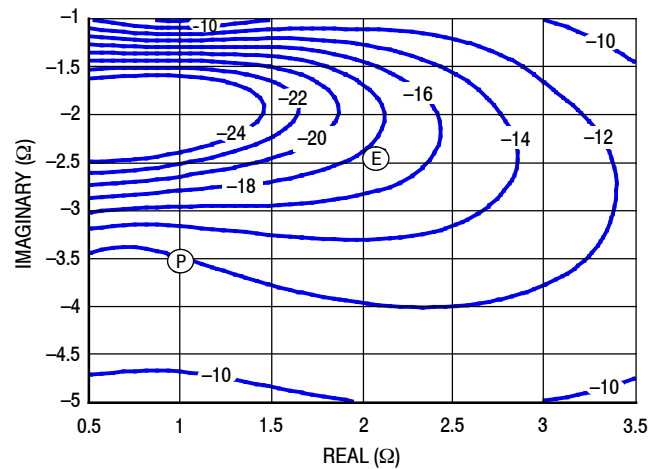


Figure 11. P1dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

### P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1840 MHz

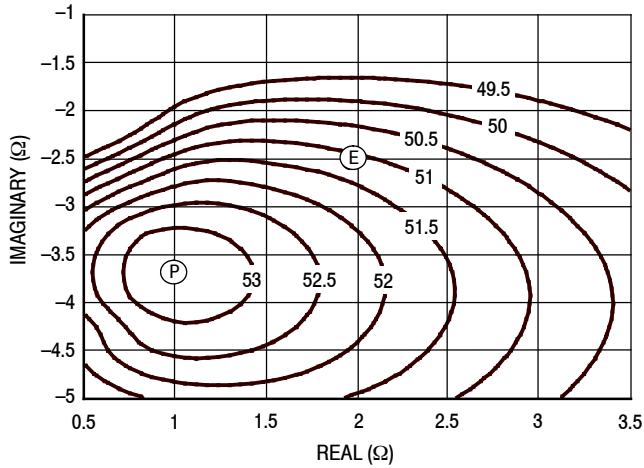


Figure 12. P3dB Load Pull Output Power Contours (dBm)

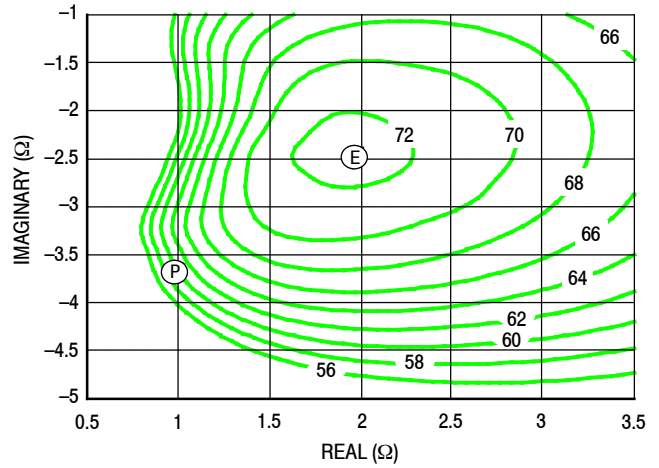


Figure 13. P3dB Load Pull Efficiency Contours (%)

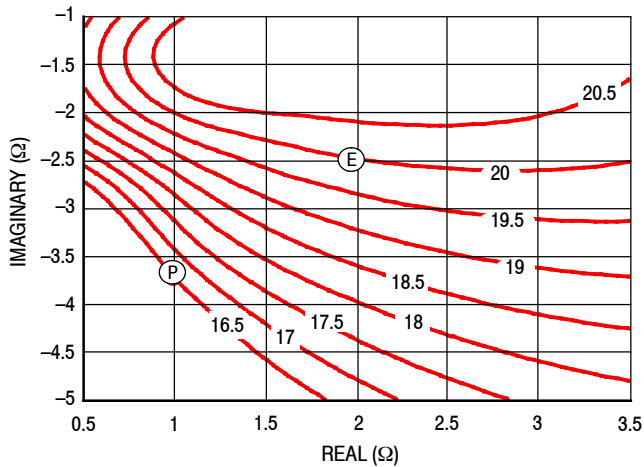


Figure 14. P3dB Load Pull Gain Contours (dB)

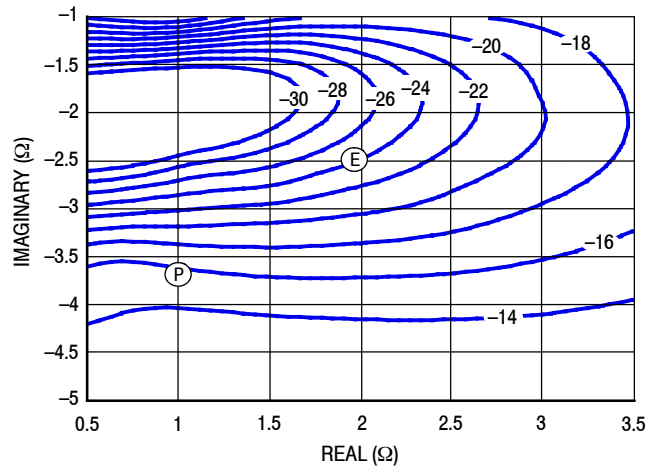
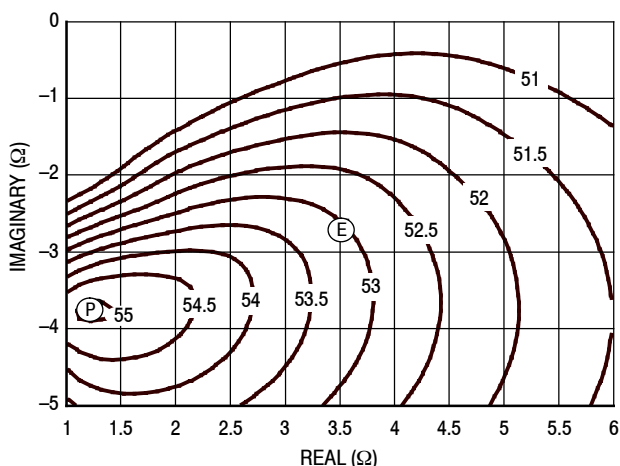


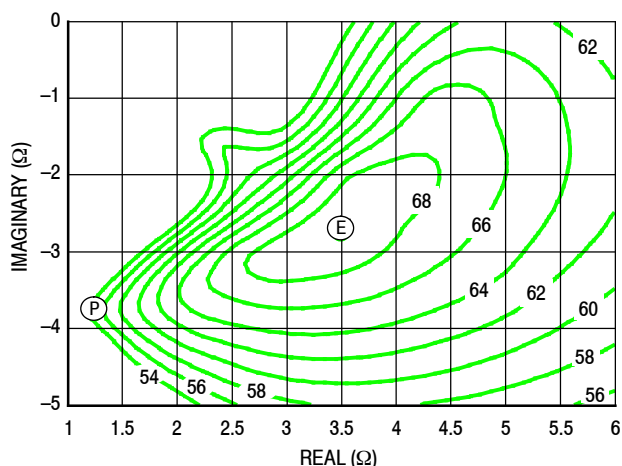
Figure 15. P3dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

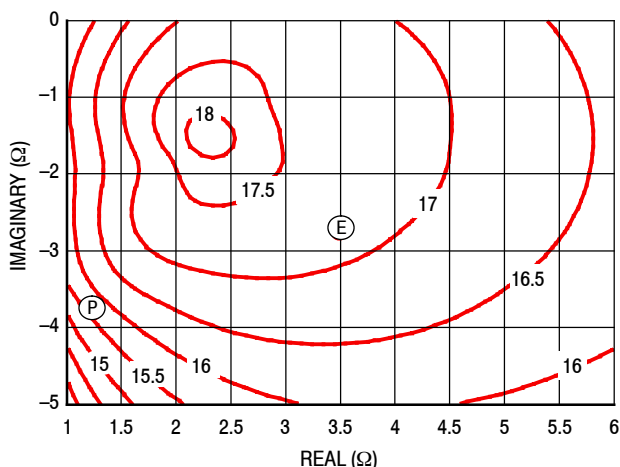
**P1dB – TYPICAL PEAKING LOAD PULL CONTOURS — 1840 MHz**



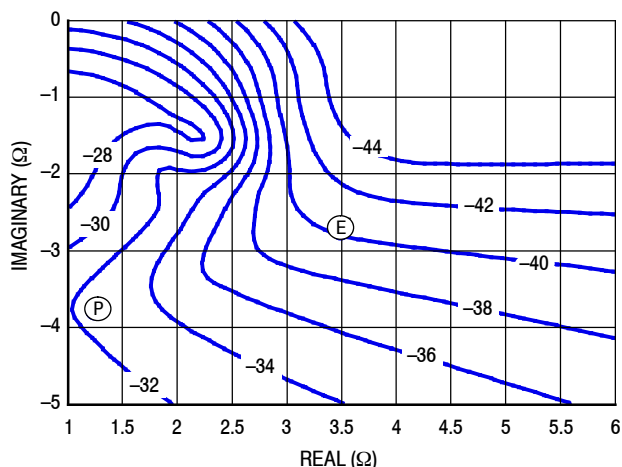
**Figure 16. P1dB Load Pull Output Power Contours (dBm)**



**Figure 17. P1dB Load Pull Efficiency Contours (%)**



**Figure 18. P1dB Load Pull Gain Contours (dB)**



**Figure 19. P1dB Load Pull AM/PM Contours (°)**

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

### P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1840 MHz

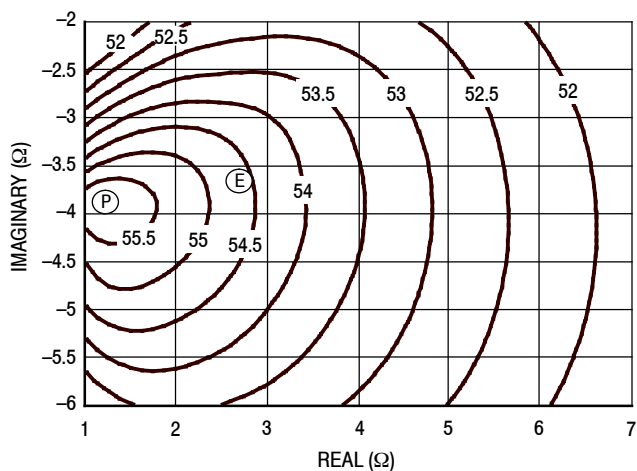


Figure 20. P3dB Load Pull Output Power Contours (dBm)

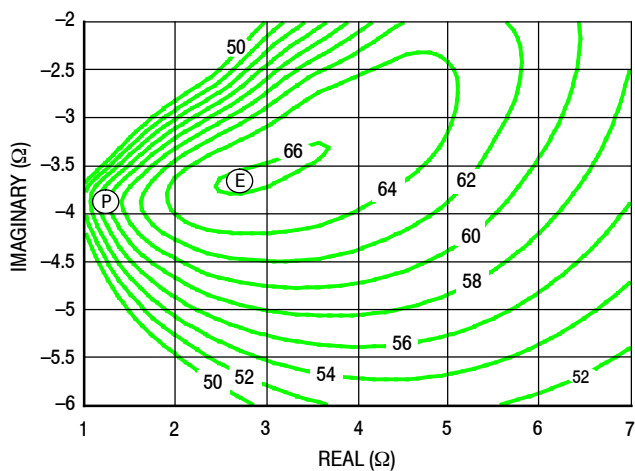


Figure 21. P3dB Load Pull Efficiency Contours (%)

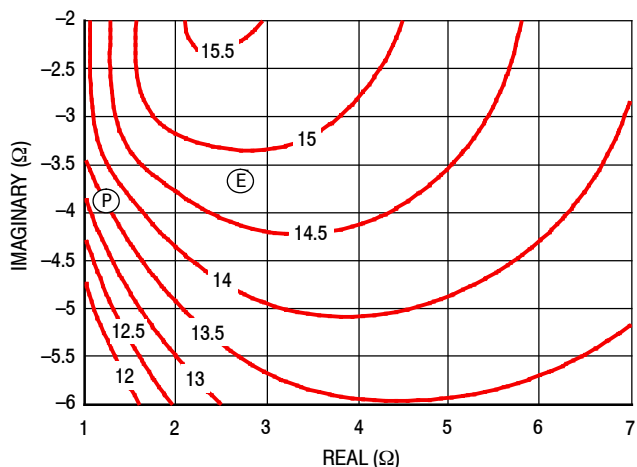


Figure 22. P3dB Load Pull Gain Contours (dB)

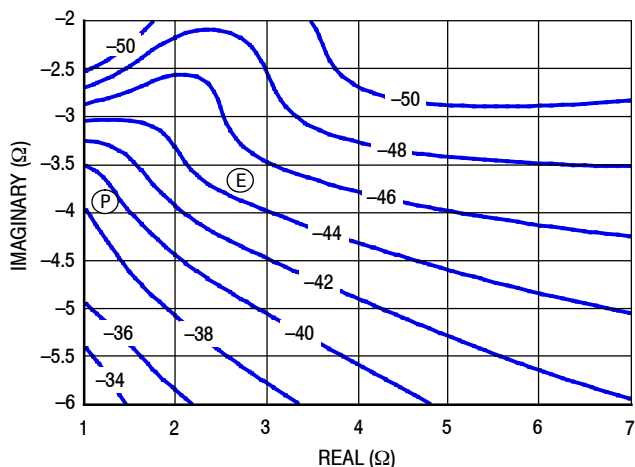
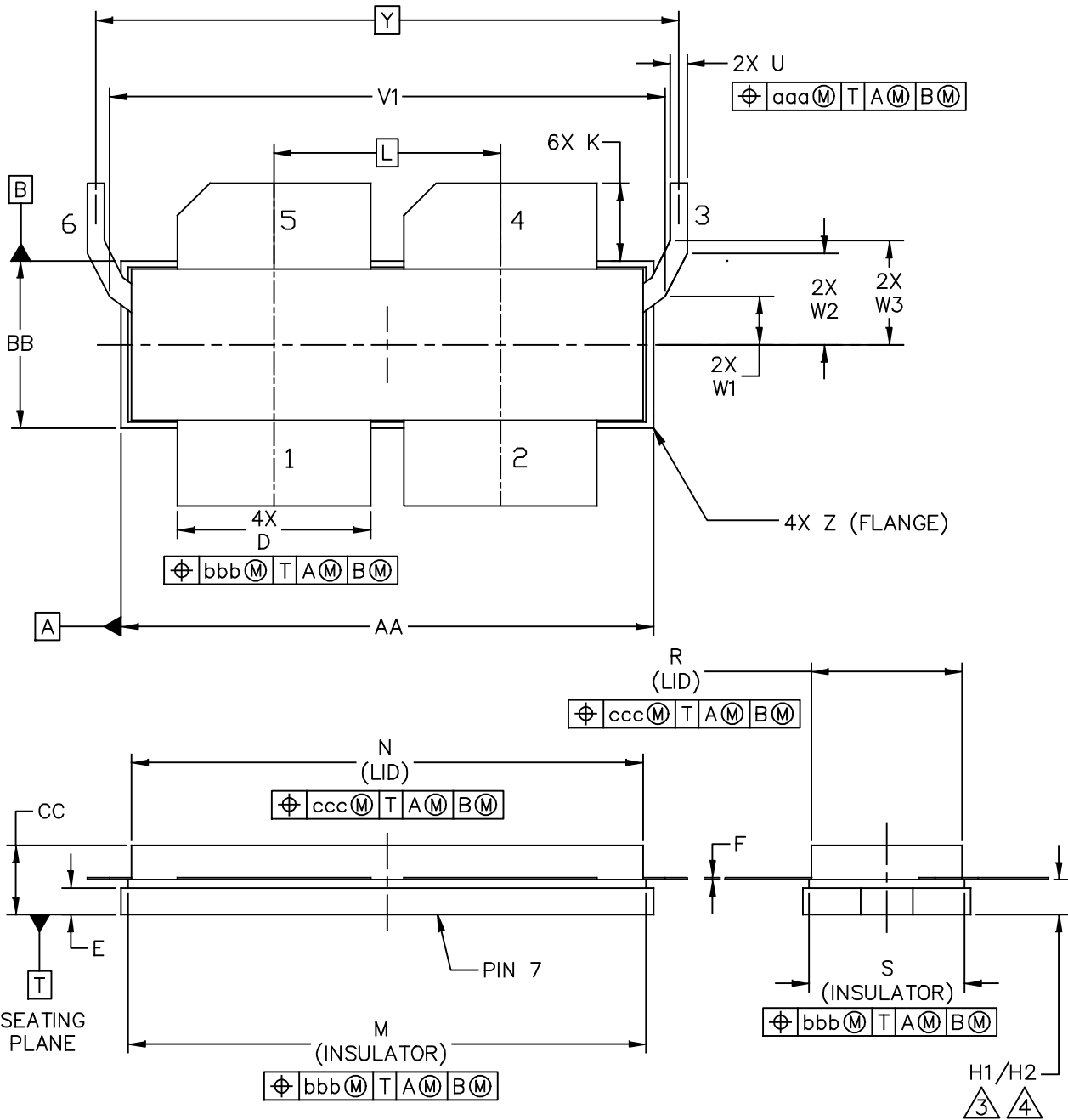


Figure 23. P3dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

PACKAGE DIMENSIONS



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NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	1.265	1.275	32.13	32.39	N	1.218	1.242	30.94	31.55
BB	.395	.405	10.03	10.29	R	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	S	.365	.375	9.27	9.53
D	.455	.465	11.56	11.81	U	.035	.045	0.89	1.14
E	.062	.066	1.57	1.68	V1	1.320	1.330	33.53	33.78
F	.004	.007	0.10	0.18	W1	.110	.120	2.79	3.05
H1	.082	.090	2.08	2.29	W2	.213	.223	5.41	5.66
H2	.078	.094	1.98	2.39	W3	.243	.253	6.17	6.43
K	.175	.195	4.45	4.95	Y	1.390 BSC		35.31 BSC	
L	.540 BSC		13.72 BSC		Z	R.000	R.040	R0.00	R1.02
M	1.219	1.241	30.96	31.52	aaa	.015		0.38	
					bbb	.010		0.25	
					ccc	.020		0.51	

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Refer to the following resources to aid your design process.

**Application Notes**

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

**Engineering Bulletins**

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

**Software**

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

**Development Tools**

- Printed Circuit Boards

**To Download Resources Specific to a Given Part Number:**

1. Go to <http://www.freescale.com/rf>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

**REVISION HISTORY**

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2015	• Initial Release of Data Sheet

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