

A2I09VD030N/030GN

RF LDMOS Wideband Integrated Power Amplifiers

Rev. 3.0 — 24 September 2026

Product data sheet



1 General description

The A2I09VD030N wideband integrated circuit is designed with on-chip matching that makes it usable from 575 MHz to 1300 MHz. This multi-stage structure is rated for 48 V to 55 V operation and covers all typical cellular base station modulation formats.

2 Features and benefits

- On-chip matching (50 Ω input, DC blocked)
- Integrated quiescent current temperature compensation with enable/disable function¹
- Designed for digital predistortion error correction systems
- Optimized for Doherty applications

3 Typical performance

Table 1. Typical W-CDMA performance — 900 MHz

Typical Single-Carrier W-CDMA Performance: $V_{DD} = 48$ Vdc, $I_{DQ1(A+B)} = 46$ mA, $I_{DQ2(A+B)} = 154$ mA, $P_{out} = 4$ W Avg., Input Signal PAR= 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
920 MHz	34.4	19.9	-45.0
940 MHz	34.5	20.0	-44.6
960 MHz	34.3	19.8	-44.3

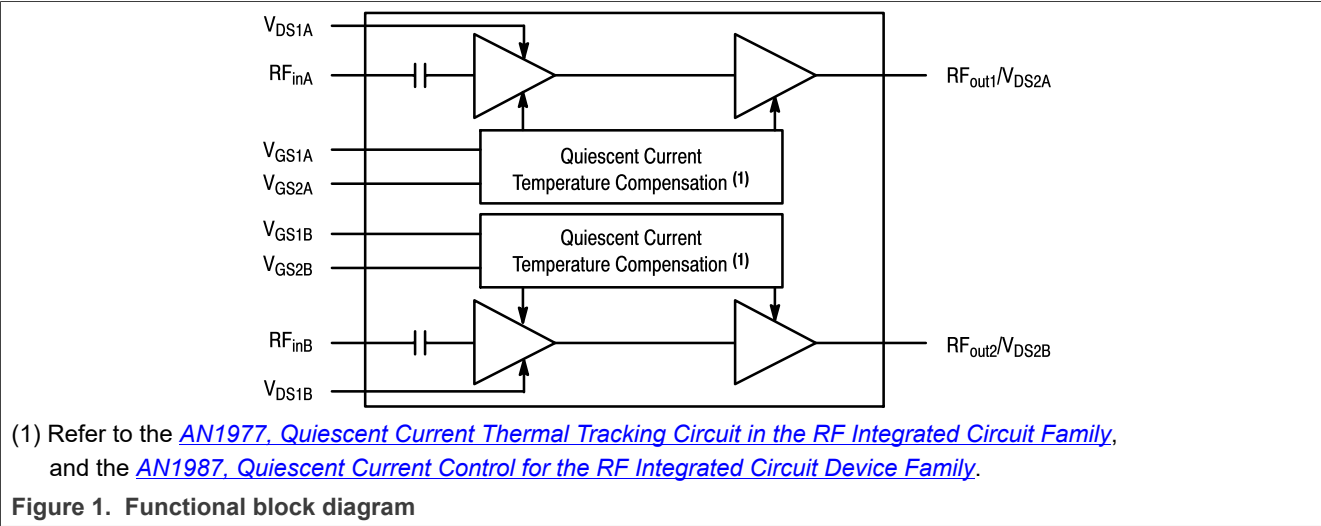
Table 2. Typical W-CDMA performance — 780 MHz

Typical Single-Carrier W-CDMA Performance: $V_{DD} = 48$ Vdc, $I_{DQ1(A+B)} = 50$ mA, $I_{DQ2(A+B)} = 150$ mA, $P_{out} = 4$ W Avg., Input Signal PAR= 9.9 dB @ 0.01% Probability on CCDF.

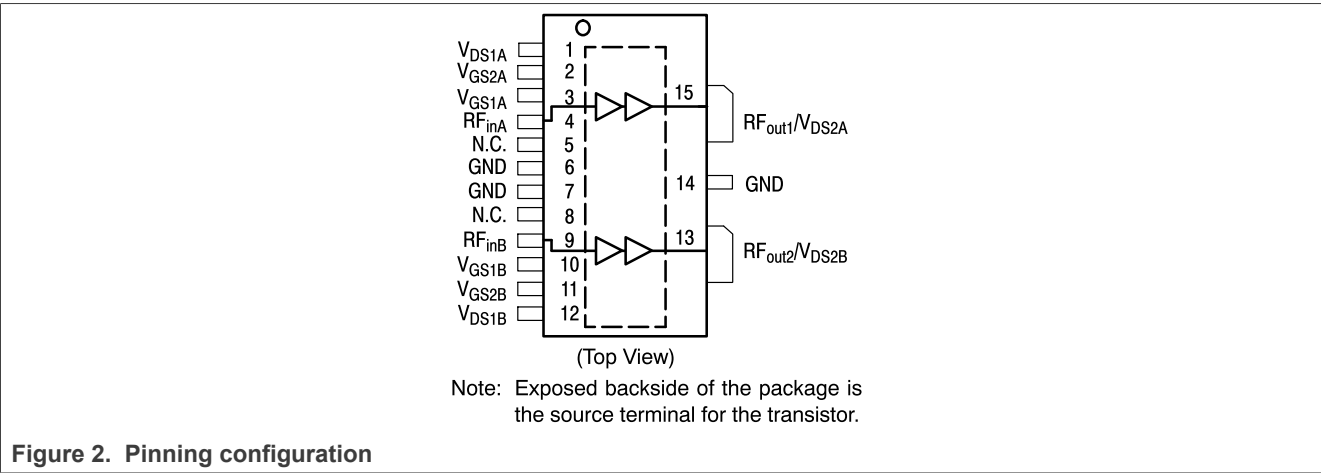
Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
728 MHz	30.9	19.6	-44.7
748 MHz	31.1	19.5	-45.5
768 MHz	31.2	19.3	-46.2

¹ Refer to the [AN1977, Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family](#), and the [AN1987, Quiescent Current Control for the RF Integrated Circuit Device Family](#).

4 Functional block diagram



5 Pinning information



6 Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
A2I09VD030NR1	TO-270WB-15	R1 Suffix = 500 Units, 44 mm Tape Width, 13-inch Reel	SOT1722-1
A2I09VD030GNR1	TO-270WBG-15		SOT1722-3

7 Limiting values

Table 4. Limiting values

Rating	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	-0.5, +105	Vdc
Gate-source Voltage	V_{GS}	-0.5, +10	Vdc
Operating Voltage	V_{DD}	+0, 55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range ^{[1] [2]}	T_J	-40 to +225	°C
Input Power	P_{in}	20	dBm

[1] Continuous use at maximum temperature will affect MTTF.

[2] Refer to [AN1955, Thermal Measurement Methodology of RF Power Amplifiers](#).

8 Thermal characteristics

Table 5. Thermal characteristics

Characteristic	Symbol	Value ^[1]	Unit
Thermal Resistance, Junction to Case Case Temperature 73 °C, 4 W Avg., W-CDMA, 940 MHz Stage 1, 48 Vdc, $I_{DQ1(A+B)}$ 46 mA Stage 2, 48 Vdc, $I_{DQ2(A+B)}$ 154 mA	$R_{\theta JC}$	6.7 2.8	°C/W

[1] Refer to [AN1955, Thermal Measurement Methodology of RF Power Amplifiers](#).

9 ESD protection characteristics

Table 6. ESD protection characteristics

Test methodology	Class
Human Body Model (per JESD22-A114)	1B
Charge Device Model (per JESD22-C101)	C0B

10 Moisture sensitivity level

Table 7. Moisture sensitivity level

Test methodology	Rating	Package peak temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

11 Electrical characteristics

Table 8. Electrical characteristics
(T_A = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off characteristics ^[1]					
Zero Gate Voltage Drain Leakage Current (V _{DS} = 105 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 55 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V _{GS} = 1.5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
On characteristics					
Gate Threshold Voltage ^[1] (V _{DS} = 10 Vdc, I _D = 1.5 μAdc)	V _{GS(th)}	1.3	1.8	2.3	Vdc
Fixture Gate Quiescent Voltage (V _{DD} = 48 Vdc, I _{DQ1(A+B)} = 46 mAdc, Measured in Functional Test)	V _{GS(Q)}	4.8	5.5	6.4	Vdc
Off characteristics ^[1]					
Zero Gate Voltage Drain Leakage Current (V _{DS} = 105 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 55 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V _{GS} = 1.5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
On characteristics					
Gate Threshold Voltage ^[1] (V _{DS} = 10 Vdc, I _D = 7 μAdc)	V _{GS(th)}	1.3	1.8	2.3	Vdc
Fixture Gate Quiescent Voltage (V _{DD} = 48 Vdc, I _{DQ2(A+B)} = 154 mAdc, Measured in Functional Test)	V _{GS(Q)}	4.0	5.0	5.6	Vdc
Drain-Source On-Voltage ^[1] (V _{GS} = 10 Vdc, I _D = 100 mAdc)	V _{DS(on)}	0.1	0.8	1.5	Vdc
Functional tests ^{[2] [3]} (In NXP Doherty Test Fixture, 50 Ω system) V _{DD} = 48 Vdc, I _{DQ1(A+B)} = 46 mA, I _{DQ2(A+B)} = 154 mA, P _{out} = 4 W Avg., f = 960 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power gain	G _{ps}	32.0	34.3	35.6	dB
Power added efficiency	PAE	18.5	19.8	—	%
Output Peak-to-average Ratio @ 0.01% Probability on CCDF	PAR	8.9	9.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	-44.3	-41.1	dBc
Load mismatch (In NXP Doherty Test Fixture, 50 Ω system) I _{DQ1(A+B)} = 46 mA, I _{DQ2(A+B)} = 154 mA, f = 940 MHz					
VSWR 10:1 at 55 Vdc, 44.5 W CW Output Power (3 dB Input Overdrive from 33 W CW Rated Power)	No Device Degradation				
Typical performance (In NXP Doherty Test Fixture, 50 Ω system) V _{DD} = 48 Vdc, I _{DQ1(A+B)} = 46 mA, I _{DQ2(A+B)} = 154 mA, 920 MHz – 960 MHz bandwidth					
P _{out} @ 1 dB Compression Point, CW	P1dB	—	33.3	—	W
P _{out} @ 3 dB Compression Point ^[4]	P3dB	—	40.5	—	W

Table 8. Electrical characteristics ...continued*(T_A = 25 °C unless otherwise noted)*

Characteristic	Symbol	Min	Typ	Max	Unit
AM/PM (Maximum value measured at the P3dB compression point across the 920 MHz – 960 MHz frequency range)	Φ	—	-22	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW _{res}	—	70	—	MHz
Quiescent Current Accuracy over Temperature ^[5] with 2 k Ω Gate Feed Resistors (-30 to 85 °C) Stage 1 with 2 k Ω Gate Feed Resistors (-30 to 85 °C) Stage 2	ΔI_{QT}	— —	2 8	— —	%
Gain Flatness in 40 MHz Bandwidth @ P _{out} = 120 W Avg.	G _F	—	0.29	—	dB
Gain Variation over Temperature (-30 °C to +85 °C)	ΔG	—	0.004	—	dB/°C
Output Power Variation over Temperature (-30 °C to +85 °C)	ΔP_{1dB}	—	0.014	—	dB/°C

[1] Each side of device measured separately.

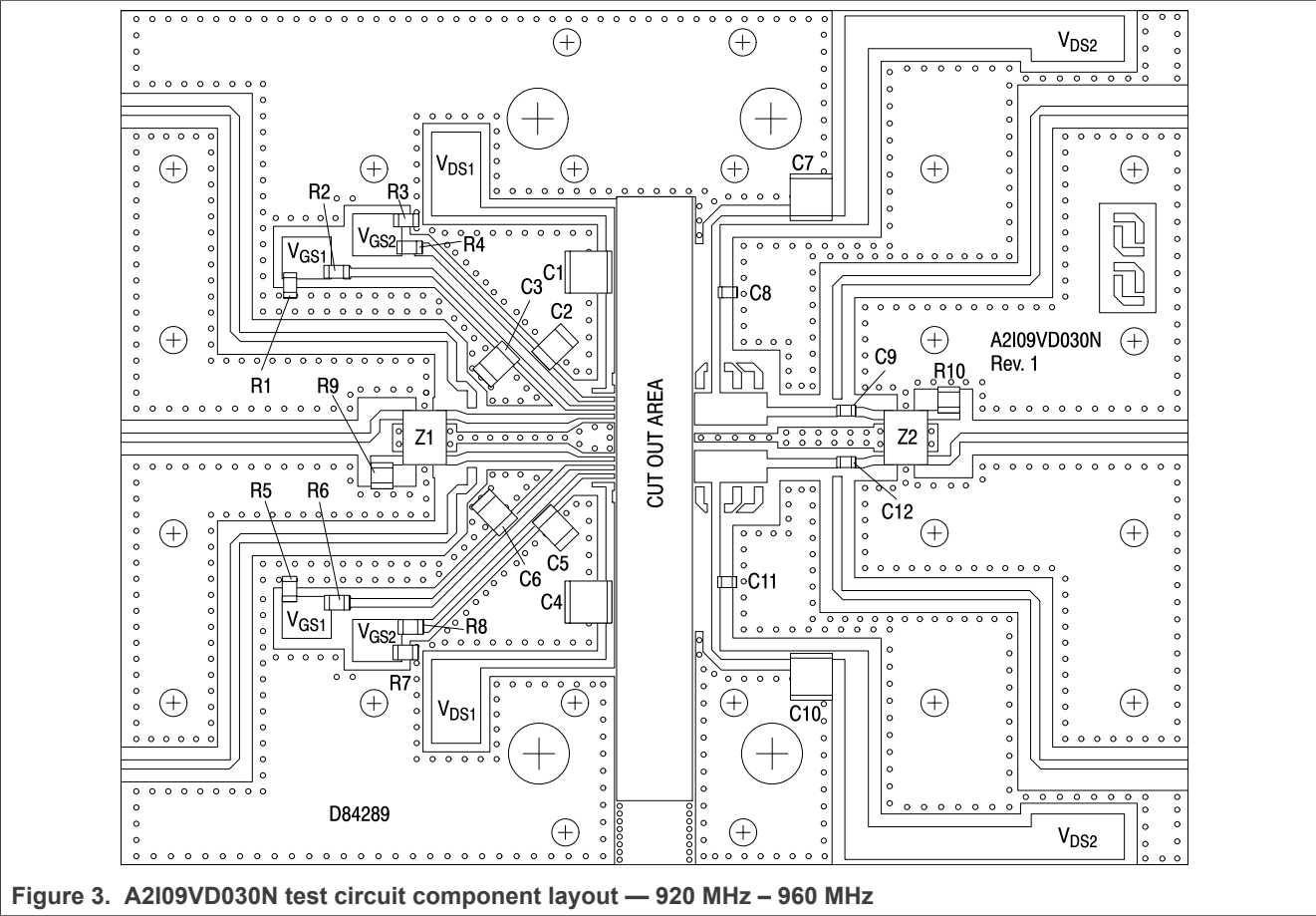
[2] Part internally input matched.

[3] Measurement made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.

[4] P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01 % probability on CCDF.[5] Refer to the [AN1977, Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family](#), and the [AN1987, Quiescent Current Control for the RF Integrated Circuit Device Family](#).

12 Component layout and parts list — 920 MHz – 960 MHz

12.1 Component layout — 920 MHz – 960 MHz



12.2 Component designations and values — 920 MHz – 960 MHz

Table 9. A2I09VD030N test circuit component designations and values — 920 MHz – 960 MHz

Part	Description	Part number	Manufacturer
C1, C4, C7, C10	10 μ F Chip Capacitor	C5750X7S2A106M	TDK
C2, C3, C5, C6	3.3 μ F Chip Capacitor	C4532X7R1H335K	TDK
C8, C9, C11, C12	47 pF Chip Capacitor	ATC600F470JT250XT	ATC
R1, R3, R5, R7	51 k Ω , 1/4 W Chip Resistor	CRCW120651K0JNEA	Vishay
R2, R4, R6, R8	1.5 k Ω , 1/4 W Chip Resistor	CRCW12061K50FKEA	Vishay
R9, R10	50 Ω , 4 W Chip Resistor	C10A50Z4	Anaren
Z1, Z2	800 MHz – 1000 MHz, 90°, 3 dB Hybrid Coupler	X3C09P1-03S	Anaren
PCB	Rogers RO4350B, 0.020", ϵ_r = 3.66	D84289	MTL

13 Typical characteristics — 920 MHz – 960 MHz

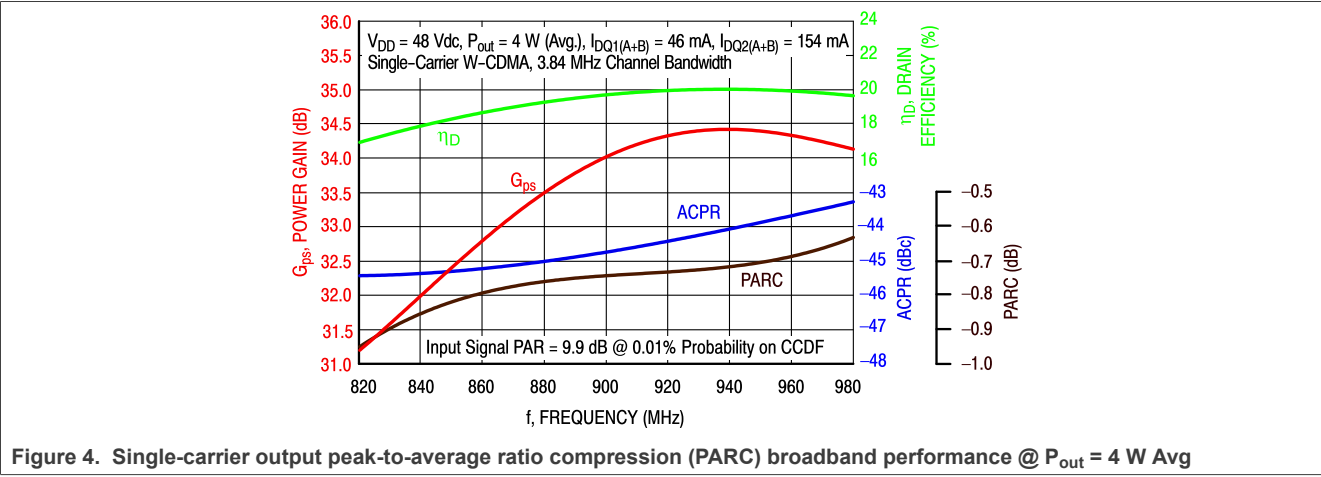


Figure 4. Single-carrier output peak-to-average ratio compression (PARC) broadband performance @ $P_{out} = 4$ W Avg

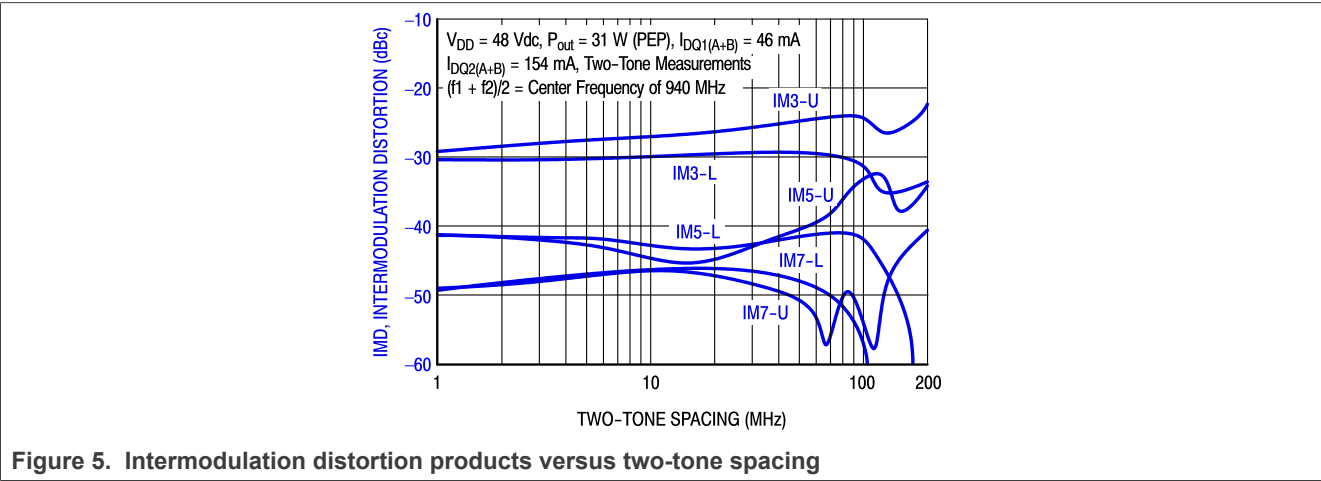


Figure 5. Intermodulation distortion products versus two-tone spacing

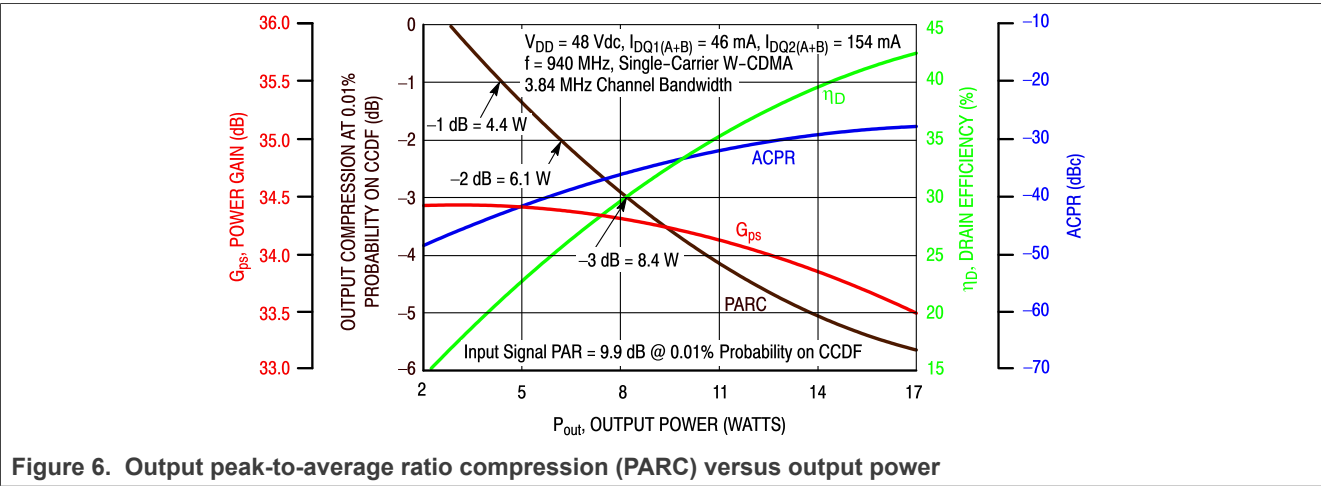


Figure 6. Output peak-to-average ratio compression (PARC) versus output power

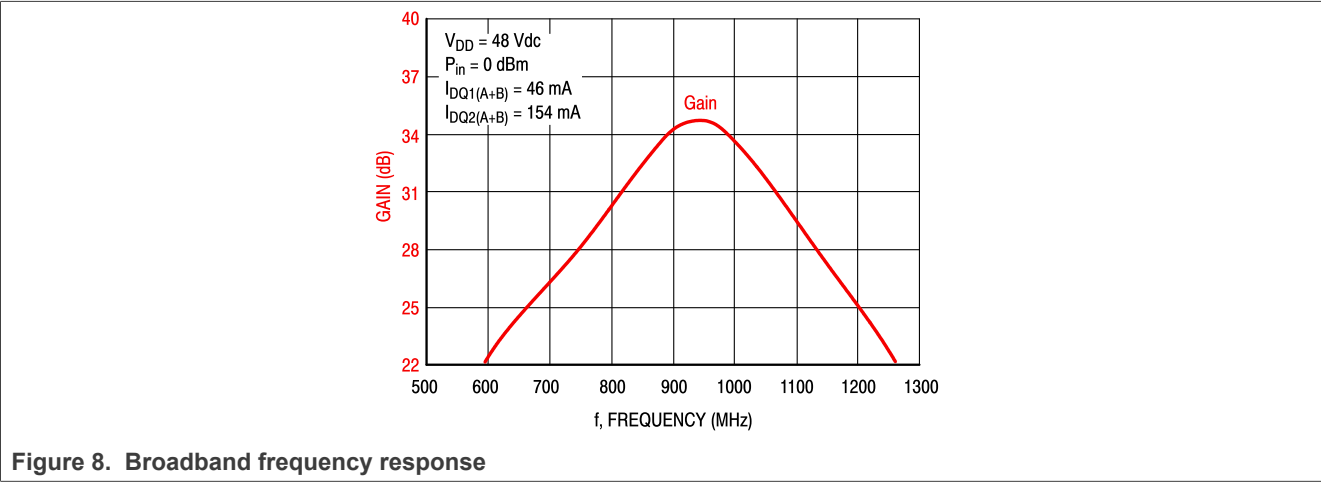
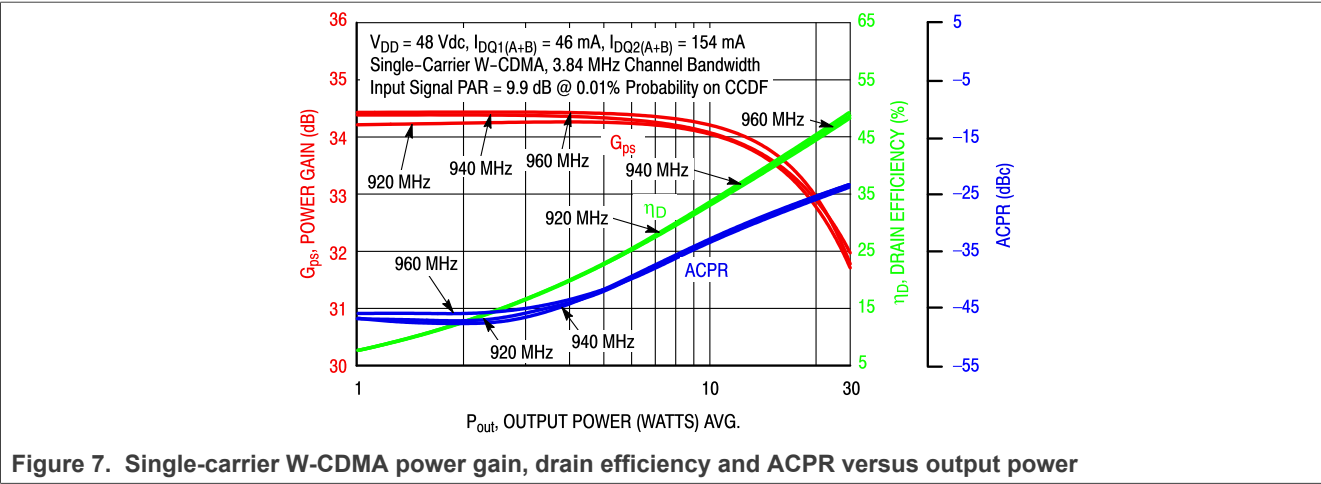


Table 10. Load pull performance — Maximum power tuning — P1dB
 $V_{DD} = 48\text{ Vdc}$, $I_{DQ1} = 23\text{ mA}$, $I_{DQ2} = 77\text{ mA}$, Pulsed CW, 10 $\mu\text{sec(on)}$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{[1]}$ (Ω)	Gain (dB)	(dBm)	(W)	ηD (%)	AM/PM ($^\circ$)
920	42.0 – j3.99	47.6 + j4.36	19.0 + j17.4	33.0	43.5	22	62.4	-4
940	51.7 – j4.27	55.1 + j9.85	20.8 + j17.3	33.0	43.6	23	62.5	-4
960	61.3 – j9.97	64.0 + j11.2	21.8 + j17.6	32.9	43.8	24	63.6	-4

[1] Load impedance for optimum P1dB power.

Table 11. Load pull performance — Maximum power tuning — P3dB $V_{DD} = 48 \text{ Vdc}$, $I_{DQ1} = 23 \text{ mA}$, $I_{DQ2} = 77 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{[1]}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	42.0 – j3.99	48.7 + j4.46	21.2 + j15.9	30.8	44.4	27	64.2	-4
940	51.7 – j4.27	55.9 + j9.75	22.3 + j15.8	30.7	44.4	27	63.6	-4
960	61.3 – j9.97	64.5 + j10.9	22.3 + j16.1	30.7	44.5	28	63.9	-4

[1] Load impedance for optimum P3dB power.

Table 12. Load pull performance — Maximum efficiency tuning — P1dB $V_{DD} = 48 \text{ Vdc}$, $I_{DQ1} = 23 \text{ mA}$, $I_{DQ2} = 77 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{[1]}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	42.0 – j3.99	47.5 + j11.4	13.9 + j32.8	36.0	40.9	12	72.4	-6
940	51.7 – j4.27	56.3 + j13.8	17.7 + j28.9	34.9	42.3	17	71.3	-5
960	61.3 – j9.97	66.7 + j14.6	17.7 + j30.1	34.8	42.2	17	71.7	-6

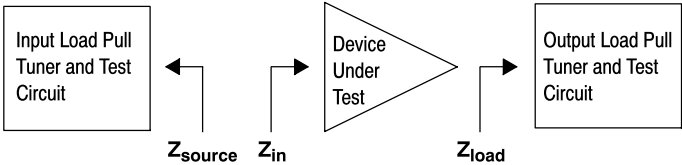
[1] Load impedance for optimum P1dB power.

Table 13. Load pull performance — Maximum efficiency tuning — P3dB $V_{DD} = 48 \text{ Vdc}$, $I_{DQ1} = 23 \text{ mA}$, $I_{DQ2} = 77 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

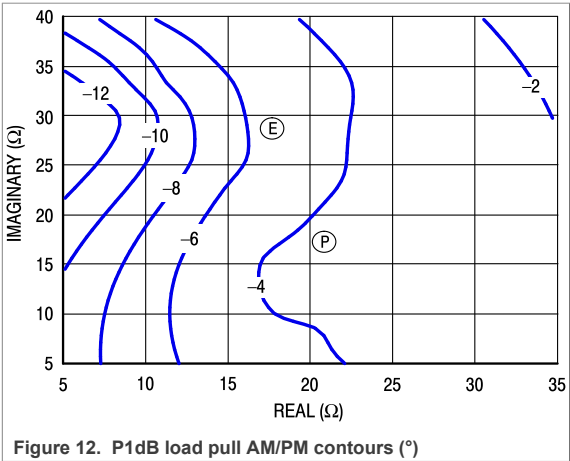
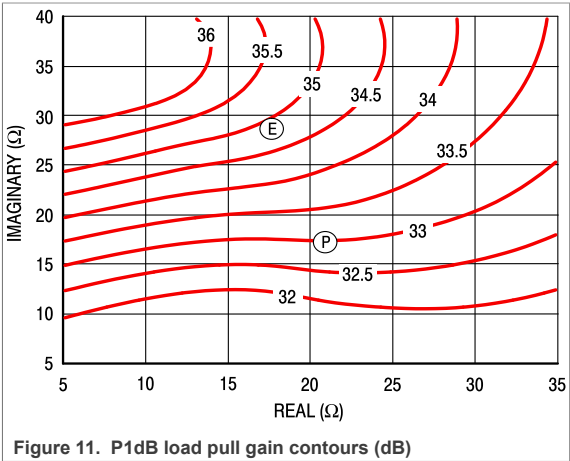
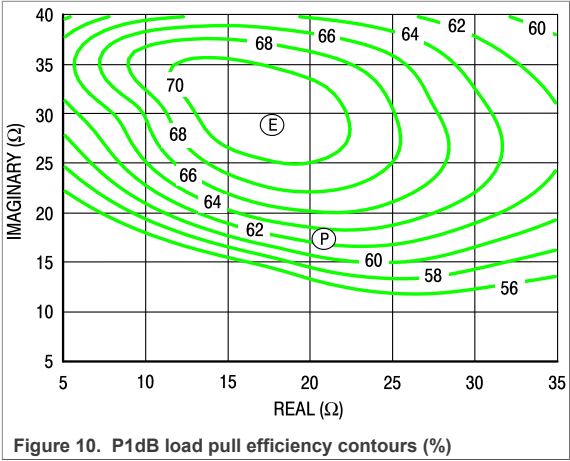
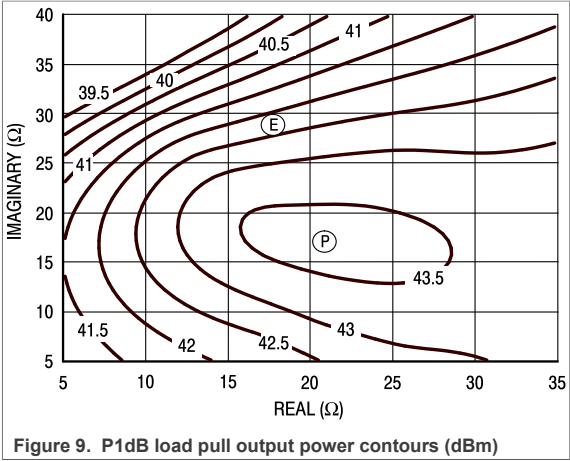
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{[1]}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	42.0 – j3.99	50.2 + j11.4	13.4 + j33.0	34.1	41.6	15	73.9	-10
940	51.7 – j4.27	57.5 + j13.6	17.4 + j29.2	32.9	42.9	20	72.3	-7
960	61.3 – j9.97	68.0 + j14.3	17.0 + j30.8	32.9	42.7	19	72.4	-7

[1] Load impedance for optimum P3dB power.

Notes:*Measurement made on a per side basis* Z_{source} = Measured impedance presented to the input of the device at the package reference plane. Z_{in} = Impedance as measured from gate contact to ground. Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



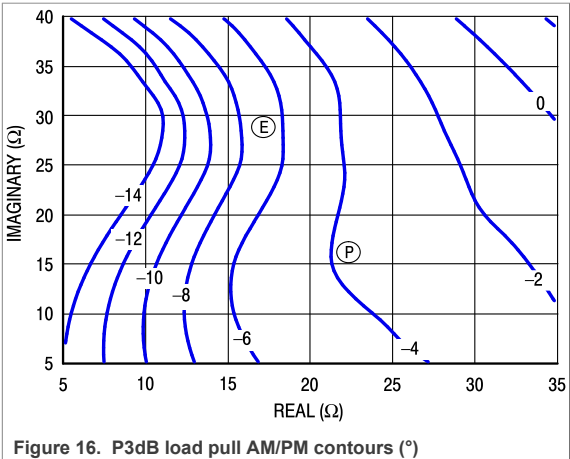
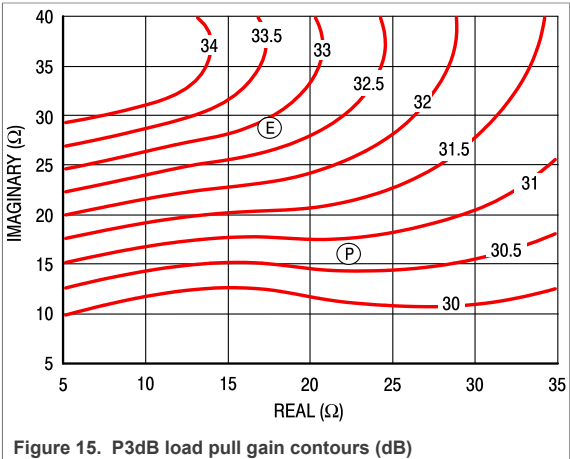
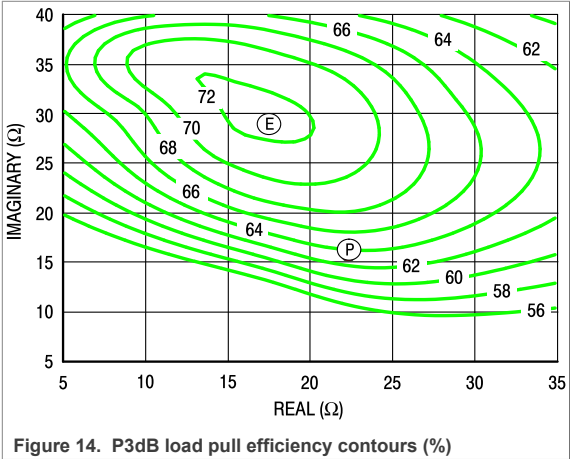
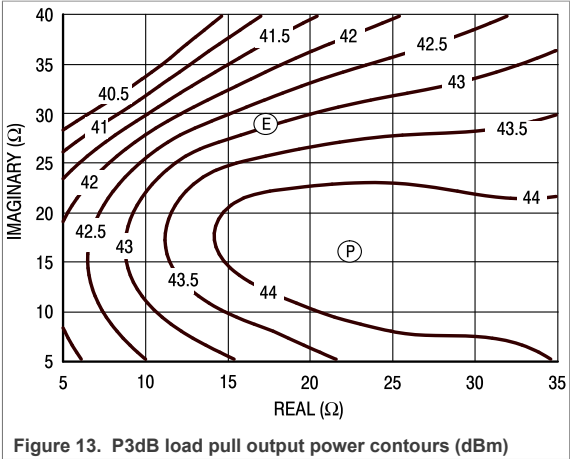
14 P1dB – Typical load pull contours — 940 MHz



NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

15 P3dB – Typical load pull contours — 940 MHz

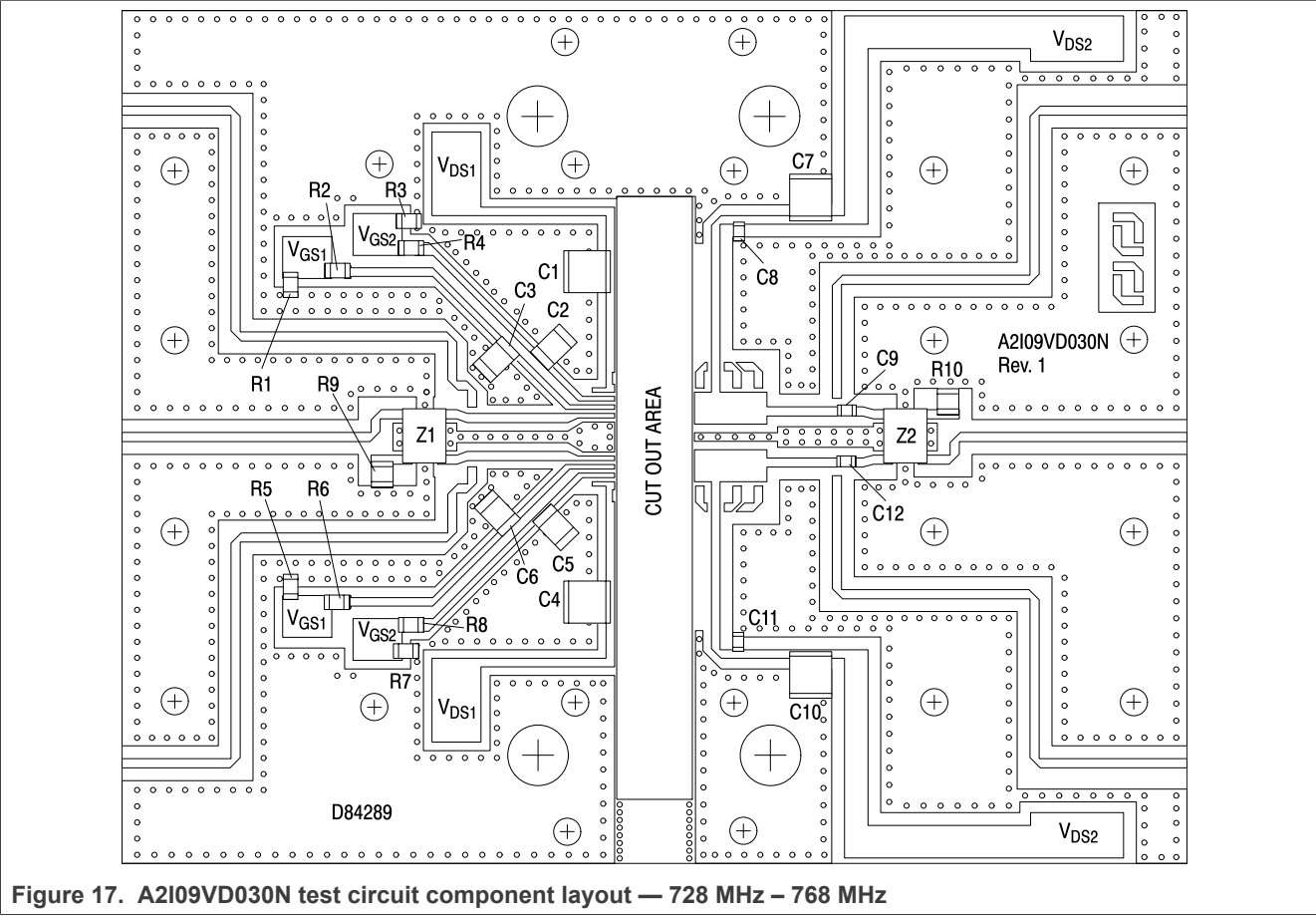


NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

16 Component layout and parts list — 728 MHz – 768 MHz

16.1 Component layout — 728 MHz – 768 MHz



16.2 Component designations and values — 728 MHz – 768 MHz

Table 14. A2I09VD030N test circuit component designations and values — 728 MHz – 768 MHz

Part	Description	Part number	Manufacturer
C1, C4, C7, C10	10 μ F Chip Capacitor	C5750X7S2A106M	TDK
C2, C3, C5, C6	3.3 μ F Chip Capacitor	C4532X7R1H335K	TDK
C8, C9, C11, C12	47 pF Chip Capacitor	ATC600F470JT250XT	ATC
R1, R3, R5, R7	51 k Ω , 1/4 W Chip Resistor	CRCW120651K0JNEA	Vishay
R2, R4, R6, R8	1.5 k Ω , 1/4 W Chip Resistor	CRCW12061K50FKEA	Vishay
R9, R10	50 Ω , 4 W Chip Resistor	C10A50Z4	Anaren
Z1, Z2	600 MHz – 900 MHz, 90°, 3 dB Hybrid Coupler	X3C07P1-03S	Anaren
PCB	Rogers RO4350B, 0.020", ϵ_r = 3.66	D84289	MTL

17 Typical characteristics — 728 MHz – 768 MHz

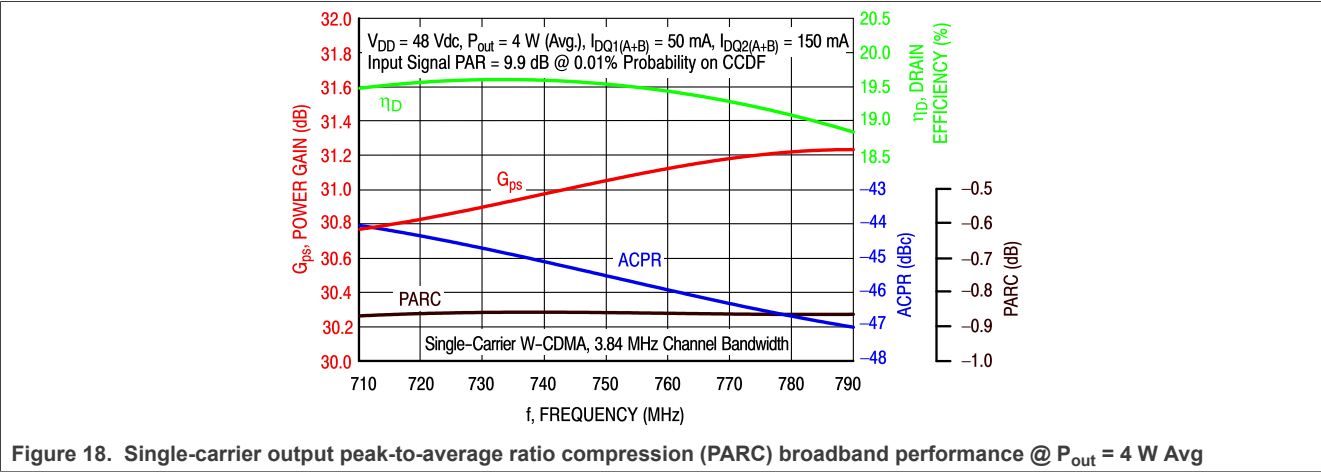


Figure 18. Single-carrier output peak-to-average ratio compression (PARC) broadband performance @ $P_{out} = 4$ W Avg

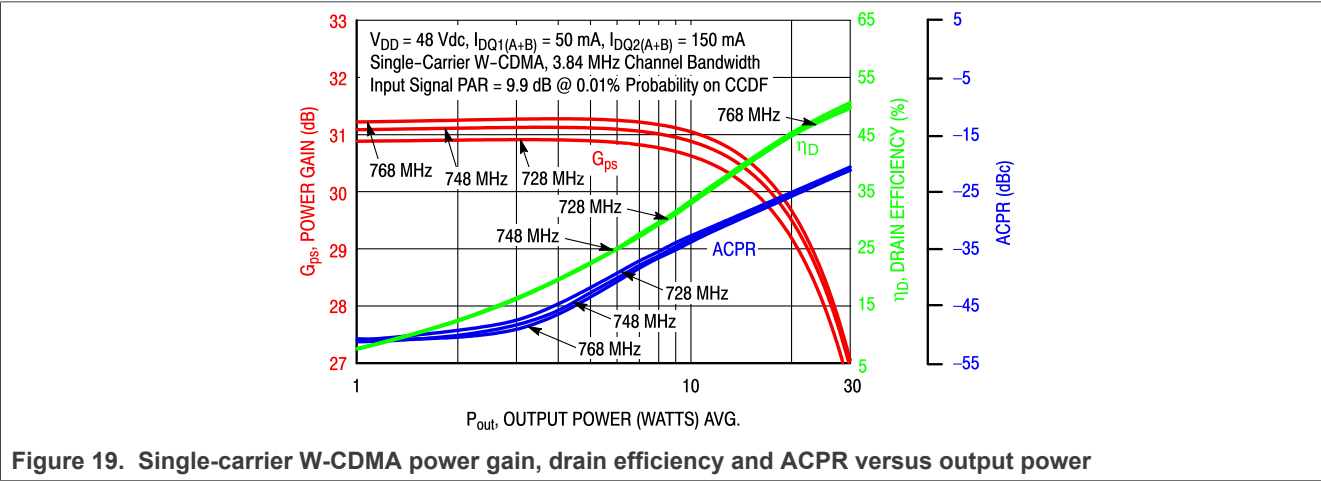


Figure 19. Single-carrier W-CDMA power gain, drain efficiency and ACPR versus output power

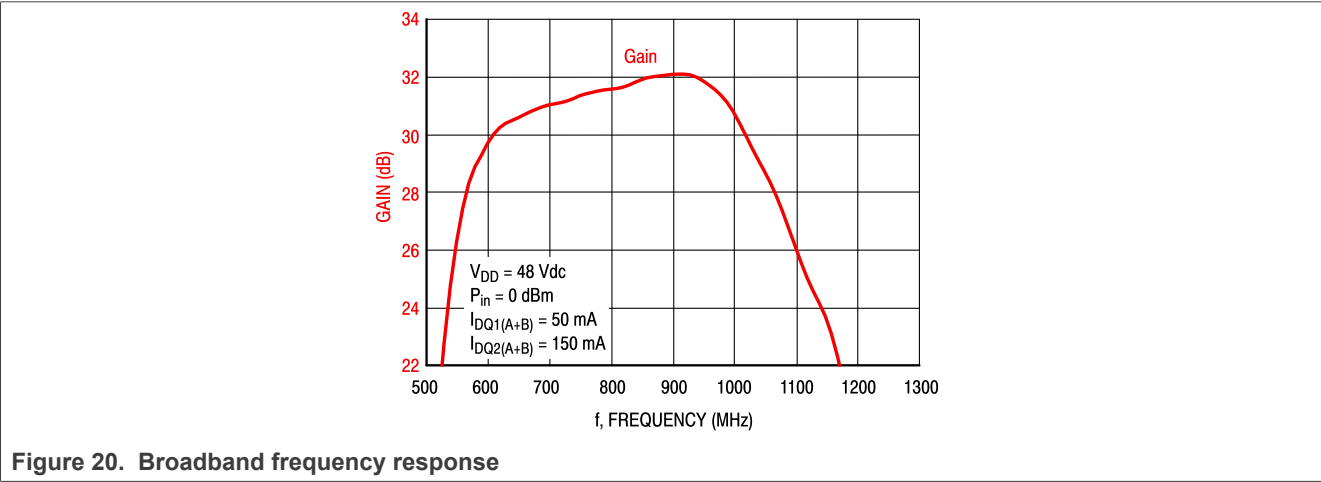


Figure 20. Broadband frequency response

Table 15. Load pull performance — Maximum power tuning — P1dB $V_{DD} = 48 \text{ Vdc}$, $I_{DQ1} = 23 \text{ mA}$, $I_{DQ2} = 77 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{[1]}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	$42.7 + j26.4$	$43.7 - j27.6$	$25.9 + j7.81$	29.6	43.2	21	61.4	-6
748	$36.3 + j26.3$	$42.0 - j25.0$	$24.9 + j9.30$	29.8	43.2	21	61.7	-5
768	$39.0 + j25.5$	$39.7 - j22.1$	$25.8 + j9.51$	30.1	43.4	22	62.1	-4

[1] Load impedance for optimum P1dB power.

Table 16. Load pull performance — Maximum power tuning — P3dB $V_{DD} = 48 \text{ Vdc}$, $I_{DQ1} = 23 \text{ mA}$, $I_{DQ2} = 77 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{[1]}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	$42.7 + j26.4$	$43.0 - j27.1$	$25.4 + j7.31$	27.5	44.0	25	63.7	-6
748	$36.3 + j26.3$	$41.5 - j24.6$	$24.6 + j8.58$	27.7	44.0	25	64.0	-5
768	$39.0 + j25.5$	$39.2 - j21.6$	$24.9 + j9.05$	27.9	44.1	26	64.3	-5

[1] Load impedance for optimum P3dB power.

Table 17. Load pull performance — Maximum efficiency tuning — P1dB $V_{DD} = 48 \text{ Vdc}$, $I_{DQ1} = 23 \text{ mA}$, $I_{DQ2} = 77 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{[1]}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	$42.7 + j26.4$	$42.1 - j26.9$	$32.6 + j31.6$	31.8	41.2	13	69.9	-7
748	$36.3 + j26.3$	$40.8 - j24.3$	$29.1 + j25.5$	31.6	42.0	16	70.6	-6
768	$39.0 + j25.5$	$38.3 - j21.1$	$29.1 + j27.5$	32.0	42.0	16	71.0	-5

[1] Load impedance for optimum P1dB power.

Table 18. Load pull performance — Maximum efficiency tuning — P3dB
 $V_{DD} = 48\text{ Vdc}$, $I_{DQ1} = 23\text{ mA}$, $I_{DQ2} = 77\text{ mA}$, Pulsed CW, 10 $\mu\text{sec(on)}$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{[1]}$ (Ω)	Gain (dB)	(dBm)	(W)	ηD (%)	AM/PM ($^{\circ}$)
728	$42.7 + j26.4$	$42.4 - j26.7$	$33.6 + j22.2$	29.1	42.9	20	71.4	-6
748	$36.3 + j26.3$	$40.8 - j23.9$	$29.9 + j23.7$	29.5	42.9	20	72.4	-5
768	$39.0 + j25.5$	$38.4 - j20.8$	$28.8 + j26.3$	29.9	42.8	19	72.4	-5

[1] Load impedance for optimum P3dB power.

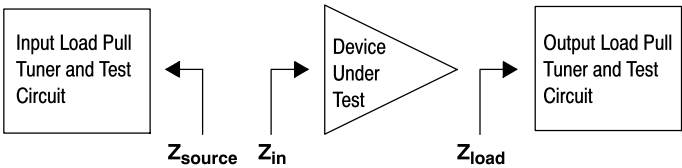
Notes:

Measurement made on a per side basis

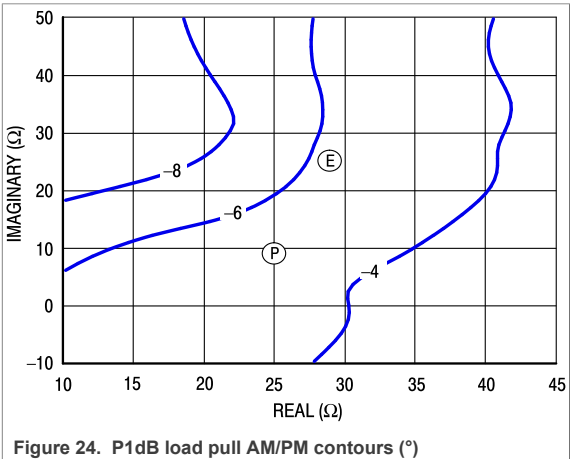
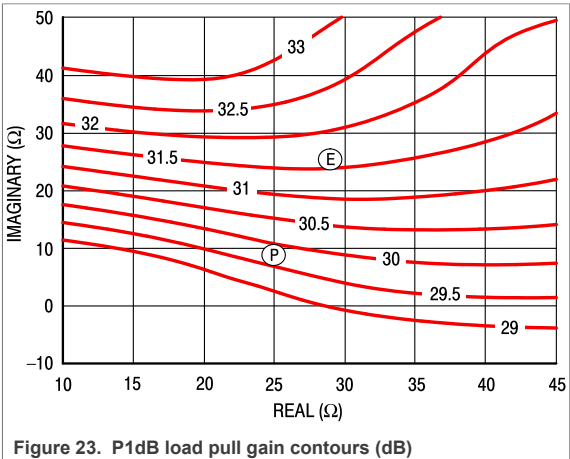
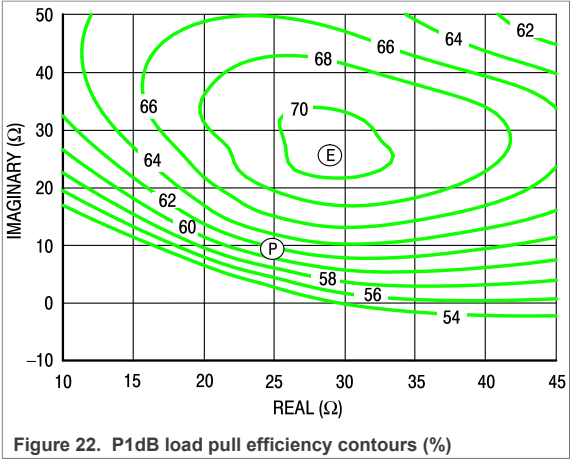
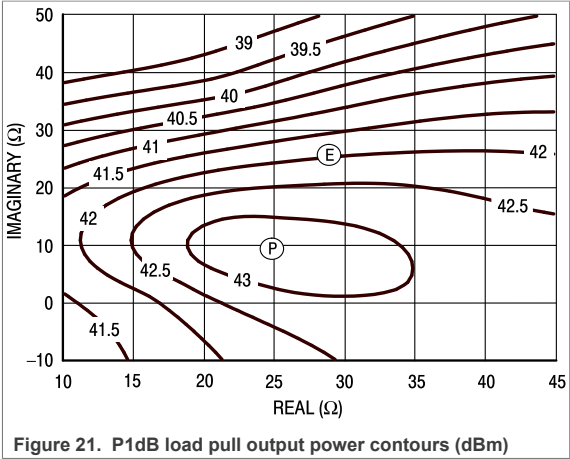
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



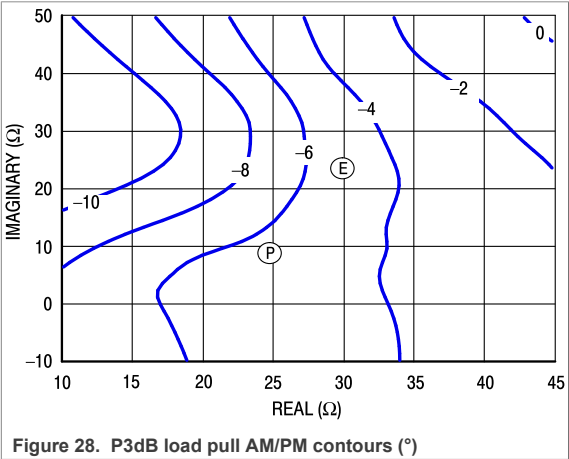
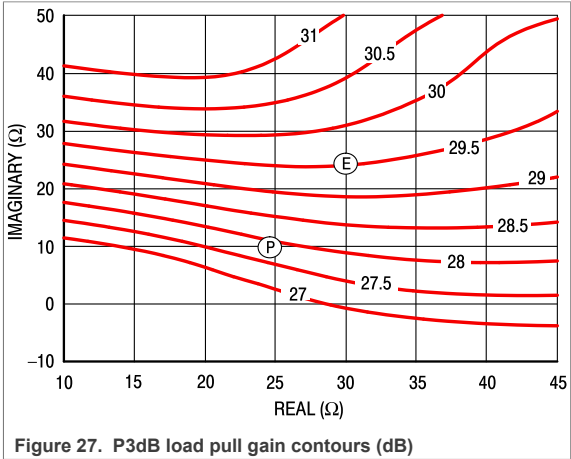
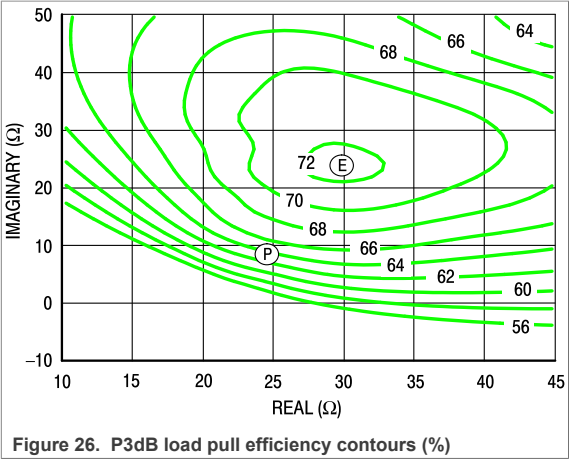
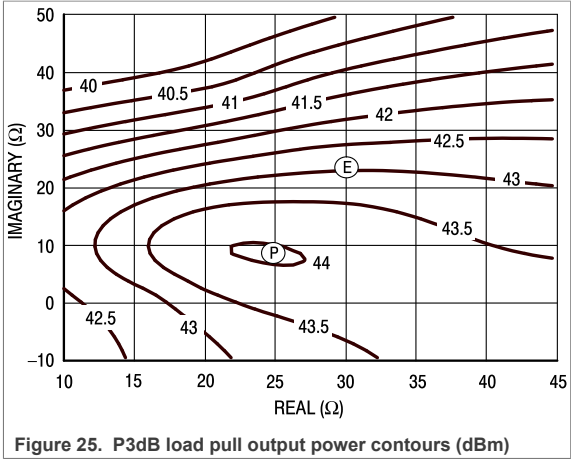
18 P1dB – Typical load pull contours — 748 MHz



NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

19 P3dB – Typical load pull contours — 748 MHz



NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

20 Package outline

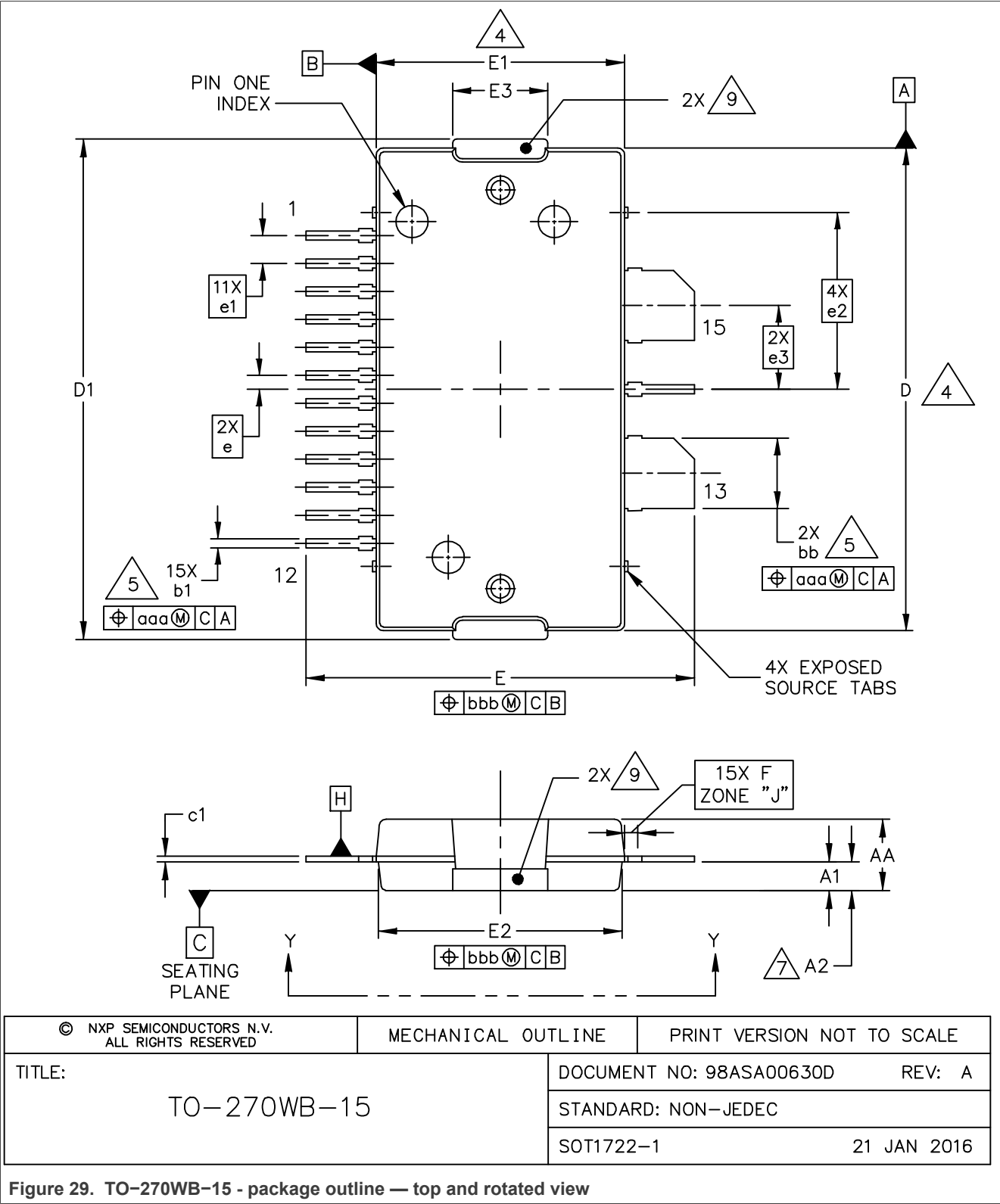
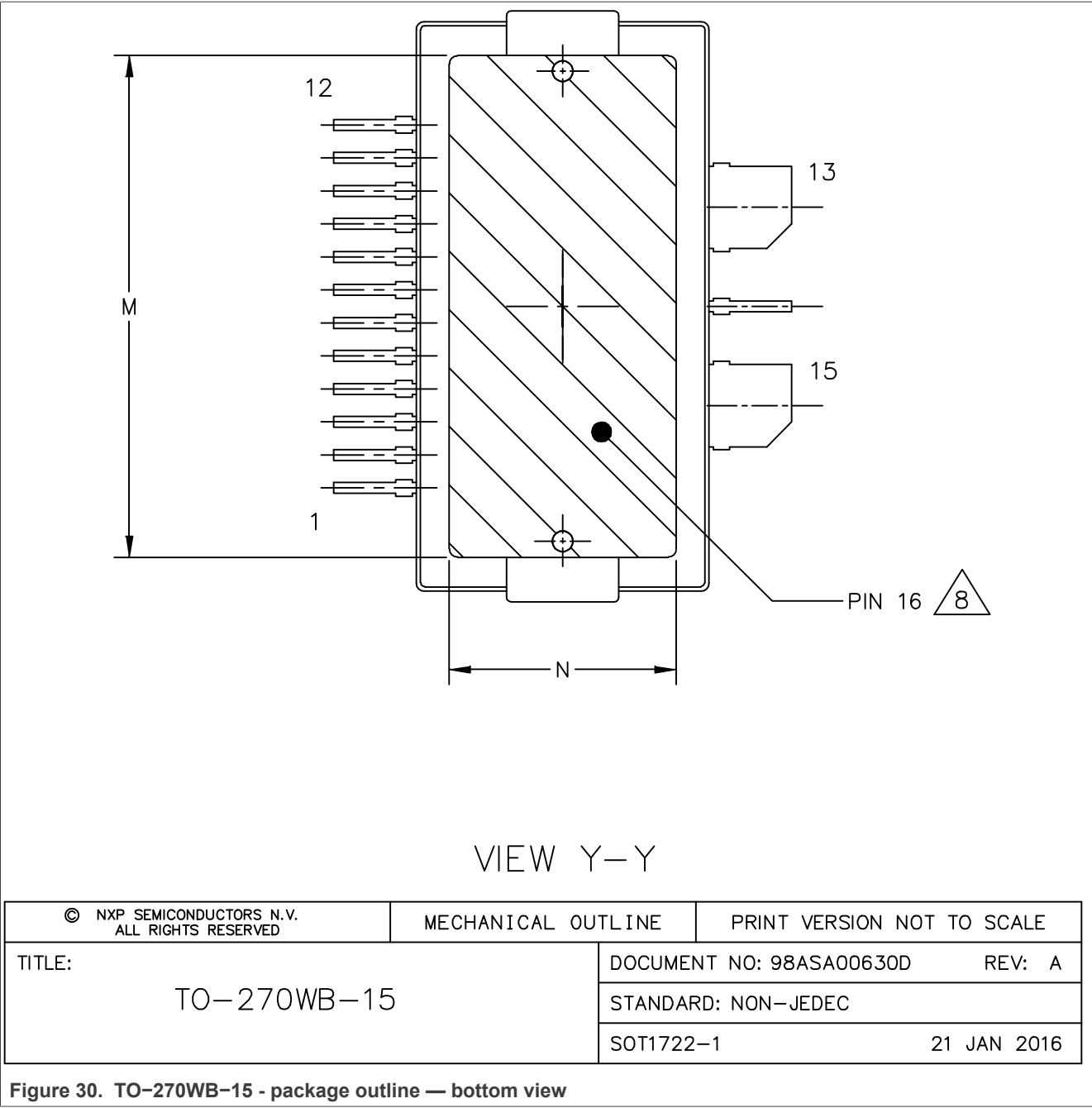


Figure 29. TO-270WB-15 - package outline — top and rotated view

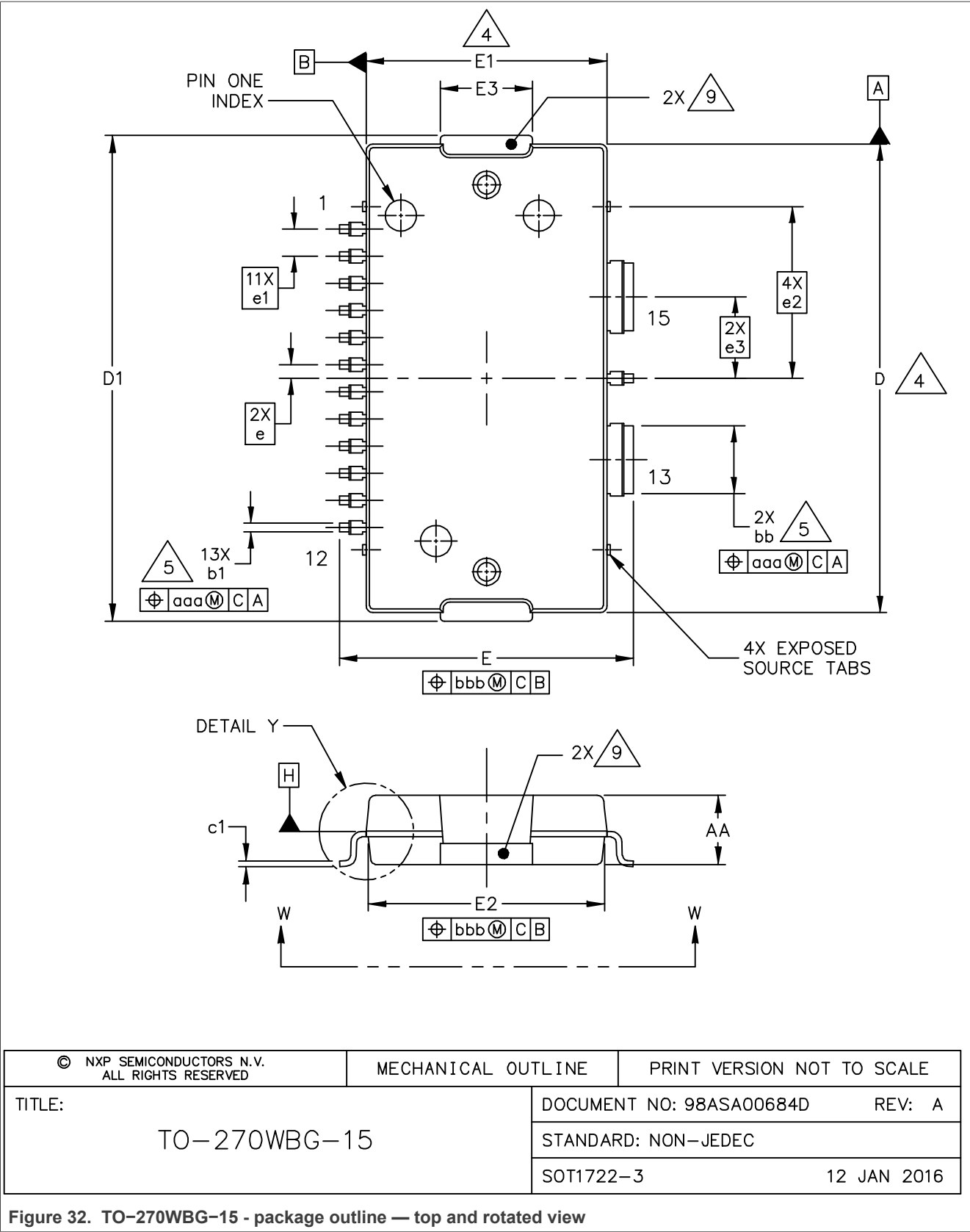


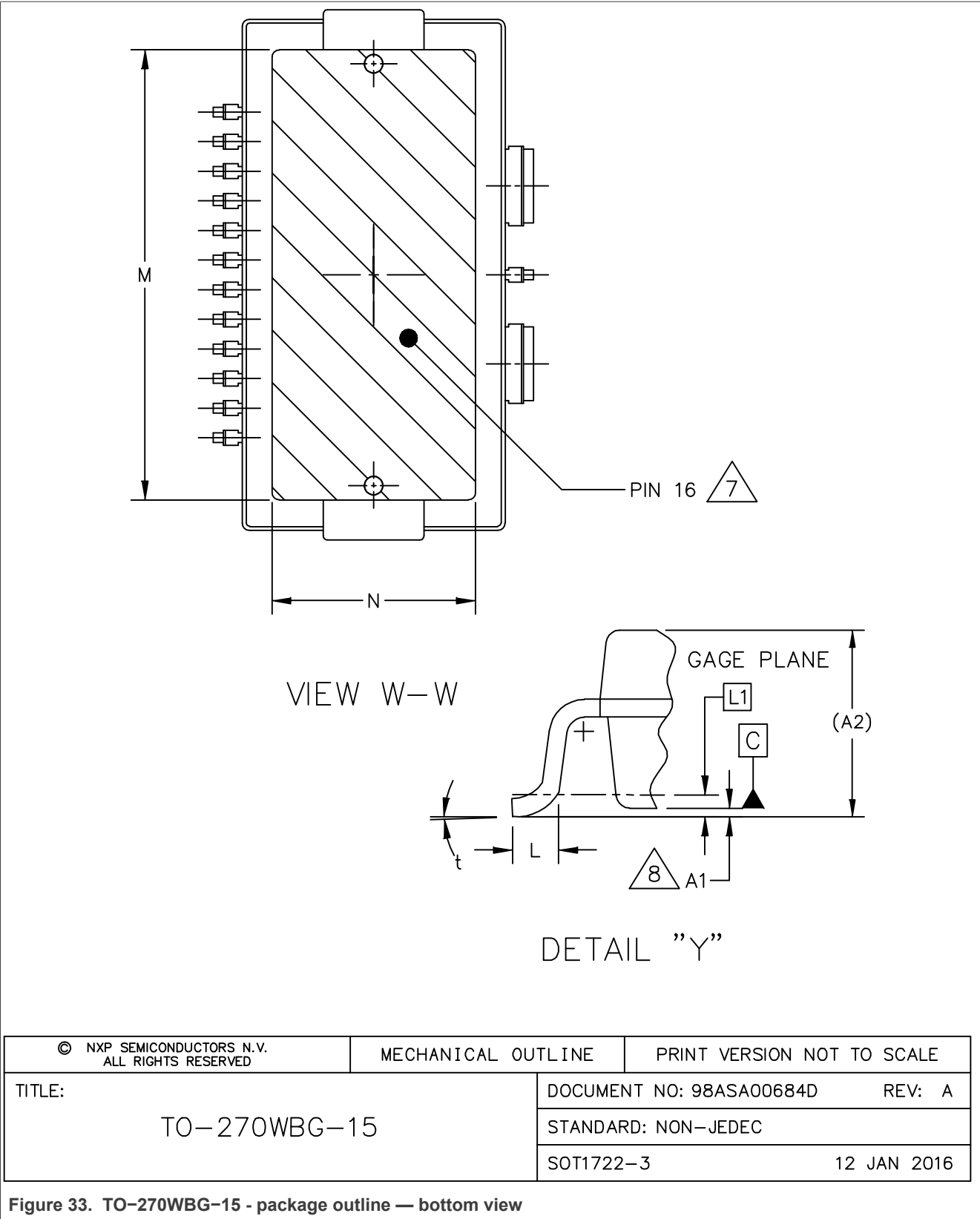
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.
8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.
9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

INCH			MILLIMETER		INCH			MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	M	.600	----	15.24	----
A1	.039	.043	0.99	1.09	N	.270	----	6.86	----
A2	.040	.042	1.02	1.07	bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	c1	.007	.011	0.18	0.28
E	.551	.559	14.00	14.20	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	e3	.120 BSC		3.05 BSC	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
					bbb	.008		0.20	
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TITLE: TO–270WB–15					DOCUMENT NO: 98ASA00630D REV: A				
					STANDARD: NON–JEDEC				
					SOT1722–1				

Figure 31. TO–270WB–15 - package outline — notes





NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

INCH			MILLIMETER		INCH			MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	M	.600	----	15.24	----
A1	.001	.004	0.03	0.10	N	.270	----	6.86	----
A2	(.105)		(2.67)		bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	c1	.007	.011	0.18	0.28
E	.429	.437	10.90	11.10	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	e3	.120 BSC		3.05 BSC	
L	.018	.024	0.46	0.61	t	2"	8"	2"	8"
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
					bbb	.008		0.20	
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TITLE: TO-270WBG-15					DOCUMENT NO: 98ASA00684D REV: A				
					STANDARD: NON-JEDEC				
					SOT1722-3				

Figure 34. TO-270WBG-15 - package outline — notes

21 References

Refer to the following resources to aid your design process.

Application notes

- [AN1907, Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages](#)
- [AN1955, Thermal Measurement Methodology of RF Power Amplifiers](#)
- [AN1977, Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family](#)
- [AN1987, Quiescent Current Control for the RF Integrated Circuit Device Family](#)

Engineering bulletins

- EB212, Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTF Calculator
- RF High Power Model
- .s2p File

Development tools

- Printed Circuit Boards

22 Revision history

The following table summarizes revisions to this document.

Table 19. Revision history

Document ID	Release date	Description
A2I09VD030N_030GN v.3.0	24 September 2026	• Updated data sheet to our latest template and legal information • Updated "Power gain" and "Adjacent channel power ratio" Max values in Table 8
A2I09VD030N_030GN v.2.0	October 2022	• Updated frequency band of operation for this device to 575 MHz –1300 MHz
A2I09VD030N_030GN v.1.0	March 2017	• Functional test table: added Output Peak-to-Average Ratio measurement to the functional test table
A2I09VD030N_030GN v.0.0	December 2016	• Initial release of data sheet

Legal information

Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

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