Using the CodeTEST Probe with Freescale™ MCF5272 Processor

This document describes the requirements for connecting the CodeTEST Probe to the external bus interface of the MCF5272 processor.

Purpose

This document supplements the *Setup and Installation Guide for the CodeTEST Probe*, which provides generic information on setting up, connecting, and configuring the CodeTEST Probe, and describes CodeTEST address and data port requirements, and bus and timing requirements.

Use the information in this document to make the physical connection between the CodeTEST Probe and the external bus interface of the MCF5272 processor and to configure the Probe with the CodeTEST Manager.

Hardware Connections

The CodeTEST Probe supports 16- and 32-bit port sizes. You will need to identify data and address tag ports to be used for data transfers to the CodeTEST Probe. The connection can use a dedicated or non-dedicated chip select.

External bus interface with Dedicated Chip Select

The following connections are required:

Probe	Processor	Notes
A31:4	NC	Not required when using dedicated chip select.
A3:1	A3:1	
D31:0	D31:0	
X15:0	NC	
C0	VCC	VCC – Not necessary.
C1	SDCLK	CLK
C2	NC	DS
C3	R/W*	AS - Connect chip select controlling CodeTEST ports.
C4	NC	RST2
C5	NC	RST1
C6	CSn*	CYC - Connect chip select controlling CodeTEST ports. See Note.

CodeTEST Development Team

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Probe	Processor	Notes
C7	NC	WS

Note: The chip select that controls the region containing the CodeTEST ports is connected to the bus arbitration signal (CYC) and the R/W* is used as the address strobe (AS) because the R/W* signal is not asserted for the duration of the chip select. The R/W* signal is used to latch valid address and data and the chip select is used to further qualify the access to a particular region.

External bus interface with Non-Dedicated Chip Select

The following connections are required:

Probe	Processor	Notes
A31:23	NC	Address bits not available externally.
A22:0	A22:0	
D31:0	D31:0	
X15:0	NC	
C0	VCC	VCC – Not necessary.
C1	SDCLK	CLK
C2	NC	DS
C3	R/W*	AS
C4	NC	RST2
C5	NC	RST1
C6	CSn*	CYC - Connect chip select controlling CodeTEST ports.
C7	NC	WS

Probe Configuration

This section identifies the settings you should use in the **Probe Config Utility** in the CodeTEST Manager when you configure the Probe.

External bus interface with Dedicated Chip Select

Use the Universal Probe type and select the following settings:

Field	Setting	Notes
Port Address	0x0	
Port Address Mask	0xFFFFFFFF	Ignore address bus.
Extended Bus	0x0	
Extended Bus Mask	0xFFFF	
Bus Type	Non-Multiplexed	

Port Size		Select appropriately for target hardware.
Reset Configuration	Neither	
Strobe Configuration	1 Strobe	
Address Strobe Polarity	Low	
Write Strobe Polarity	Disabled	
Bus Arbitration Polarity	Low	
Endianess		Set appropriately for target hardware.
Word Swap	No	
Frequency Range		Set to the frequency of SDCLK.
Phase Shift		Adjust as necessary to obtain accurate data.
Invert Clock	No	
Router Image		Select appropriate router image.

External bus interface with Non-Dedicated Chip Select

Use the Universal Probe type and select the following settings:

Field	Setting	Notes
Port Address		Enter address of the Probe tag port.
Port Address Mask	0xFF800000	Ignore A31:23 of address bus.
Extended Bus	0x0000	
Extended Bus Mask	0xFFFF	
Bus Type	Non-Multiplexed	
Port Size		Select appropriately for target hardware.
Reset Configuration	Neither	
Strobe Configuration	1 Strobe	
Address strobe Polarity	Low	
Write Strobe Polarity	Disabled	
Bus Arbitration Polarity	Low	
Endianess		Set appropriately for target hardware.
Word Swap	No	
Frequency Range		Set to the frequency of SDCLK.
Phase Shift		Adjust as necessary to obtain accurate data.
Invert Clock	No	
Router Image		Select appropriate router image.

Limitations

Processors with bus frequencies over 100 MHz must have at least 2 clock cycles per bus cycle.

The Probe does not support the following memory activities:

- Pipelined accesses: Multiple or overlapping address cycles in relation to the data portion of a bus cycle.
- Burst accesses: The tag ports must be located in a non-burst memory region.
- Misaligned accesses: The tag ports must be on 64-bit aligned memory locations.
- Cache: The tag ports must be located in non-cached or cached write-through memory.
- DRAM: The tag ports cannot be located in DRAM on processors with built-in DRAM controllers.
- 8-bit ports: 8-bit ports are not correctly reconstructed into 32-bit tags.