NXP Semiconductors
Application Note

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Parallel mode

for the dual SOIC 24 V high-side switch family

1 Introduction

This application note describes parallel mode operations and sensing configurations for the following devices:

- MC06XS4200
- MC10XS4200
- MC20XS4200
- MC22XS4200
- MC50XS4200

These intelligent high-side switches are designed for use in 24 V systems such as trucks, busses, and special engines. They are applicable to other industrial and 12 V applications as well. The low $R_{DS(on)}$ channels can be used to control incandescent lamps, LEDs, solenoids, or DC motors. Control, device configuration, and diagnostics are performed through a 16-bit SPI interface, allowing easy integration into existing applications. For complete feature descriptions, refer to the individual data sheets for the devices.

NXP analog ICs are manufactured using the SMARTMOS process, a combinational BiCMOS manufacturing flow that integrates precision analog, power functions and dense CMOS logic together on a single cost-effective die.

Contents

2 Parallel mode description

For the devices listed above, parallel mode provides a means of increasing output current beyond the capabilities of a single channel. In parallel mode, current may be driven up to twice the maximum capability of a single channel. Output current is equally distributed between the two channels.

Features

- 2x max. current of a single channel
- Direct input control or SPI control with output synchronization
- Open load ON, open load OFF and short to battery diagnostics, each channel reports its own diagnostics in FAULT_x registers
- Current sensing up to overcurrent low threshold (OCLx)

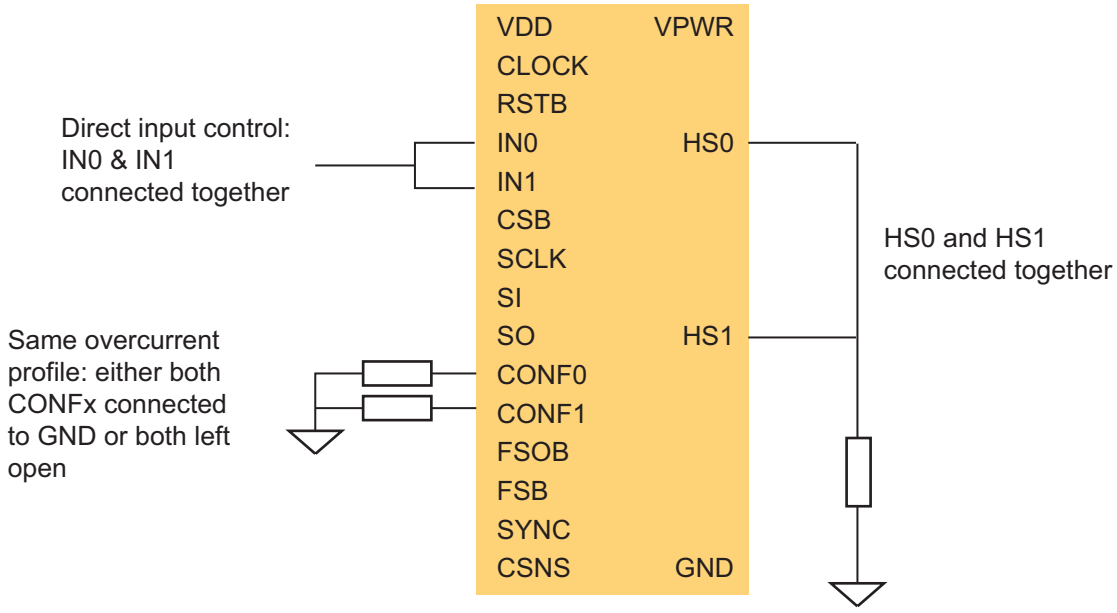
In parallel mode, all active protections apply to both channels. Any activation on one channel turns off both channels:

- Overcurrent detection based on Channel 0 configuration
- Severe short-circuit
- Overtemperature
- Auto retry capability based on Channel 0 configuration

2.1 Pin configuration for parallel mode

The pin configuration for parallel mode is as follows:

- For direct input control: IN0 and IN1 connected together
- CONF0 & CONF1 have same configuration either Motor or Bulb
- HS0 and HS1 are connected together



Note: only pins that require specific connections for parallel operation are represented here

Figure 1. Pin configuration for parallel mode

3 Output parallel mode configuration

Bit PARALLEL of register GCR has to be set to 1 to enable the parallel mode.

The switching configuration is defined by Channel 0 only. All contents on Channel 1 configuration is replaced by contents from Channel 0. Only channel diagnostics remain independent. The enabling / disabling of each diagnostics is set separately for each channel (Bit D8, D7, and D6 of CONFR_x register).

SI Register	SI Data															
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GCR	WDIN	P	0	1	1	0	0	PWM_en_1	PWM_en_0	PARALLEL	T_H_en	WD_dis	$V_{DD\_FAIL\_en}$	CSNS1_en	CSNS0_en	OV_dis

to enable PWM

set to 1

Figure 2. Parallel mode register settings

4 Current sense in parallel mode

Be aware that, in parallel mode, the current sense output might reflect either the sum of both channels' current or the current from one channel only. The low level overcurrent threshold depends on the current sense method used.

4.1 Current sense: sum of HS0 and HS1 currents

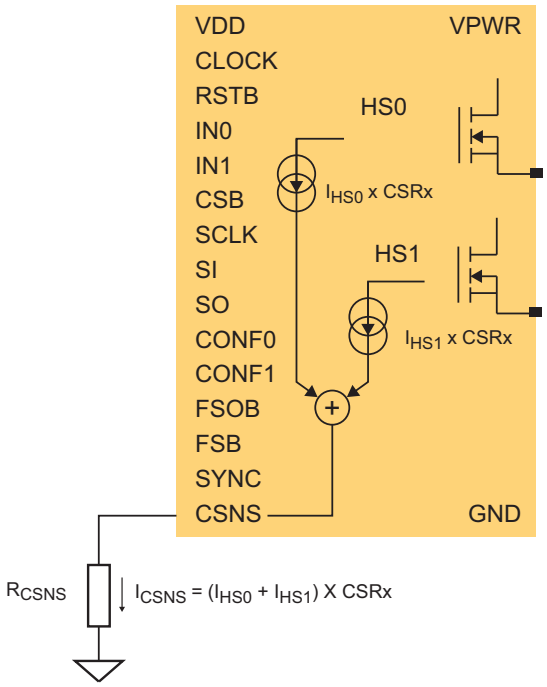


Figure 3. Current sense: sum of the channels

Current sense in parallel mode

Figure 4 illustrates the configuration causing the CSNS pin to reflect the sum of the currents from both the HS0 and HS1 channels.

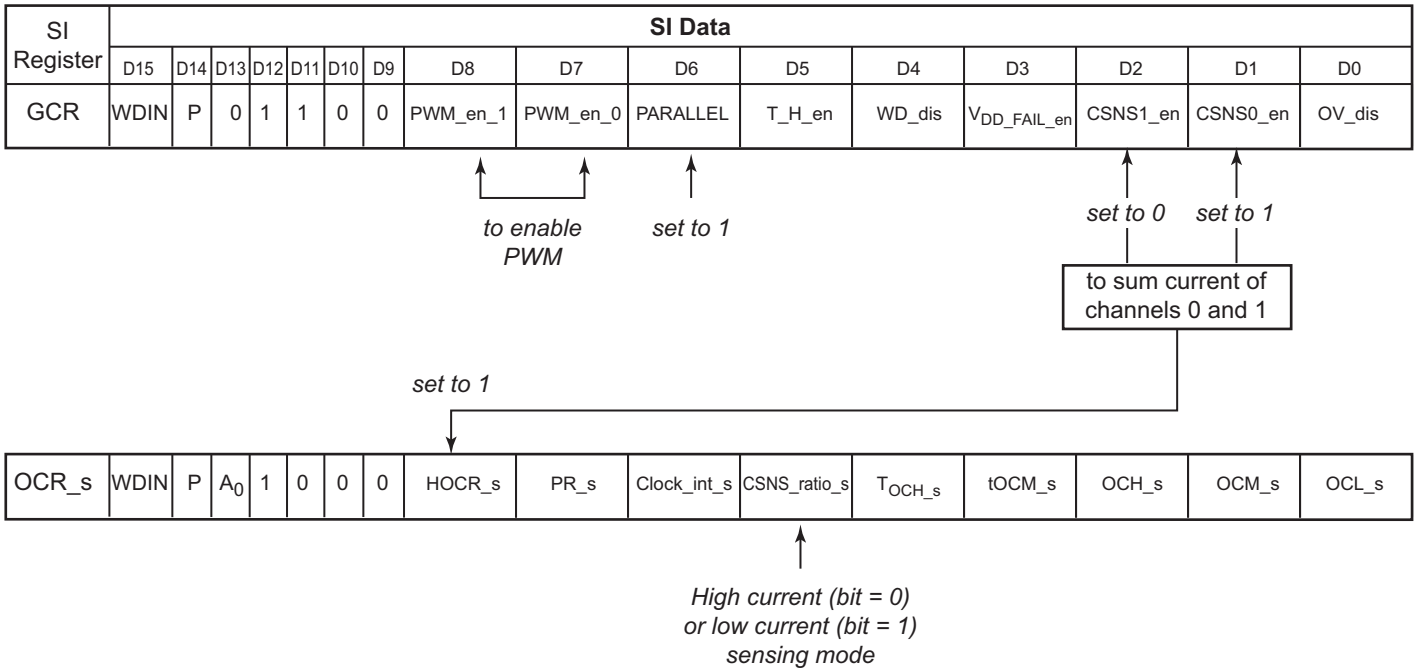


Figure 4. SPI settings for configuration for current sense sum

NOTE

When selecting bit HOCR = 1 (bit D8 of OCR_s register) to sum two HSx currents, the level overcurrent threshold is subsequently selected to either IOCL2 or IOCL3.

D8	D6	D2	D1	Activated function as CSNS pin
x	x	0	0	Disabled
0	x	0	1	Current sensing on Channel 0
0	x	1	0	Current sensing on Channel 1
0	x	1	1	Temperature sensing
1	0	0	1	Current sensing on Channel 0
1	x	1	1	Temperature
1	1	0	1	Current sensing summed currents of channels 0 and 1

HOCR (D8)	OCL_s (bit D0)	Selected OCL Current Level
0	0	$I_{\_OCL1\_x}$ (default)
0	1	$I_{\_OCL1\_x}$
1	0	$I_{\_OCL2\_x}$
1	1	$I_{\_OCL3\_x}$

Example

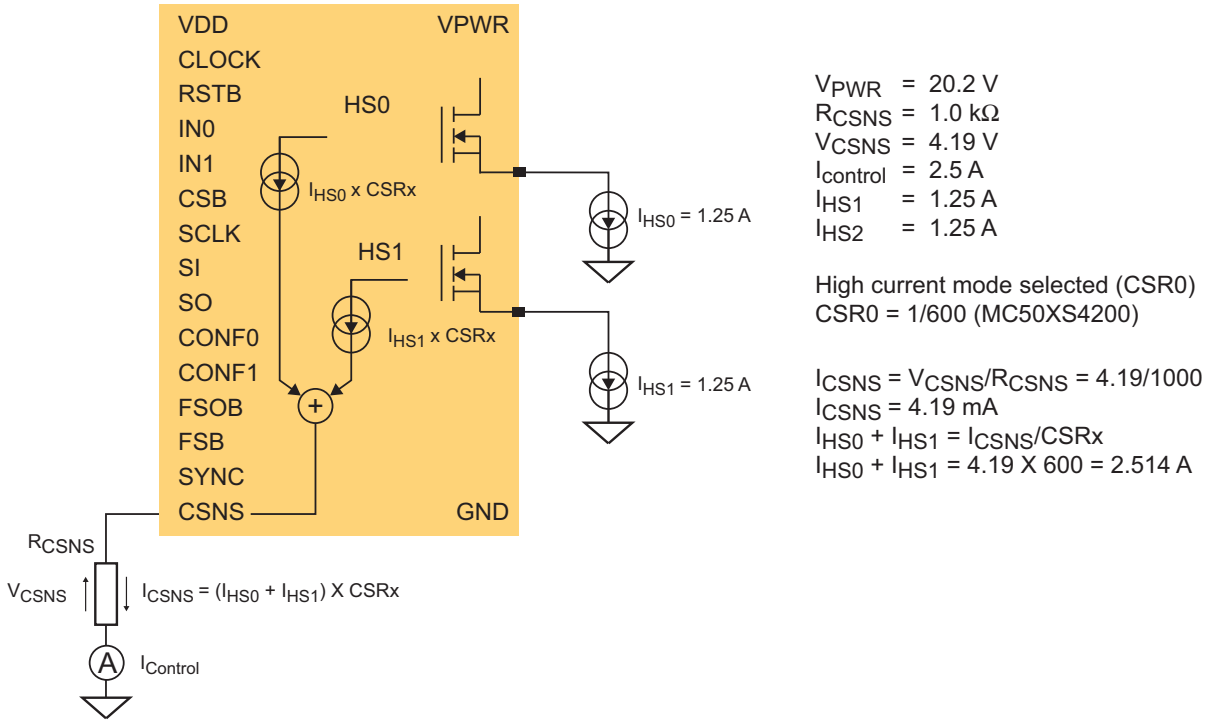


Figure 5. Example of current sum

4.2 Current sense: one channel only

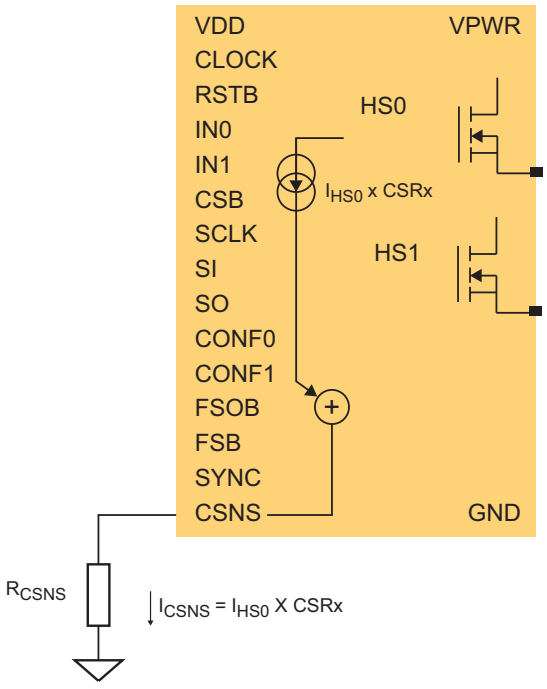


Figure 6. Current sense on one channel

Current sense in parallel mode

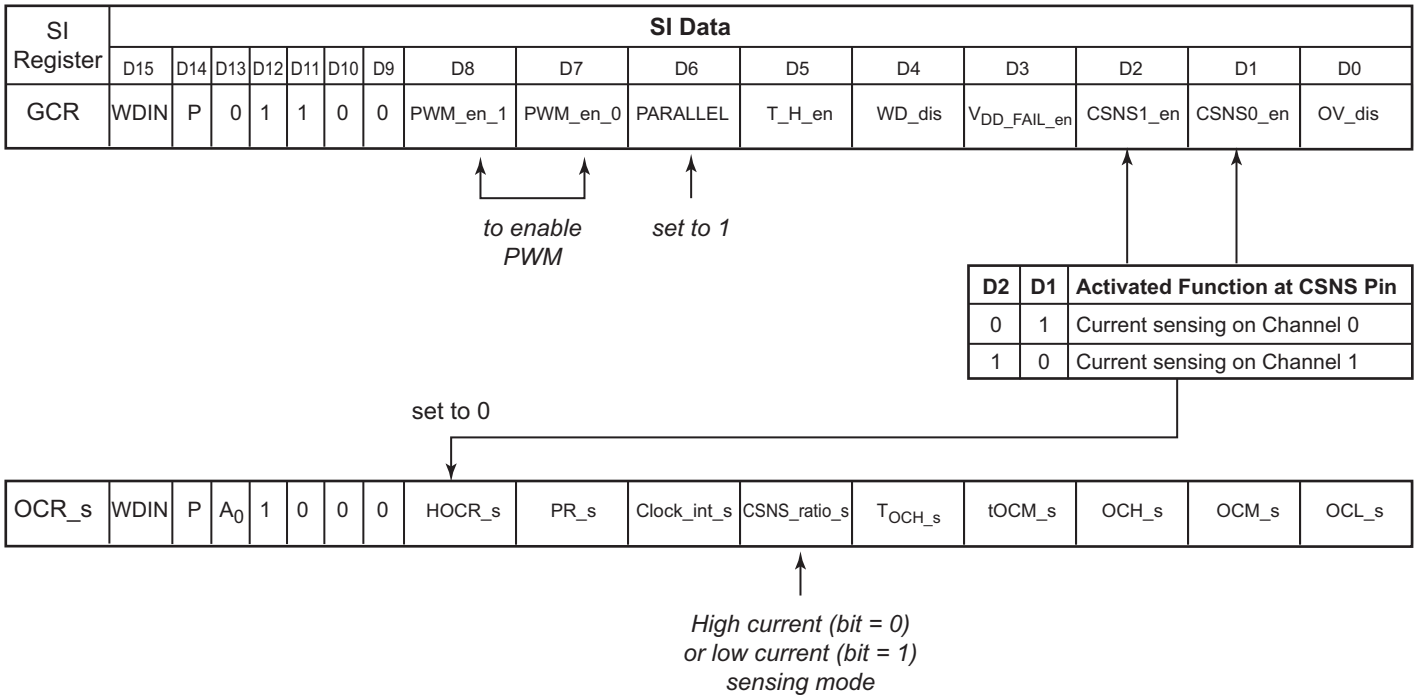


Figure 7. SPI settings for current sensing on one channel

When selecting bit HOCR = 0, current sensing is either on Channel 0 or on Channel (HOCR bit is set to 1 to sum currents) 1. The low-level overcurrent threshold is selected to IOCL1.

D8	D6	D2	D1	Activated function as CSNS pin
x	x	0	0	Disabled
0	x	0	1	Current sensing on Channel 0
0	x	1	0	Current sensing on Channel 1
0	x	1	1	Temperature sensing
1	0	0	1	Current sensing on Channel 0
1	x	1	1	Temperature
1	1	0	1	Current sensing summed currents of channels 0 and 1

HDCR (D8)	OCL_s (bit D0)	Selected OCL Current Level
0	0	$I_{\_OCL1\_x}$ (default)
0	1	$I_{\_OCL1\_x}$
1	0	$I_{\_OCL2\_x}$
1	1	$I_{\_OCL3\_x}$

5 Revision history

Revision	Date	Description
1.0	5/2015	• Initial release
	7/2016	• Updated to NXP document form and style

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