

Understanding SYSCLK Jitter

This application note describes basic jitter terminology and the aspects pertaining to the SYSCLK clock design requirements, when designing with the PowerQUICC™ III processors.

1 Introduction to Jitter

Jitter is a time deviation of a signal transition from its ideal position in time. It can be caused by many different factors, including PLL loop noise, thermal noise, cross talk, power supply ripple. It can be characterized by using multiple terminology.

The jitters—cycle-to-cycle (short-term jitter), and period (long-term jitter)—are the most common and familiar specifications.

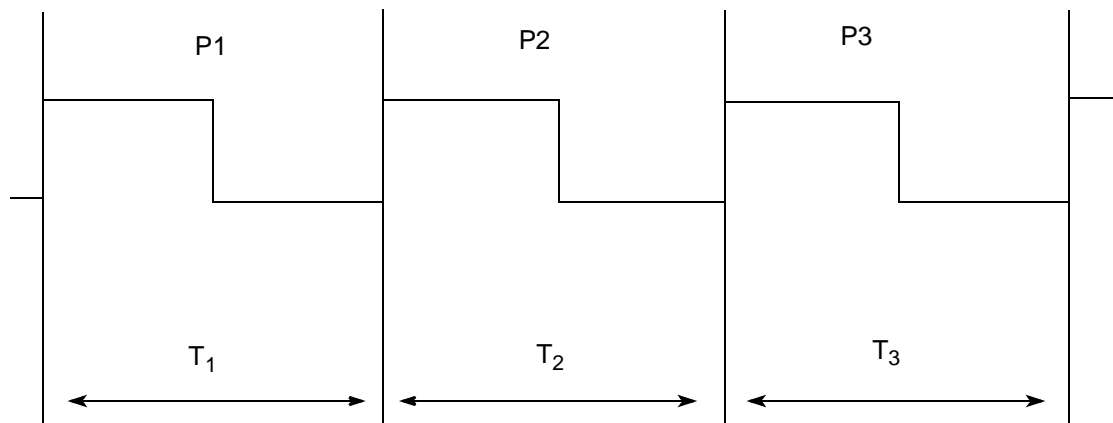
This application note provides a brief overview of basic terminology and is not intended to provide a comprehensive overview of jitter.

Contents

1. Introduction to Jitter	1
1.1. Cycle-to-Cycle Jitter	2
1.2. Period Jitter	3
1.3. Time Interval Error Jitter	3
1.4. Random Versus Deterministic Jitter	4
2. SYSCLK Specification on PowerQUICC III Processors	6
3. Phase Jitter on PowerQUICC III Processors	7
4. References	8
5. Revision History	8

1.1 Cycle-to-Cycle Jitter

Cycle-to-cycle jitter is defined as the maximum difference between any two adjacent clock periods. It is always specified as an absolute magnitude and not by positive or negative value. [Figure 1](#) shows the cycle-to-cycle jitter.

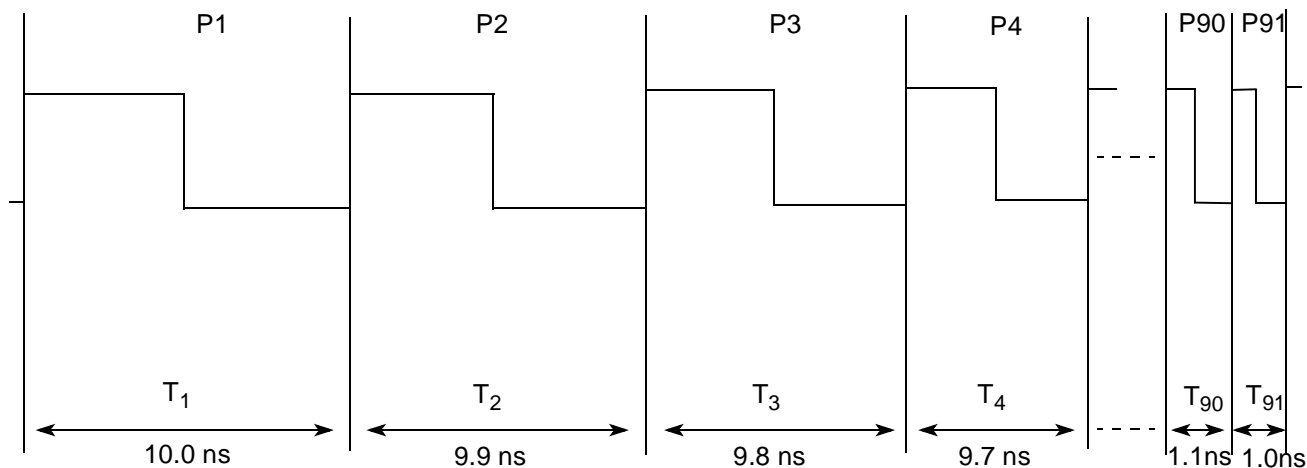


$$|T_2 - T_1| = 100 \text{ ps}, |T_3 - T_2| = 100 \text{ ps}, \dots, |T_n - T_{(n-1)}| = 100 \text{ ps}$$

Figure 1. Cycle-to-Cycle Jitter

Cycle-to-cycle jitter is important for specifying the performance of PLL however, it does not establish a relationship between non-adjacent clocks. Specifically, it does not address frequency drift over time.

For example, the clock shown in [Figure 2](#) meets 100 ps of cycle-to-cycle jitter specifications. However, over the time, frequency of the clock has drifted significantly.



$$|T_2 - T_1| = 100 \text{ ps}, |T_3 - T_2| = 100 \text{ ps}, |T_n - T_{(n-1)}| = 100 \text{ ps} \dots$$

Figure 2. Cycle-to-Cycle Jitter with Frequency Drift

1.2 Period Jitter

Period jitter is defined as the maximum deviation of any clock **period** from its mean clock **period**. It compares the length of each period to the average period of an ideal clock at a long-term average frequency of the signal.

Period jitter is typically specified over a set number of clock cycles. Jedec Specification, JESD65B, suggests, measuring jitter over 10,000 cycles when the clock is in a range of 10 to 100 MHz. However, if clock cycles are not specified, it is recommended to measure period jitter over 100,000 cycles to better represent jitter over an “infinite” time span.

For example, the clock shown in Figure 3 can be specified as a comparison of n periods to the ideal period. In practice, it is difficult to quantify an ideal period, thus average period is used. Therefore, compare n periods to the reference “average period.”

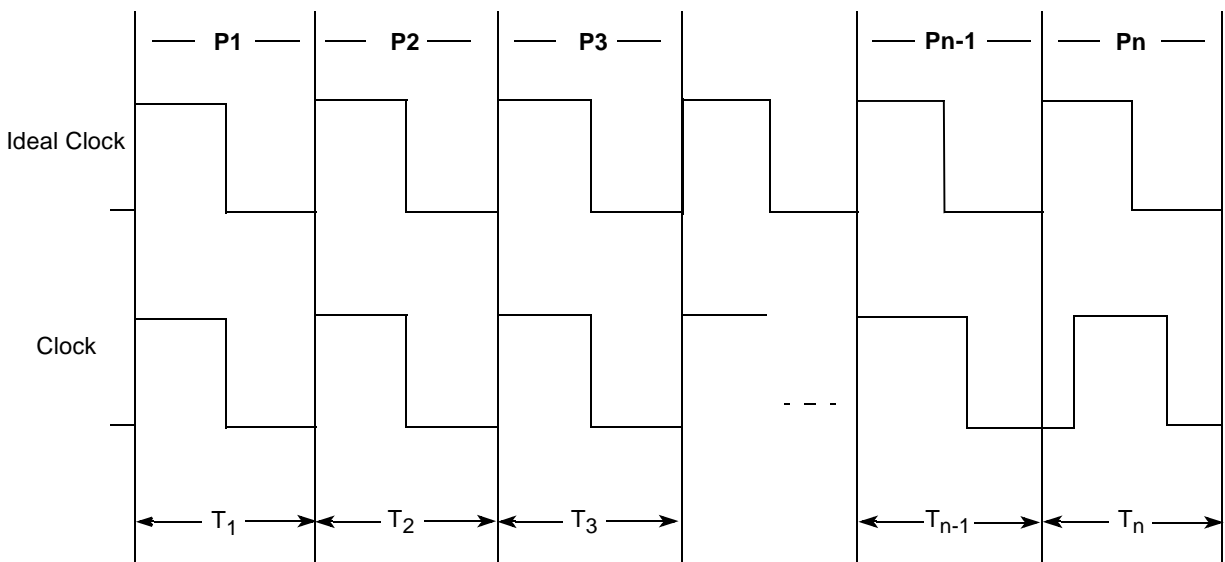


Figure 3. Period Jitter

This describes jitter over time, and ensures that the clock does not drift.

1.3 Time Interval Error Jitter

Time Interval Error (TIE) is the difference between observed clock **edge** time and expected clock **edge** time for each clock edge present. It is measured by subtracting the actual clock edge from the ideal clock edge. It is important to note that TIE refers to clock edges, while period jitter refers to clock period.

Figure 4 shows an example of actual clock compared to an ideal clock and is derived per cycle jitter of an actual clock.

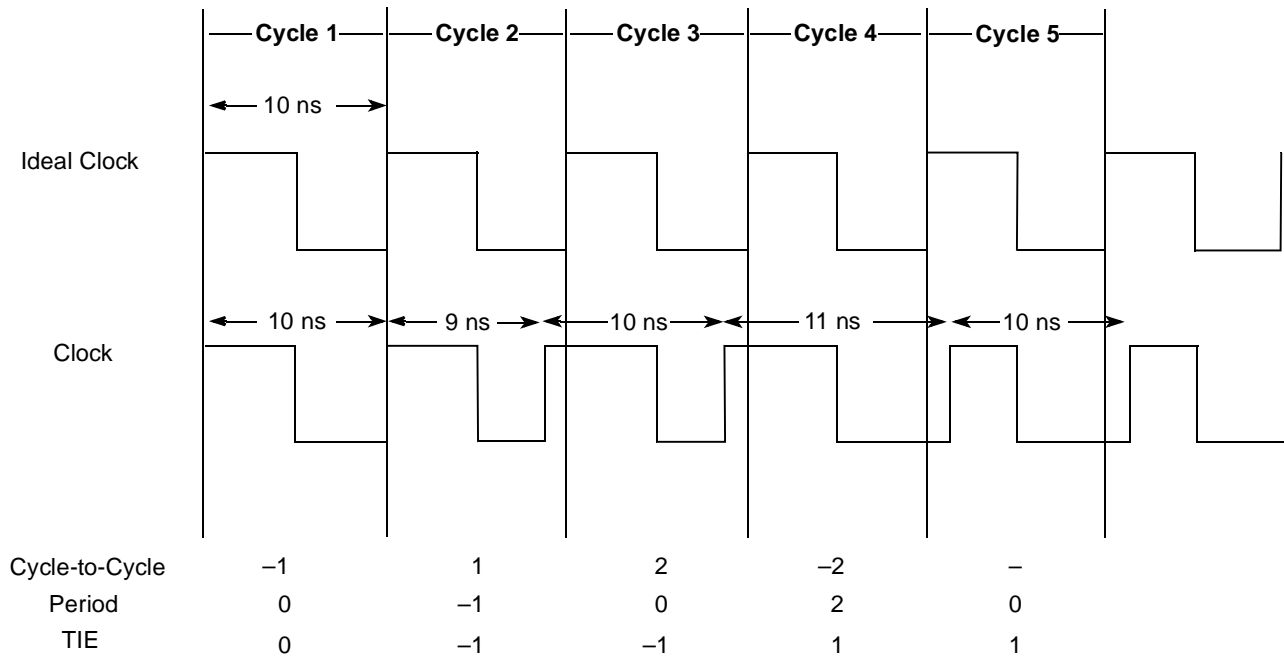


Figure 4. TIE as Related to Cycle-to-Cycle and Period Jitter

In Figure 4, the period of an ideal clock is assumed as 10 ns and jitter is always ± 1 ns deviated from an ideal clock. From first to second cycle, short-term (cycle-to-cycle) jitter is -1 ns. This equates to a period jitter of $T_m - 1$ ns (where T_m is the ideal or mean clock period).

From 2nd to 3rd cycle, short-term jitter is 1 ns (this is a measurement of change in two adjacent clock cycles of non-ideal clock). Rounding to the nearest ns, the equation for period jitter over the course of two cycles becomes $T_m - [(T_1 + T_2) / 2] = T_m - 1$. TIE compares the actual signal to ideal clock, and thus is equal to -1 for the 2nd cycle.

TIE is related to both cycle-to-cycle and period jitter. In fact, cycle-to-cycle jitter and period jitter can be calculated from TIE.

1.4 Random Versus Deterministic Jitter

Jitter (total jitter) is typically composed of a random jitter (RJ) component and a deterministic jitter (DJ) component. Deterministic jitter is caused by impedance mismatch, power supply ripple, crosstalk, ground bounce, intersymbol interference, ringing, and reference clock feed through. It is an artifact of board design and is typically controllable. DJ can be reduced by proper board design or IC selection.

The remaining components of jitter are random. Random jitter is caused by factors like thermal oscillations, thermal noise that result in levels of jitter and cannot be predicted on a cycle-by-cycle basis. It is not bounded. The longer you observe, wider the period variation appears; therefore, RJ is best described as a Gaussian distribution. The tails of a Gaussian distribution extends indefinitely on either side

of the mean. This implies that it is impossible to specify a peak-to-peak jitter range that bounds RJ 100% of the time. Instead, bound a range that contains the jitter for x percent of the time. Typically, long-haul optical systems specify jitter in terms of RMS over N cycles, or peak-to-peak cycle-to-cycle jitter over N cycles (N can be 200,000–300,000 cycles). SONET is specified at $14 \times$ RMS, which equates to 10^{-12} bit error rate (BER). Figure 5 shows the Gaussian distribution.

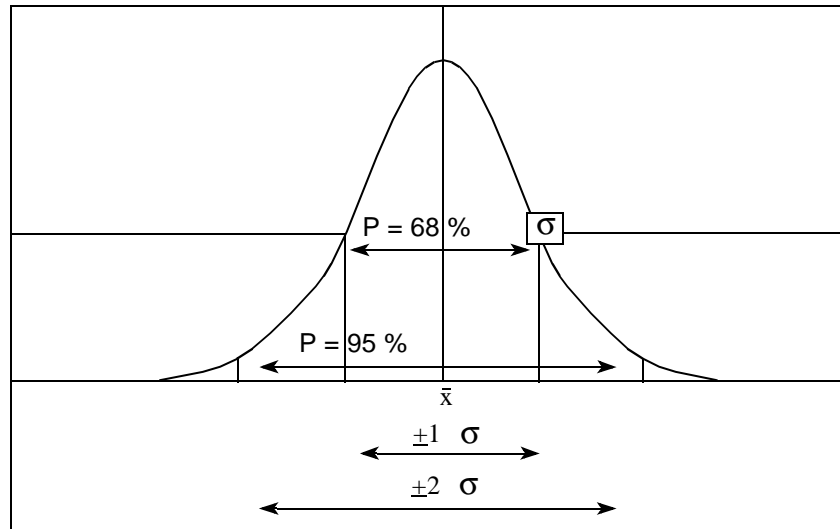


Figure 5. Gaussian Distribution

For example, one standard deviation is a point from the mean that contains 68.26% of all measurements (standard deviation is same as RMS).

Table 1 shows time to outlier clock for various standard deviation, considering a 100-MHz clock.

Table 1. Standard Deviation and BER for 100-MHz Clock

Standard Deviation (+/-)	% of Total Population	Time to Outlier for 100-MHz Clock	Bit Error Rate
1	68.2700000000000000%	32 ns	0.16
2	95.4500000000000000%	220 ns	2.28×10^{-2}
3	99.7300000000000000%	3.7 μ s	1.35×10^{-3}
4	99.9936660000000000%	157 μ s	0.32×10^{-4}
5	99.9999426700000000%	17 ms	2.87×10^{-7}
6	99.9999980270000000%	5.1 sec	0.98×10^{-9}
7	99.9999999974400000%	65 min	1.28×10^{-12}
8	99.9999999998760000%	~22 hours	0.62×10^{-15}

Total jitter (TJ) is the sum effect of RJ and DJ over a number of cycles. Since RJ is a Gaussian distribution, and there are no bounds, the calculation is not simply an addition of RJ and DJ. Total jitter can be specified as follows:

$$TJ = (\sigma \times RJ) + DJ \tag{Eqn. 1}$$

Figure 6 shows probability outside of peak-to-peak approximation.

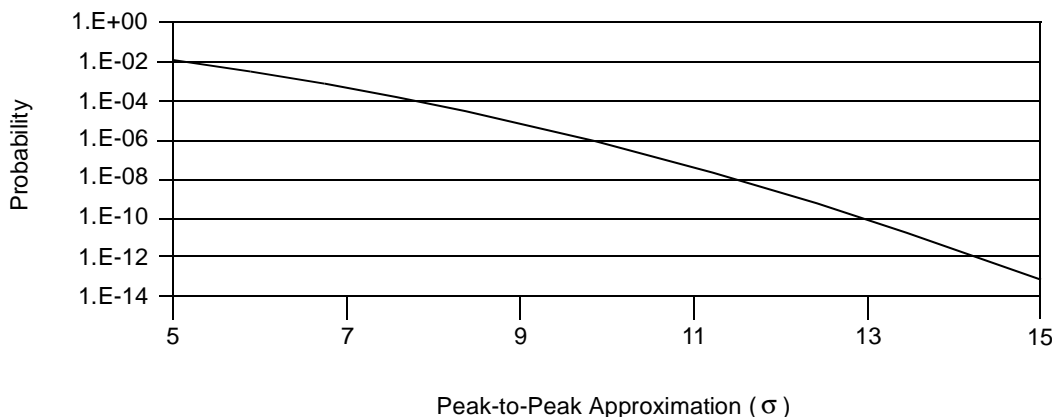


Figure 6. Probability Outside of Peak-to-Peak Approximation

In order to bound TIE over a number of cycles, statistically meaningful number of clock cycles are required (for example, 10^{12} or an approximation of it). Assuming that all RJ on a board is Gaussian, and there is a finite probability that any independent sample would be outside an approximated peak-to-peak value, a peak-to-peak total jitter can be extrapolated. Probability decreases as the number of standard deviations used to approximate the peak-to-peak value increases, and in the end, a total jitter calculation becomes a statistical calculation.

For this example of a BER equal to 10^{12} cycles, $TJ = (14.262 \times RJ) + DJ$. It is interesting to note that RJ plays a much more significant role in the total jitter than DJ; in this case 14.262 times more.

2 SYSCCLK Specification on PowerQUICC III Processors

For example, on MPC8548 microcontroller, SYSCCLK jitter is specified as 150 ps of total jitter. This is a TIE jitter specification, from which cycle-to-cycle and period jitter requirements can be calculated. It is recommended to measure TIE over at least 100,000 cycles and the thumb rule is to measure over 10^{12} cycles. However, as per Table 1, this measurement can take some time. On some oscilloscopes, it may be easier to measure TJ. TIE over n cycles is the equivalent measurement to TJ, as σ is proportional to the number of cycles.

Table 2 provides the system clock (SYSCLK) AC timing specifications.

Table 2. SYSCLK Timing Specifications

(At recommended operating conditions with OVDD = 3.3 V ± 165 mV.)

Parameter/Condition	Symbol	Min	Typical	Max.	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	16	—	133	MHz	1, 6
SYSCLK cycle time	t_{SYSCLK}	7.5	—	60	ns	6
SYSCLK rise and fall time	$t_{\text{KH}, \text{TKL}}$	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	$t_{\text{KHK}}/t_{\text{SYSCLK}}$	40	—	60	%	3
SYSCLK jitter	—	—	—	±150	ps	4, 5

Notes:

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies.
- Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short-term and long-term—and is guaranteed by design.
- The SYSCLK driver's closed loop jitter bandwidth should be <500 KHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- This parameter has been adjusted slower according to the workaround for device erratum GEN 13.

Since the SYSCLK input is not used for long-haul transmission of large data packets to a device running on a separate clock domain, a measurement like BER is not really applicable. SYSCLK impacts internal timing budgets, and the ability of internal PLL to track the clock. The PCB designer's main concern is to ensure that jitter on SYSCLK is such that it is outside the bandwidth in which the PowerQUICC III PLL can amplify it.

In Table 2, note 5 specifies the internal PLL's closed loop jitter. This specification further narrows down the jitter requirement for SYSCLK and specifies 500 kHz to 10 MHz as the range at which the gain curve of the internal PLL is positive and has a peak (this means jitter can be amplified). At lower frequencies, PLL tracks precisely and at higher frequencies PLL response is damped and jitter is attenuated. Therefore, spread spectrum clock inputs (~30 kHz) work as SYSCLK inputs.

3 Phase Jitter on PowerQUICC III Processors

Period jitter and phase jitter are often confused. Phase jitter, as specified on PowerQUICC III products, is a deviation in edge location with respect to mean edge location. Table 3 lists the AC requirements for the PCI Express SerDes clocks.

Table 3. SD_REF_CLK and SD_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	100	ps	—
t_{REFPJ}	Phase jitter, Deviation in edge location with respect to mean edge location.	-50	—	50	ps	—

References

So, phase jitter as specified is a TIE or TJ measurement over 100,000 cycles.

4 References

- http://www.lecroy.com/tm/Library/WhitePapers/PDF/WP_TechBrief_Dif_Ref_Jit.pdf
- <http://pdfserv.maxim-ic.com/arpdf/AppNotes/3hfan402.pdf>

5 Revision History

Table 4 provides a revision history for this application note.

Table 4. Document Revision History

Rev. Number	Date	Substantive Change(s)
1	02/19/2010	Updated Figure 3 in Section 1.2, "Period Jitter." Removed Equation from the Section 1.2, "Period Jitter." Revised Figure 4 in Section 1.3, "Time Interval Error Jitter." Added Equation 1 in Section 1.4, "Random Versus Deterministic Jitter" and updated content accordingly. Added Figure 6 Probability Outside of Peak-to-Peak Approximation Section 1.4, "Random Versus Deterministic Jitter." Updated Section 2, "SYSCLK Specification on PowerQUICC III Processors." Updated Section 3, "Phase Jitter on PowerQUICC III Processors," regarding phase jitter as TIE specification.
0	01/20/2010	Initial Release.

THIS PAGE INTENTIONALLY LEFT BLANK

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
 Technical Information Center, EL516
 2100 East Elliot Road
 Tempe, Arizona 85284
 1-800-521-6274 or
 +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
 Technical Information Center
 Schatzbogen 7
 81829 Muenchen, Germany
 +44 1296 380 456 (English)
 +46 8 52200080 (English)
 +49 89 92103 559 (German)
 +33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
 Headquarters
 ARCO Tower 15F
 1-8-1, Shimo-Meguro, Meguro-ku
 Tokyo 153-0064
 Japan
 0120 191014 or
 +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
 Exchange Building 23F
 No. 118 Jianguo Road
 Chaoyang District
 Beijing 100022
 China
 +86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor
 Literature Distribution Center
 1-800 441-2447 or
 +1-303-675-2140
 Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale, the Freescale logo, CodeWarrior, ColdFire, PowerQUICC, StarCore, and Symphony are trademarks of Freescale Semiconductor, Inc. Reg. U.S. Pat. & Tm. Off. CoreNet, QorIQ, QUICC Engine, and VortiQa are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.
 © 2010 Freescale Semiconductor, Inc.

