Freescale Semiconductor
Application Note

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Migration from MPC8313E Revision 1.0 to Revision 2.x

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1 Overview

The MPC8313E PowerQUICC™ II Pro processor delivers high performance with low power dissipation. It offers the following high-specification blocks:

- 333-MHz e300c3 core
- Integrated security engine
- Two Gigabit Ethernet interfaces with SGMII and IEEE Std 1588™ support
- Two SGMII PHY interfaces with single PLL
- 32-bit DDR 1/2 scaling to 333-MHz data rate
- Enhanced local bus controller with NAND Flash support
- 32-bit PCI 2.3 controller
- On-chip and external USB PHYs

MPC8313E revision 2.x is hardware backward compatible with revision 1.0 but requires some changes in software. Additional features, such as enabling/disabling NAND ECC during boot up, have been added.

Contents

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This document explores the migration from silicon revision 1.0 to 2.x with respect to software, hardware, internal module revision, and chip pin assignment, and serves as a relevant guide for both software and hardware developers.

This migration document is not intended to replace the latest silicon or reference manual errata. Refer to the Freescale website listed on the back page of this document for the latest versions of errata and related documents. Revision 1 of the *MPC8313E PowerQUICC™ II Pro Integrated Processor Family Reference Manual,* includes some of the revision 2.x silicon updates, and revision 2 of the reference manual will include the remaining changes.

2 Required Software Configuration

This section lists important software programming differences between revision 1.0 and revision 2.x. Customers wishing to continue with revision 2.x silicon in their revision 1.0 design must make the following required software changes:

1. SVR value, JTAG, PCI, and SPRIDR ID are different from revision 1.0 to 2.x. Refer to Section 2.1, “System ID Values in Revisions 1.0 and 2.x,” for more details.
2. Program the security revision ID to 0x0000_0000_0002_00A0. Refer to Section 2.1, “System ID Values in Revisions 1.0 and 2.x,” for more details.
3. Check the values of the SPCR registers as new functionality has been added to bits 0, 1, 16, and 17. Refer to Section 5.1.1, “SPCR Register Details,” for more details.
4. Check the value of the LTESR register as new functionality has been added to bit 30. Refer to Table 10 for more details.
5. Program the CONTROL[REFSEL] value to either 0x01 or 0x10 for a 24- or 48-MHz UTMI PLL reference clock frequency. See Section 2.2, “USB REFSEL Options in Revisions 1.0 and 2.x.”
6. If the MPC8313E was configured as a full-speed USB device (UTMI) in revision 1.0, CONTROL[USB_EN] should be used as described in Section 2.3, “USB Full-Speed Operation in Revisions 1.0 and 2.x.”
7. SICRH[7] controls two functions now. Its default value is 0x1 in revision 1.0, whereas its default value is 0x0 in revision 2.x. SICRH[7] = 1 selects the newly added 1588 timer functionality on the local bus address pins. Customers not wishing to use the 1588 timer functionality can simply set SICRH[7] to 0x0. If a read to this register is being compared with the expected default value, customers should be aware of the new default value. See Table 20 for more details.
8. If the values of the eTSEC interrupt vectors in software were previously changed per the workaround described in the IPIC1 erratum listed in the *MPC8313E PowerQUICC™ II Pro Integrated Host Processor Device Errata*, the original values need to be reinstated. The eTSEC interrupts were swapped in revision 1.0. This erratum was fixed in revision 2.x. Refer to Section 2.4, “eTSEC Interrupt Vectors in Revisions 1.0 and 2.x,” for more details.
9. If byte shifting was previously implemented in software per the workaround described in the eTSEC9 erratum listed in the *MPC8313E PowerQUICC™ II Pro Integrated Host Processor Device Errata*, software must be rewritten so that no byte shifting is done. In revision 1.0, software was required to compensate for an error in the byte offset for arbitrary L2 extraction filer

feature. The byte offset was shifted such that in some cases the wrong bytes were extracted and some byte offsets were unable to be extracted. This erratum was fixed in revision 2.x. Refer to Section 2.5, “eTSEC L2 Arbitrary Extraction in Revisions 1.0 and 2.x,” for more details.

To ensure the revision 1.0 design continues to function smoothly with this migration, please follow the precautions outlined in the remainder of this document.

2.1 System ID Values in Revisions 1.0 and 2.x

New SVRs have been assigned based on the system revisions. Their values are listed in Table 1.

Table 1. SVR Values

	SVR		
	Rev. 1.0	**Rev. 2.0**	**Rev. 2.1**
MPC8313E	0x80B0_0010	0x80B0_0020	0x80B0_0021
MPC8313	0x80B1_0010	0x80B1_0020	0x80B1_0021

The security block version ID has also been changed. Its revision 1.0 and revision 2.x values are listed in Table 2.

Table 2. Security ID Register Values

	Security Identification (ID) Register Values	
	Rev. 1.0	**Rev. 2.x**
MPC8313E	0x0000_0000_0000_00A0	0x0000_0000_0002_00A0

The updated JTAG ID, PCI REVID, and SPRIDR are listed in Table 3.

Table 3. Device ID Values

Register	Width	Rev. 1.0	Rev. 2.0	Rev. 2.1
JTAG ID	0–15	0x0687	0x2687	0x3687
PCI REVID	7–0	0x10	0x20	0x21
SPRIDR	16–31	0x0010	0x0020	0x0021

2.2 USB REFSEL Options in Revisions 1.0 and 2.x

In revision 1.0, the USB register CONTROL[REFSEL] defaults to 0x00, setting the frequency value for the UTMI PLL reference clock to 12 MHz; in revision 2.x, CONTROL[REFSEL] defaults to 0x01. Customers with revision 1.0 designs will need to change REFSEL to 0x01 for 24 MHz or 0x10 for 48 MHz in migrating to revision 2.x. Otherwise, the PLL will not lock, as CONTROL[REFSEL] = 0x00 is reserved. See Section 4.2, “Functional Corrections to Revision 1.0,” for more information.

2.3 USB Full-Speed Operation in Revisions 1.0 and 2.x

The issue with the pull up on the DP line not disappearing when the MPC8313E is configured as a full-speed USB device (UTMI) and a hard reset or power-on reset is asserted has been fixed. In order to initiate a device attach sequence, CONTROL[USB_EN] needs to be set before setting the USBCMD[RS] (run/stop) bit. Refer to USB18 in the *MPC8313E PowerQUICC™ II Pro Integrated Host Processor Device Errata*, for the history on this erratum.

2.4 eTSEC Interrupt Vectors in Revisions 1.0 and 2.x

The IPIC1 erratum listed in the *MPC8313E PowerQUICC™ II Pro Integrated Host Processor Device Errata* was fixed in revision 2.x. The workaround for revision 1.0 no longer applies. Customers who have changed the value of the eTSEC interrupt vectors in software should update their software to reflect the proper values for the eTSEC interrupts in the SIPNR_H/SIFCR_H/SIMSR_H registers as shown below:

5 = TSEC2 ERR
4 = TSEC2 RX
3 = TSEC2 TX
2 = TSEC1 ERR
1 = TSEC1 RX
0 = TSEC1 TX

Software should also be updated to reflect the proper eTSEC interrupt ID numbers as follows:

32 = TSEC1 TX
33 = TSEC1 RX
34 = TSEC1 ERR
35 = TSEC2 TX
36 = TSEC2 RX
37 = TSEC2 ERR

2.5 eTSEC L2 Arbitrary Extraction in Revisions 1.0 and 2.x

The eTSEC9 erratum listed in the *MPC8313E PowerQUICC™ II Pro Integrated Host Processor Device Errata* was fixed in revision 2.x. The workaround for revision 2.x no longer applies. Customers who implemented byte shifting in their software as described in the workaround for eTSEC9 should remove this byte shifting.

3 Software Workarounds for Revision 1.0 Errata

Both revision 1.0 and revision 2.x customers may remove or retain the software workarounds previously implemented for revision 1.0 as described in this section.

NOTE

In DDR24 listed in the *MPC8313E PowerQUICC™ II Pro Integrated Host Processor Device Errata*, one of the workarounds for revisions 1.0 and 2.0 recommendations is to prevent pipelined operation. It is recommended to use pipelined operation in revision 2.1.

The software workarounds for the following errata listed in the *MPC8313E PowerQUICC™ II Pro Integrated Host Processor Device Errata* are still required:

- eTSEC41: Multiple BD Tx frame may cause hang

The software workarounds for the following errata listed in the *MPC8313E PowerQUICC™ II Pro Integrated Host Processor Device Errata* can be removed, but leaving the workarounds in place will have no detrimental effects:

- SPI5: Selection of GPIO functionality on $\overline{\text{SPISEL}}$ signal causes MME in SPI
- PCI2: NXT_PTR field of hot swap register in PCI PM
- PCI22: PCI input and output hold from clock (t_{PCIXKH} and t_{PCKHOX}) do not meet specification
- eTSEC1: eTSEC reads to filer do not work
- eTSEC5: WWR bit anomaly
- eTSEC8: RSTAT[RXF0] set regardless of destination ring if WWR = 0
- eTSEC12: Tx IP and TCP/UDP checksum generation not supported for some Tx FCB offsets
- eTSEC15: Transmit jumbo frames greater than 2400 bytes may cause lost data, loss of BD synchronization, or false underrun error
- eTSEC18: Parsing of MPLS label stack or non-IPv4/IPv6 label not supported
- eTSEC19: Compound filer rules do not rollback the mask
- eTSEC20: Filer does not support matching on broadcast address flag PID1[EBC]
- eTSEC21: L3 fragment frame files on non-existent source/destination ports
- eTSEC22: RxBD[TR] not asserted during truncation when last 4 bytes match CRC
- eTSEC24: Parser results may be lost if TCP/UDP checksum checking is enabled
- eTSEC25: Transmission of truncated frames may cause hang or lost data
- eTSEC27: Transmitting PAUSE flow control frame may cause transmit lockup
- eTSEC28: eTSEC does not support parsing of LLC/SNAP/VLAN packets
- eTSEC29: Arbitrary extraction on short frames uses data from previous frame
- eTSEC30: Preamble-only with error causes false CR error on next frame
- eTSEC31: eTSEC filer reports incorrect Ethertypes with certain MPLS frames
- eTSEC34: Some combinations of Tx packets may trigger false data parity error (DPE)
- eTSEC35: Back-to-back Rx frames may lose parser results of second frame

- eTSEC36: Generation of Ethernet pause frames may cause Tx lockup and false BD close
- eTSEC39: May drop Rx packets with lossless flow control enabled
- eTSEC40: Rx synchronization error may cause corrupted packets and limitations with gigabit operation
- eTSEC46: eTSEC does not verify IPv6 routing header type field
- eTSEC47: No parse after back-to-back IPv6 routing header
- eTSEC48: L4 info passed to filer in L2/L3-only mode
- eTSEC49: MAC header data corruption
- eTSEC54: Frame > 9600 bytes with TOE = 1 hangs controller
- eTSEC56: Setting RCTRL[LFC] = 0 may not immediately disable LFC
- eTSEC60: Tx data may be dropped at low system to Tx clock ratios
- eTSEC61: Rx may hang if Rx FIFO overflows
- eTSEC62: Rx packet padding limitations at low clock ratios
- eTSEC63: False TCP/UDP checksum error for some values of pseudo header source address
- IEEE 1588_1: eTSEC IEEE 1588 reset bit
- IEEE 1588_9: 1588 reference clock limited to 1/2 CSB clock in asynchronous mode
- IEEE 1588_11: 1588 reference clock pulse required between writes to TMR_ALARM*n*_L and TMR_ALARM*n*_H
- IEEE 1588_15: Use of asynchronous 1588 reference clock may cause errors
- IEEE 1588_18: FIPER's periodic pulse phase not realigned when the 1588 current time is adjusted

4 New Features and Corrections

4.1 New Features

The following new features are available in revision 2.x:

- IEEE Std 1588, version-2 support.
- Two additional 1588 pin multiplexing options. See Section 7, "Pin Assignments," and Section 8, "Configuration of Newly Added Functions," for more information.
- One new field (SPCR[TSEC1588]) that controls the selection of multiplexing options for 1588 timer pins. See Section 5.1.1, "SPCR Register Details," for more information.
- Four new eLBC registers (FECC0–FECC3, Flash ECC block registers) for reporting the calculated ECC value. See Section 5.1.3, "FECCn Register Details," for more information.
- One new transfer error ECC register (LTECCR) for reporting correctable single-bit ECC errors and uncorrectable multi-bit ECC errors. See Section 5.1.4, "LTECCR Register Details," for more information.
- One new field (LTESR[UCC]) that shows the completion status for special operations on the eLBC UPMs. See Section 5.1.2, "LTESR Register Details," for more information.

- One new signal (LB_POR_CFG_BOOT_ECC_DIS) multiplexed with TSEC1_MDC that enables/disables ECC checking during boot time. In revision 1.0, ECC checking for the first 4K bytes of code from NAND flash was enabled by default. See Section 6, “Hardware Differences,” for more information.
- Two new fields (SPCR[BUFGTX125] and SPCR[BUFMDIO]) that control the input buffer of the TSEC1_GTX_125 clock and the TSEC1_MDIO pin. See Section 5.1.1, “SPCR Register Details,” for more information.
- The PCI space can now be configured as cacheable for the instruction spacethrough setting the e300 core HID0[ICE] bit. This is limited to fetching complete cache lines during reads (instruction fetches) and does not guarantee any data coherency. Software needs to ensure data coherency in cases where data is modified in the cache or another master performs a write to a cached PCI address.

4.2 Functional Corrections to Revision 1.0

- eTSEC:
  - The two eTSECs have been upgraded to correct numerous errata as documented in revision 2 of the *MPC8313E PowerQUICC™ II Pro Integrated Host Processor Device Errata*.
  - SGMII functionality is fully functional in revision 2.x. Refer to eTSEC2 in the *MPC8313E PowerQUICC™ II Pro Integrated Host Processor Device Errata*.
  - Customers using the eTSEC parser/filer should be aware of a difference in behavior between revision 1.0 and revision 2.x silicon. The difference involves handling of the Ethernet type/length field in cases where the field contains a value between 1500 and 1536. In revision 2.x, values between 1500 and 1536 are interpreted as a type. Since there are currently no valid types in this range publicly defined by IANA, the controller will not parse beyond the length/type field of any such frame.

    If the same packet is encountered with revision 1.0 silicon, parser/filer behavior is different. With revision 1.0, such packets are treated as payload length. Software must confirm the parser and filer results by checking the type/length field after the packet has been written to memory to see if it falls in this range.
- SEC:
  - The security engine now implements SEC revision 2.2.2. The new version includes fixes for AES counter issues and SRTP mode. See SEC1, SEC2, and SEC3 in the *MPC8313E PowerQUICC™ II Pro Integrated Host Processor Device Errata*.
  - The security engine ID is included in the security block identification register. In revision 1.0, the value of this ID was 0x0000_0000_0000_00A0. In revision 2.x, the value of this ID is 0x0000_0000_0002_00A0.
- PCI:
  - The NXT_PTR field of the PCI hot swap register in the PCI configuration space, which provides the address of the next power management capability, now has the correct value of 0x80. Previously, NXT_PTR had a value of 0x00, which shows the last capability in the list. NXT_PTR can be read internally using CFG_ADDR or externally using a configuration read

cycle. See PCI2 in the *MPC8313E PowerQUICC™ II Pro Integrated Host Processor Device Errata*.

- IPIC:
  - As mentioned in Section 2.4, "eTSEC Interrupt Vectors in Revisions 1.0 and 2.x," the eTSEC interrupts were swapped in revision 1.0 of the MPC8313E. Revision 2.x fixes this erratum (IPIC 1). Changing the value of the eTSEC interrupts vector in software is no longer necessary in revision 2.x.
- USB:
  - The USB PHY PLL meets USB compliance specifications in high-speed transmit mode with an on-chip USB 2.x PHY. Refer to USB1 in the *MPC8313E PowerQUICC™ II Pro Integrated Host Processor Device Errata*, for the history on this erratum.
  - The issue with the pull up on the DP line not disappearing when the MPC8313E is configured as a full-speed USB device (UTMI) and a hard reset or power-on reset is asserted has been fixed. In order to initiate a device attach sequence, CONTROL[USB_EN] needs to be set before setting the USBCMD[RS] (run/stop) bit. Refer to USB18 in the *MPC8313E PowerQUICC® II Pro Integrated Host Processor Device Errata*, for the history on this erratum.
  - Different REFSEL options in the USB CONTROL register for the on-chip PHY.

    Table 4 shows the original description for CONTROL[REFSEL], applicable to revision 1.0.

Table 4. CONTROL[REFSEL] Bit Settings (Revision 1.0)

Bits	Name	Description
24–25	REFSEL[1:0]	The REFSEL signals are used to set the frequency value for the UTMI PLL reference clock. These bit fields are not relevant if not in UTMI mode. 00 Reference clock frequency is 12 MHz (default) 01 Reference clock frequency is 16 MHz 10 Reference clock frequency is 48 MHz 11 Reserved

Table 5 shows the new description for CONTROL[REFSEL], applicable to revision 2.x.

Table 5. CONTROL[REFSEL] Bit Settings (Revision 2.x)

Bits	Name	Description
24–25	REFSEL[1:0]	The REFSEL signals are used to set the frequency value for the UTMI PLL reference clock. These bit fields are not relevant if not in UTMI mode. 00 Reserved 01 Reference clock frequency is 24 MHz (default) 10 Reference clock frequency is 48 MHz 11 Reserved

- General:
  - New SVR value for software detection. PVR remains 0x8085_0010. See Section 2.1, "System ID Values in Revisions 1.0 and 2.x."

5 Software Differences

Section 5.1, "New Fields and Registers in Rev 2.x," lists the memory map changes to revision 2.x.

5.1 New Fields and Registers in Rev 2.x

Table 6 lists registers and register fields new to revision 2.x. The new SPCR and LTESR fields were all reserved in revision 1.0 and set to 0. These fields all default to a value of 0 in revision 2.x. However, note that SPCR[BUFGTX125] and SPCR[BUFMDC_IO] will default to different values depending on the value of CFG_RESET_SOURCE[0:3] as seen in Table 8.

The SICRH[eLBC] field defaults to 1, such that when CFG_LBIU_MUX_EN is asserted during power-on reset, timer functionality is selected. See Table 20 for more information.

The FECC*n* registers and the LTECCR all default to zeros. However, once the MPC8313E has finished booting up, the values of the FECC*n* registers will depend on the ECC calculated over the first 4K of data in NAND Flash. The value of LTECCR will depend on whether single- or multi-bit errors were found while loading the boot code.

Table 6. New Registers and Fields

Register	Offset	Field	Bits	Change
SPCR	0x0_0110	BUFGTX125	0	New field; previously reserved. Controls buffer operation of the TSEC1_GTX_CLK125 pin.
		BUFMDIO	1	New field; previously reserved. Controls buffer operation of the TSEC1_MDIO pin.
		TSEC1588	16–17	New field; previously reserved. Selects one out of three 1588 timer-multiplexing options (eTSEC1, LA[0:15], UART2 + I^2C1).
LTESR	0x0_50B0	UCC	30	New field; previously reserved. Shows eLBC special operation completion status for UPM.
SICRH	0x0_0118	eLBC	7	New field; previously reserved. Selects function on multiplexed LA pins on the eLBC. 1588 timing option is pin function 2; LA option is pin function 0.
FECC*n*	0x0_5100	—	—	New register. Reports the calculated ECC value.
	0x0_5104	—	—	New register. Reports the calculated ECC value.
	0x0_5108	—	—	New register. Reports the calculated ECC value.
	0x0_510C	—	—	New register. Reports the calculated ECC value.
LTECCR	0x0_50C4	—	—	New register. Reports correctable single-bit ECC errors and uncorrectable multi-bit ECC errors.

5.1.1 SPCR Register Details

Table 7 shows the bit descriptions for SPCR[BUFGTX125] and SPCR[BUFMDC_IO]. As described in the eTSEC10 erratum in the *MPC8313E PowerQUICC™ II Pro Integrated Host Processor Device Errata*, the TSEC1_GTX_CLK signal is shared between eTSEC1 and eTSEC2, and TSEC1_GTX_CLK is internally supplied by LV_{DDB}, which supplies eTSEC1. In revision 1.0, when operating in RGMII or RTBI

mode, the voltage level of TSEC1_GTX_CLK125, which is supplied by an external PHY or oscillator, was required to be the same as the eTSEC1 voltage, which is controlled by SICRH[30].

The new fields SPCR[BUFGTX125] and SPCR[BUFMDIO] were added to revision 2.x to allow software control over the TSEC1_GTX_CLK and TSEC1_MDIO signals, such that the only remaining restriction is that a 3.3-V signal cannot be used to drive TSEC1_GTX_CLK125 when the eTSEC1 bank is powered by a 2.5-V LV_{DDB} supply.

Table 7. SPCR Register Description

Bits	Field	Description
0	BUFGTX125	Software control over the TSEC1_GTX_CLK125 signal. 0 The signal supplied from an external PHY or oscillator to TSEC1_GTX_CLK125 has the same voltage level as the LV_{DDB} power supply. (default) 1 A 2.5-V signal is supplied to TSEC1_GTX_CLK125 from an external PHY or oscillator, and the LV_{DDB} power supply has a 3.3-V voltage level.
1	BUFMDIO	Software control over the TSEC1_MDIO signal. Needs to be set according to the voltage level of the signal supplied to TSEC1_MDIO from an external PHY. 0 A 3.3-V signal is supplied from an external PHY to TSEC1_MDIO (default) 1 A 2.5-V signal is supplied from an external PHY to TSEC1_MDIO.

As shown in Table 8, the default values of SPCR[BUFGTX125] and SPCR[BUFMDC_IO] will differ in different configuration modes depending on the value of CFG_RESET_SOURCE[0:3]. The value of CFG_RESET_SOURCE[0:3] configures the different interface modes for eTSEC1 and eTSEC2.

Table 8. CFG_RESET_SOURCE and SPCR Settings

CFG_RESET_SOURCE[0:3]	eTSEC1 Mode	eTSEC2 Mode	SPCR[BUFGTX125] Default Value	SPCR[BUFMDC_IO] Default Value
1000	RTBI	MII	0	0
1001	RGMII	RTBI	0	1
1010	MII	RMII	0	0
1011	RMII	RTBI	1	0
1100	MII	RGMII	1	0

Table 9 shows the bit descriptions for SPCR[TSEC1588].

Table 9. SPCR[TSEC1588] Bit Settings

Bits	Name	Description
16–17	TSEC1588	00 Selects 1588 pins muxed with eTSEC1 (default) 01 Selects 1588 pins muxed with LA[10:15] PADs. 10 Selects 1588 pins muxed with UART2 + I2C1 PADs. 11 Reserved

5.1.2 LTESR Register Details

Table 10 shows the bit description for LTESR[UCC].

Table 10. LTESR[UCC] Bit Settings

Bits	Name	Description
30	UCC	UPM command completion event 0 No UPM operation in progress, or operation pending (default) 1 UPM operation has completed, allowing software to continue processing of results.

5.1.3 FECC*n* Register Details

The local bus Flash ECC block registers (FECC*n*), shown in Table 11, specify the ECC value calculated during writes or reads by eLBC. It can be used for verify after write feature in software. In the case that automatic ECC generation or checking is enabled, this register is guaranteed to hold the correct value after an FCM command completion event occurs and before the next FCM transaction is triggered.

Table 11. FECC*n* (FECC0–FECC3) Bit Settings

Bits	Name	Description
0	V	Valid bit. This bit denotes that the ECC stored in this register is valid. It is set for full page write/read transfers if ECC generation/checking is enabled in BR*n*[DECC]. (default 0)
1–7	—	Reserved (default 0)
8–31	ECC	24-bit ECC; For n^{th} 512 bytes of a page in case of large page or for $(4k + n)^{th}$ 512-byte page for small page where k = 0,1,2,...). It stores calculated ECC value during writes/reads. (default 0)

5.1.4 LTECCR Register Details

The transfer error ECC register LTECCR, shown in Table 12, captures errors during full page read transfers on an FCM command completion event, provided ECC checking is enabled in BRx[DECC]. It is a write-1-to-clear register. Write operations can clear but not set bits.

Table 12. LTECCR Bit Settings

Bits	Name	Description
0–11	—	Reserved (default 0)
12–15	SBCE	Single bit correctable error (default 0) There are at most four 512-byte page blocks (for a large page device) checked by ECC. A bit is set for the 512-byte block that had a single bit correctable ECC error on read (bit 12 represents block 0, the first 512 bytes of a page; if ORx[PGS] = 0, bits 13–15 are always 0).
16–27	—	Reserved (default 0)
28–31	MBUE	Multi bit uncorrectable error (default 0) There are at most four 512-byte page blocks (for a large page device) checked by ECC. A bit is set for the 512-byte block that had an uncorrectable ECC error on read (bit 28 represents block 0, the first 512 bytes of a page; if ORx[PGS] = 0, bits 29–31 are always 0).

6 Hardware Differences

This section shows the hardware differences between revisions 1.0 and 2.x.

6.1 Option for ECC Disable for NAND Auto Boot

In revision 1.0, ECC checking was enabled by default, and no option was available for disabling or enabling it. In revision 2.x, an eLBC control signal, LB_POR_CFG_BOOT_ECC_DIS, has been added to enable or disable ECC checking during boot time. This signal is multiplexed on TSEC1_MDC as function 1. It will automatically be selected whenever $\overline{\text{HRESET}}$ is asserted; the pin will act as TSEC1_MDC at all other times. The reset block will sample this signal on $\overline{\text{PORESET}}$ negation only. The sampled value is then passed to the eLBC controller to enable/disable ECC checking during boot time. An internal pull down has been added to the TSEC1_MDC pin to enable ECC checking by default. After $\overline{\text{HRESET}}$ is negated the TSEC1_MDC function will be selected again. See Table 13 and Figure 1 for details. Note that in revision 1.0 ECC checking was also enabled by default; if disabling ECC checking during boot time is not required in revision 2.x, no hardware or software modifications are necessary.

Table 13. LB_POR_CFG_BOOT_ECC_DIS Description

Value	Description
0	Boot time ECC checking enabled (default)
1	Boot time ECC checking disabled

To disable ECC checking on revision 2.x, use a high-impedance buffer on the board, as shown in Figure 1, to drive a strong pull up on the TSEC1_MDC pin while $\overline{\text{HRESET}}$ is asserted. If a strong external pull up of at least 1.5 kΩ on the TSEC1_MDC pin has already been added, but ECC checking during boot time is desired, a high-impedance buffer will need to be used to activate this external pull up only after $\overline{\text{HRESET}}$ is negated. If no change in ECC check enable/disable is intended, no changes are required. These options have been implemented on the revision 2.x RDB board with a dip switch, high-impedance buffer, and non-populated pull up on TSEC1_MDC.

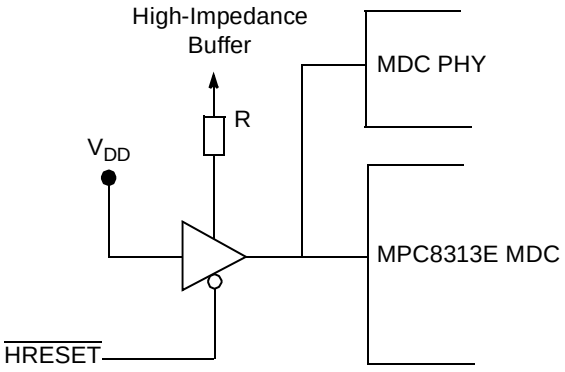

Figure 1. Recommended Circuit for Disabling ECC Checking at Boot Up

Recommended changes for all scenarios of existing revision 1.0 designs migrating to revision 2.x silicon are shown in Table 14.

Table 14. Recommended Circuit Changes on TSEC1_MDC Pin

New Feature Required (Ability to Disable ECC Checking)	Pull Up Exists on MDC	Pull Down Exists on MDC	Recommendations
No	No	No	No changes required
No	No	Yes	The external pull down will be in parallel to the internal 10k pull down. If the effective resistance becomes too low, it may hamper the TSEC1_MDC signal. It is recommended that the external pull down be removed.
No	Yes	No	Depending on the value of the external pull up, it may form a potential divider, which may be affected while booting and also on the TSEC1_MDS signal. It is recommended that the external pull up be removed.
Yes	No	No	Add circuit as shown in Figure 1.
Yes	No	Yes	Remove pull down and add the circuit as shown in Figure 1.
Yes	Yes	No	Isolate pull up with high-impedance buffer as shown in Figure 1.

6.2 Changes in AC and DC Specifications

Table 15 shows the changes in DDR AC timing.

Table 15. DDR Output AC Timing Changes

DDR Parameters	Symbol	Frequency (MHz)	Revision 1.0	Revision 2.x	Unit
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}	333	2.4	2.1	ns
		266	3.15	2.7	ns
$\overline{MCS}[n]$ output setup with respect to MCK	t_{DDKHCS}	333	2.4	2.1	ns
$\overline{MCS}[n]$ output hold with respect to MCK	t_{DDKHCX}	333	2.4	2.0	ns
		266	3.15	2.7	ns
MDQ//MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}	333	900	750	ps

Table 16 shows the change in the V_{IH} value for eLBC.

Table 16. Change in V_{IH} for eLBC

Parameter	Symbol	Revision 1.0	Revision 2.x	Unit
High-level input voltage	V_{IH}	2	2.1	V

The changes in power dissipation are shown in Table 17.

Table 17. Changes in Power Dissipation

Parameters	Core Frequency (MHz)	CSB Frequency (MHz)	Revision 1.0	Revision 2.x	Unit
Maximum power dissipation in active mode	333	167	1020	1200	mW
	400	167	1020	1200	mW
Maximum power dissipation in D3 warm mode	333	167	400	425	mW

7 Pin Assignments

MPC8313E revision 2.x uses the same 516-pin TEPBGA II package as revision 1.0. New pins are either muxed with existing pins or assigned to previously reserved pins, as shown in Table 18.

Table 18. MPC8313 Revision 2.x Pin Differences from Revision 1.0

Name	Description	Block	No. of Signals	I/O	Alternate Function	TEPBGAII
LB_POR_CFG_BOOT_ECC_DIS	Boot time ECC checking	eLBC	1	I	TSEC1_MDC	AF6
1588 Multiplexing Option with LA Pins						
TSEC_1588_TRIG2	1588 Timers	eTSEC	1	I	LA7	V23
TSEC_1588_ALARM1	1588 Timers	eTSEC	1	O	LA8	V24
TSEC_1588_PP3	1588 Timers	eTSEC	1	O	LA9	V25
TSEC_1588_CLK	1588 Timers	eTSEC	1	I	LA10	V26
TSEC_1588_GCLK	1588 Timers	eTSEC	1	O	LA11	U22
TSEC_1588_PP1	1588 Timers	eTSEC	1	O	LA12	AD24
TSEC_1588_PP2	1588 Timers	eTSEC	1	O	LA13	L25
TSEC_1588_TRIG1	1588 Timers	eTSEC	1	I	LA14	L24
TSEC_1588_ALARM2	1588 Timers	eTSEC	1	O	LA15	K26
1588 Multiplexing Option with DUART and I^2C Pins						
TSEC_1588_CLK	1588 Timers	eTSEC	1	I	UART_SOUT2	M3
TSEC_1588_GCLK	1588 Timers	eTSEC	1	O	UART_SIN2	L1
TSEC_1588_PP1	1588 Timers	eTSEC	1	O	$\overline{\text{UART\_CTS}}$[2]	L5
TSEC_1588_PP2	1588 Timers	eTSEC	1	O	$\overline{\text{UART\_RTS}}$[2]	L3
TSEC_1588_TRIG1	1588 Timers	eTSEC	1	I	IIC1_SDA	J4
TSEC_1588_ALARM2	1588 Timers	eTSEC	1	O	IIC1_SCL	J2

8 Configuration of Newly Added Functions

The SICRL and SICRH registers control the multiplexing of the device I/O pins. All newly added pins are configured in these registers. Table 19 and Table 20 show how to configure the SICRL and SICRH registers.

Table 19 defines the bit fields for the SICRL register. Each Pin Function column lists the name of the multi-function pin used in this option. Some groups have only two options (shown as Pin Function 0 and Pin Function 1) and therefore, only one control bit. In this case they can only have a value of 0b0 or 0b1. Other groups may have four options (shown as Pin Function 0, Pin Function 1, Pin Function 2, and Pin Function 3) and therefore, two control bits. In this case they can have a value of 0b00, 0b01, 0b10, or 0b11.

The newly added functions added to the SICRL and SICRH registers in revision 2.x are highlighted in bold text. The customer must check the values of these registers to confirm that the register bits are set as desired in the new configuration.

Table 19. Configuration Settings for the SICRL Register for Selecting 1588 Pin Multiplexing

SICRL [Bits] Value		0b0/0b00	0b1/0b01	0b10	0b11	Reset Value
Bits	**Group**	**Pin Function 0**	**Pin Function 1**	**Pin Function 2**	**Pin Function 3**	
2–3	LBC	LA0	MSRCID0 (DDRID)	—	GPIO[0]	11
		LA1	MSRCID1 (DDRID)	—	GPIO[1]	
		LA2	MSRCID2 (DDRID)	—	GPIO[2]	
		LA3	MSRCID3 (DDRID)	—	GPIO[3]	
		LA4	MSRCID4 (DDRID)	—	GPIO[4]	
		LA5	MDVAL (DDRID)	—	GPIO[5]	
		LA6	—	—	GPIO[6]	
		LA7	—	**TSEC_1588_TRIG2**	GPIO[7]	
		LA8	—	**TSEC_1588_ALARM1**	GPIO[13]	
		LA9	—	**TSEC_1588_PP3**	GPIO[14]	
4–5	UART	UART_SOUT1	MSRCID0 (DDRID)	—	—	00
		UART_SIN1	MSRCID1 (DDRID)	—	—	
		$\overline{\text{UART\_CTS}}$[1]	MSRCID2 (DDRID)	—	GPIO[8]	
		$\overline{\text{UART\_RTS}}$[1]	MSRCID3 (DDRID)	—	GPIO[9]	
		UART_SOUT2	MSRCID4 (DDRID)	—	**TSEC_1588_CLK**	
		UART_SIN2	MDVAL (DDRID)	—	**TSEC_1588_GCLK**	
		$\overline{\text{UART\_CTS}}$[2]	—	—	**TSEC_1588_PP1**	
		$\overline{\text{UART\_RTS}}$[2]	—	—	**TSEC_1588_PP2**	

Table 20 defines the bit fields for the SICRH register.

Table 20. Configuration Settings for the SICRH Register for Selecting 1588 Pin Multiplexing

SICRH [Bits] Value		0b0/0b00	0b1/0b01	0b10	0b11	Reset Value
Bits	**Group**	**Pin Function 0**	**Pin Function 1**	**Pin Function 2**	**Pin Function 3**	
7	eLBC	LA10		**TSEC_1588_CLK**[1]		1
		LA11		**TSEC_1588_GCLK**[1]		
		LA12		**TSEC_1588_PP1**[1]		
		LA13		**TSEC_1588_PP2**[1]		
		LA14		**TSEC_1588_TRIG**[1]		
		LA15		**TSEC_1588_ALARM2**[1]		
10–11	I^2C	IIC1_SDA	$\overline{\text{CKSTOP\_OUT}}$	—	**TSEC_1588_TRIG1**	00
		IIC1_SCL	$\overline{\text{CKSTOP\_IN}}$	—	**TSEC_1588_ALARM2**	

1 CFG_LBIU_MUX_EN must be asserted during power-on reset to select timer functionality.

9 Revision History

Table 21 provides a revision history for this application note.

Table 21. Document Revision History

Rev. Number	Date	Substantive Change(s)
1	10/2008	• Renamed all TMR_* signals with 1588_* • Added NOTE in Section 3, “Software Workarounds for Revision 1.0 Errata describing the need of reverting pipelined documentation due to DDR24. • Added column for Rev 2.1 in Table 1 and Table 3. • Changed revision 2.0 to revision 2.x as changes mentioned in this document is valid for Revsion 2.0 and 2.1. • Added Section 6.2, “Changes in AC and DC Specifications. • Made minor editorial changes to entire document.
	03/xx/08	Added third bullet to Section 4.2, “Functional Corrections to Revision 1.0.”
0	02/21/08	Initial release.

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