Power Cycling Algorithm using the MMA73x0L 3-Axis Linear Accelerometer

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INTRODUCTION

This is an article which describes techniques to minimize the power consumption of the MMA73x0L linear 3-axis accelerometer sensor while retaining the desired resolution and response time. The benefits of power cycling the accelerometer device are seen from the overall decreased power consumption of the device. This is extremely important in battery powered hand held electronic devices. Figure 1 shows the pin-out and direction of movement of the MMA73x0L accelerometer. The MMA73X0L accelerometer is a low power, low profile capacitive micromachined accelerometer featuring signal conditioning, a 1-pole low pass filter, temperature compensation, self test, 0g-detect which detects linear freefall, and g-Select which allows for the selection between 2 sensitivities. The zero-g offset and sensitivity are factory set and require no external devices. This accelerometer also has a sleep mode (pin 7) which makes it ideal for handheld battery powered electronics.

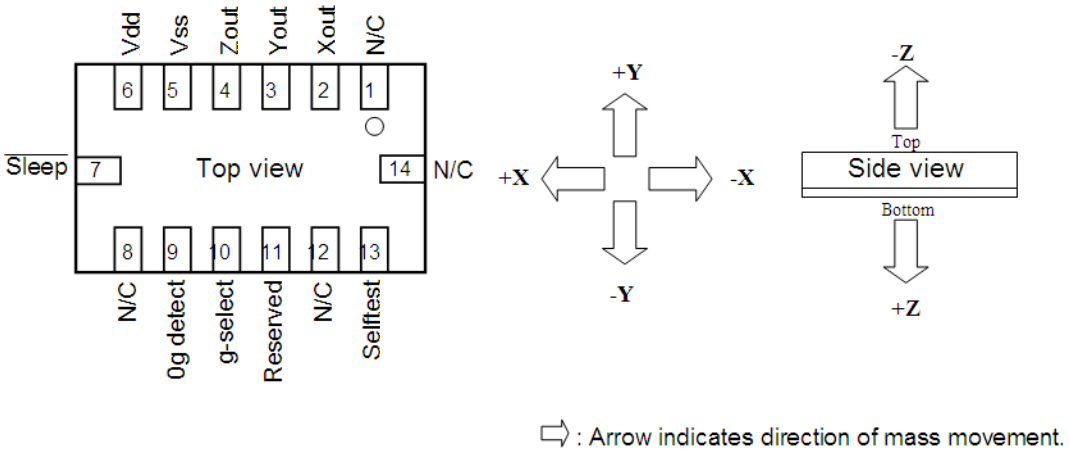


Figure 1. MMA73x0L 3-Axis Linear Accelerometer

One can reduce the overall power consumed by lowering the supply voltage, but the tradeoff of this is that this affects the sensitivity of the device because it is ratiometric. Cycling the accelerometer in and out of sleep mode can result in impressive power savings without affecting the sensitivity of the device. The device is only turned on for a small percentage of time to be able to measure the output reading from the accelerometer only as often as required by the application. The Freescale MMA73x0L accelerometers typically consumes 400µA in normal operational mode. In the lowest g-select setting in sleep mode (pin 7 from diagram above) the device consumes typically only 3µA, which is 99% less current. It is ideal to power cycle the accelerometer to be in sleep mode as much as possible.

There are a few things to consider before implementing a power cycling algorithm.

First, what is the application? What is the required resolution? What is the maximum input frequency required? Is there a set power specification target to meet? All of these questions will influence the parameters chosen for the optimal power cycling algorithm.

STEPS TO IMPLEMENTING A POWER CYCLING ALGORITHM

1. Choose the bandwidth (BW) for the output low pass filter.
2. Calculate the time constant based on the BW of the low pass filter.
3. Decide what the acceptable resolution is for the application.
4. Choose a sampling frequency and calculate the sampling period. Realize that you will be able to detect a signal that is half this sampling frequency. Verify that this is acceptable for the application.
5. Calculate the overall current consumption.

Choose BW for the Low-pass Output Filter

The low pass filter on the accelerometer X, Y and Z outputs is used, at a very minimum, to remove the clock noise from the internal switched capacitor filter circuit. This output low pass filter creates a time delay on the output response. The lower the bandwidth then the longer the time delay, which also ultimately will limit the maximum allowable sampling rate. The MMA73x0L accelerometers all have a 32k resistor on the output. Therefore the capacitor will determine the bandwidth of the low pass filter and the time constant. Using the following equation the BW of the low pass filter can be calculated.

$$BW_{LPF} = \frac{1}{2\pi RC}$$

At a minimum for reducing the clock noise a 3.3nF capacitor is suggested. The bandwidth response of the XY axis is 400Hz and the Z bandwidth response is 300Hz. Therefore it is strongly advised to choose a value for the low pass filter to be 400Hz or less. The bandwidth should be determined based on the maximum frequency input required to be detected for the application. This is recommended to maximize the resolution and dynamic range of the accelerometer. While higher bandwidths will allow lower power operation due to quicker enable times, this generally results in more noise.

Calculate the Time Constant

The time constant value is the enable time. This value is calculated with the following formula and is based on the capacitor value chosen for the low-pass output filter.

$$T_{enable} = 5xRC$$

NOTE: The enable time above is a very conservative estimate. A value of 3xRC might be an acceptable enable time. It would depend on the accuracy required for the application.

This enable time, combined with the microcontroller's sampling and A/D conversion time will determine how long the sleep pin needs to be held at V_{DD} to get an accurate reading. This is the time period that the accelerometer must be on (T_{ON}). Since the microcontroller's sample and A/D conversion time is much faster (typically 25 µs), the main limitation will be the time constant from the low-pass filter.

$$T_{ON} = T_{enable} + 25\mu s$$

Verify the Resolution Requirements for the Application

Resolution is the smallest detectable increment in acceleration. It is necessary to know what the smallest change is that needs to be detected. The accelerometer bandwidth will determine the measurement resolution, but filtering can be used to lower the noise floor and improve resolution further. The resolution can be improved by decreasing the bandwidth of the output low-pass filter. The tradeoff with better resolution is a longer enable time. The resolution is calculated by the following equation:

$$R = N \times \sqrt{BW_{LPF} \times 1.6}$$

where N is the poser spectral density noise in $\frac{\mu g}{\sqrt{Hz}}$.

The power spectral density noise value is characteristic of the accelerometer.

N=350 $\frac{\mu g}{\sqrt{Hz}}$ for X, Y, and Z; characteristic of the MMA73c0L.

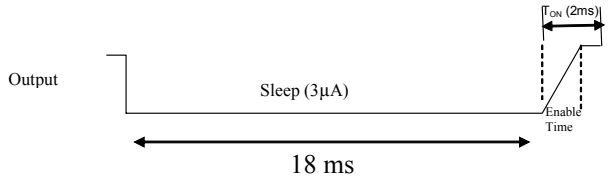
NOTE: If the resolution of the A/D converter is worse than the resolution calculated for the accelerometer then the system will be limited by the A/D converter.

Calculate the Sampling Period and Frequency

The sampling period at the very minimum must be at least T_{ON}. The duty cycle will be the percentage of the total period that the accelerometer must be on to take an accurate reading. For example, if the period is 20ms and it takes 2ms for T_{ON}, then the duty cycle will be 10%.

$$Period = \frac{T_{ON}}{DutyCycle}$$

Below is an example timing diagram showing a power cycling algorithm with a 10% Duty Cycle.



The maximum input frequency must be half (or less) the sampling frequency, satisfying the nyquist criteria. It is advisable to check that this matches with the input requirements of the application.

From the sampling period the maximum sampling frequency is the following:

$$SamplingFrequency = \frac{1}{Period}$$

Calculate the Current Consumption

The total current consumption will be approximated by the following equation:

400µA x Duty Cycle + 3µA x (1 - Duty Cycle)

Tilt: An Example Application for Power Cycling

Many tilt sensing applications are low speed in nature (<10Hz) and are often the best candidates for power cycling because the accelerometer can be turned on and off without the loss of data due to high speed changes in the output. Therefore the accelerometer can be turned off for longer times (lower sampling frequency required). The catch is that tilt applications often require a high resolution and therefore a low pass filter with a small bandwidth would be ideal to lower the noise floor. Decreasing the bandwidth on the output filter will increase the response time for the accelerometer to be able to turn on. A low pass filter with a cut off frequency of 20 Hz can be chosen, which results in a conservative time constant of approximately 40ms. If a sampling frequency of 20Hz is used (period of 50ms) then 10Hz is the maximum detectable tilt input frequency (satisfying the nyquist rate). This scenario would result in an average of 319µA of current when power cycling which is a 22% savings. If lower current consumption was required a larger bandwidth could be used on the low pass filter at the expense of the resolution. This would decrease the time constant. If the BW_{LPF}=50Hz, the time-on required is approximately 16ms, as shown in Table 5. If the same sampling frequency of 20Hz is used (period of 50ms) then the current consumption can be lowered to an average of 130µA, which is a 68% savings. Increasing the bandwidth on the low pass filter can dramatically reduce the current consumption. A comparison of the different low pass filter bandwidths for various sample rates are shown below displaying the resulting average output current for each.

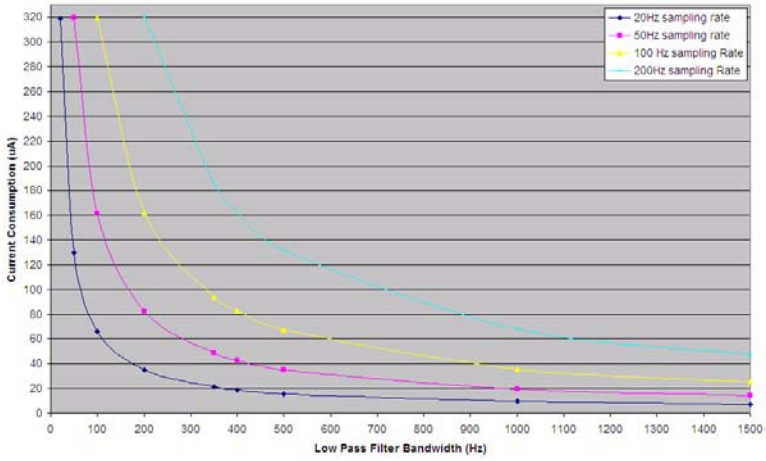


Figure 2. Average Current Consumption vs. BW_{LPF} for a Chosen Sampling Rate

Figure 2 is a comparison of the sample rate for a chosen low-pass filter BW and the resulting average current consumption.

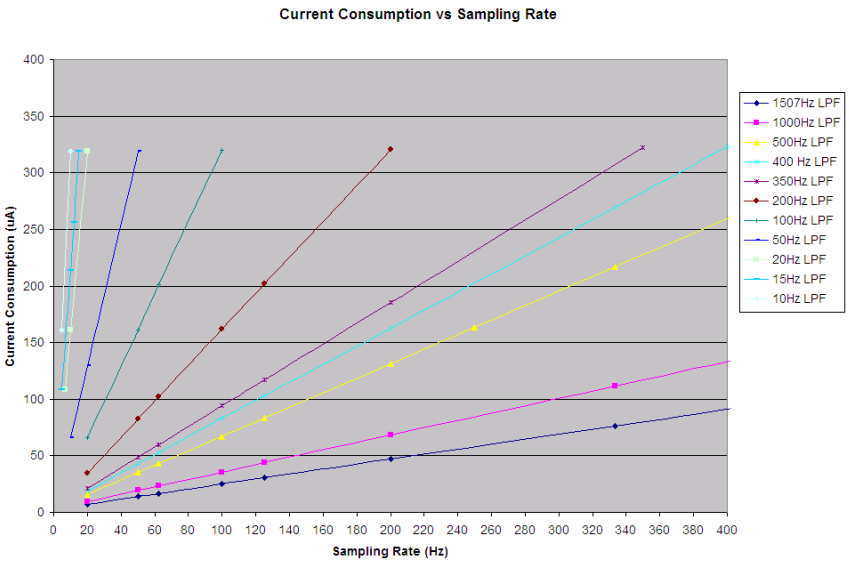


Figure 3. Average Current Consumption vs. Sampling Rate for a Chosen BW_{LPF}

The following tables show the different low pass filter bandwidths comparing different sampling frequencies.

Table 1. LPF with 3.3nF capacitor, BWLPF=1507Hz, T_{ON}=0.56ms, Res=17.19mg

Sampling Fq	Period	Duty Cycle	Total IDD (µA)
20Hz	50ms	1.1%	7.41
50Hz	20ms	2.5%	13.53
62.5Hz	16ms	3.3%	16.16
100Hz	10ms	5.3%	24.06
125 Hz	8ms	6.6%	45.12
200Hz	5ms	10.6%	73.21
500 Hz	2ms	26.5%	108.31
1000Hz	1ms	53.1%	213.62
1250Hz	0.8ms	69.4%	278.68
1500Hz	0.67ms	83.3%	333.81

Table 2. LPF with 12.4nF capacitor, BW_{LPF}=400Hz, T_{ON}=2.02ms, Res=8.85mg

Sampling Fq	Period	Duty Cycle	Total IDD (µA)
20Hz	50ms	4.0%	18.99
50Hz	20ms	10.1%	42.99
62.5Hz	16ms	12.6%	52.98
100Hz	10ms	20.1%	82.97
125 Hz	8ms	25.2%	102.97
200Hz	5ms	40.3%	162.95
333.3Hz	3ms	67.1%	269.58
400 Hz	2.5ms	80.6%	322.89

Table 3. LPF with 24.9nF capacitor, BW_{LPF}=200Hz, T_{ON}=3.98ms, Res=6.26mg

Sampling Fq	Period	Duty Cycle	Total IDD (µA)
20Hz	50ms	8%	34.79
50Hz	20ms	20%	82.48
62.5Hz	16ms	25%	102.35
100Hz	10ms	40%	161.95
125 Hz	8ms	50%	201.69
200Hz	5ms	80%	320.91

Table 4. LPF with 49.7nF capacitor, BW_{LPF}=100Hz, T_{ON}=7.98ms, Res= 4.43mg

Sampling Fq	Period	Duty Cycle	Total IDD (µA)
20Hz	50ms	16%	66.38
50Hz	20ms	40%	161.46
62.5Hz	16ms	49.9%	201.07
100Hz	10ms	79.8%	319.92

Table 5. LPF with 99.74nF capacitor, BW_{LPF}=50Hz, T_{ON}=15.94ms, Res= 3.13mg

Sampling Fq	Period	Duty Cycle	Total IDD (µA)
10Hz	100ms	15.9%	66.28
20Hz	50ms	31.9%	129.57
50Hz	20ms	79.7%	319.42

Table 6. LPF with 0.248uF capacitor, BW_{LPF}=20Hz, T_{ON}=39.8ms, Res= 1.98mg

Sampling Fq	Period	Duty Cycle	Total IDD (µA)
6.67Hz	150ms	26.5%	108.37
10Hz	100ms	39.8%	161.06
20Hz	50ms	79.6%	319.12

ALGORITHM IMPLEMENTATION USING A MICROCONTROLLER

The following are the steps that can be used as a guideline for programming a microcontroller to toggle the sleep pin on the MMA73x0L for a power cycling routine.

After the accelerometer and the microcontroller have been calibrated and initialized the following four steps will be repeated.

1. Set pin 7 (sleep pin) on MMA73x0L to Vdd (Turns the accelerometer on)
2. Wait for T_{ON} (This is the low pass filter time constant and the sampling and A/D conversion time by the microcontroller)
3. Set pin 7 (sleep pin) on MMA73x0L to Vss (Turns the accelerometer into sleep mode)
4. Wait for sleep time = Period-T_{ON}

CONCLUSION

The MMA73x0L accelerometer is inherently a low power sensor, yet there are power cycling techniques that can reduce the power further by lowering the current consumption. Generally extremely low power performance may result in a trade off with noise performance. It is important to understand the compromises and the application for the sensor to optimize the overall performance.

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