AN2506
Rev. 3, 4/2005

MSC8102 Design Checklist

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This application note provides a set of recommendations to assist you in a first-time design with the MSC8102 device. This document can also be useful as a general guideline for debugging newly designed systems because it highlights the aspects of a design that merit special attention during initial system start-up.

CONTENTS

1 Getting Started

During the first phase of designing a system with the MSC8102 device, your main tasks are to make the pin assignments and configure the reset parameters. Before you get started, you should be familiar with the available documentation, silicon revisions, software, models, and tools. Refer to **Section 10**, *Related Reading*, on page 19.

1.1 Making Pin Assignments

Some MSC8102 pins are multiplexed, depending on the device programming. Take care in programming MSC8102 registers to configure these multiplexed pins as needed for your system design. A signal function should be routed to a single pin, so if other pins provide that signal functionality, it should be turned off at the unused pins. Pin multiplexing is configured in the following registers:

- Hard reset configuration word (HRCW)
- SIU module configuration register (SIUMCR)
- Memory controller registers ORx and BRx
- GPIO port registers.

Also, some signals have one function during reset but switch to another multiplexed function during regular operation. These signals include SWTE, DSISYNC, DSI64, MODCK[1–2], and CNFGS. These signals switch to DSI functionality after exiting the reset state.

1.2 Configuring Reset Parameters

Review the HRCW to determine initial power-on-reset parameters, such as single MSC8102 bus mode versus 60x–compatible bus mode, boot port size, and on, and then set the bits for your application (see **Table 1**).

Table 1. Hard Reset Configuration Word (HRCW)

Name	Reset	Description	Settings	
EARB 0	0	**External Arbitration** Defines the initial value for ACR[EARB].	0 1	Internal arbitration is performed. External arbitration is assumed.
EXMC 1	0	**External MEMC** Defines the initial value of BR0[EMEMC].	0 1	No external memory controller is assumed. External memory controller is assumed.
INTOUT 2	0	**$\overline{\text{INT\_OUT}}$ or $\overline{\text{IRQ7}}$ Selection** Defines the initial value of SIUMCR[INTOUT].	0 1	$\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$ is $\overline{\text{IRQ7}}$. $\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$ is $\overline{\text{INT\_OUT}}$.
EBM 3	0	**External 60x-compatible Bus Mode** Defines the initial value of BCR[EBM].	0 1	Single bus mode. 60x-compatible bus mode.
BPS 4–5	00	**Boot Port Size** Defines the initial value of BR0[PS], the port size for memory controller bank 0.	00 01 10 11	64-bit port size. 8-bit port size. 16-bit port size. 32-bit port size.
SCDIS 6	0	**SC140 Cores Disabled** Enables/disables the SC140 cores.	0 1	SC140 cores enabled. SC140 cores disabled.
ISPS 7	0	**Internal Space Port Size** Defines the initial value of BCR[ISPS]. Setting ISPS enables a 32-bit master to access the internal space.	0 1	Acts as a 64-bit slave to external masters access to its internal space. Acts as a 32-bit slave to external masters access to its internal space.

Table 1. Hard Reset Configuration Word (HRCW) (Continued)

Name	Reset	Description	Settings
IRPC 8	0	**Interrupt Pin Configuration** Defines the initial value of SIUMCR[IRPC].	0 $\overline{\text{IRQ2}}$, $\overline{\text{IRQ3}}$, $\overline{\text{IRQ5}}$ active. 1 BADDR29, BADDR30, BADDR31 active.
— 9	0	Reserved. Write to zero for future compatibility.	
DPPC 10–11	00	**Data Parity Pin Configuration** Defines the initial value of SIUMCR[DPPC].	00 $\overline{\text{IRQ}}$[1–7] active. 01 DP[0–7] active. 10 DREQ[1–4], $\overline{\text{DACK}}$[1–4] active. 11 $\overline{\text{EXT\_BR}}$[2–3], $\overline{\text{EXT\_BG}}$[2–3], $\overline{\text{EXT\_DBG}}$[2–3], and $\overline{\text{IRQ}}$[6–7] active.
NMI OUT 12	0	**NMI OUT** Defines whether the host or one of the SC140 cores handles a non-maskable interrupt (NMI) event.	0 $\overline{\text{NMI}}$ is serviced by SC140 cores. 1 $\overline{\text{NMI}}$ is routed to $\overline{\text{NMI\_OUT}}$ and serviced by the external host.
ISBSEL 13–15	000	**Initial Internal Space Base Select** Defines the initial value of IMMR[ISB], which determines the base address of the internal memory space. The SC140 internal address space spans from 0x00000000–0x00FFFFFF (16 MB). Therefore it is not advisable to map the IMMR in this space, since the SC140s cannot access the SIU registers.	000 0xF0000000 001 0xF0F00000 010 0xFF000000 011 0xFFF00000 100 Reserved. Do not use. 101 Reserved. Do not use. 110 0x0F000000 111 0x0FF00000
BBD 17	0	**Bus Busy Disable** Defines the initial value of SIUMCR[BBD].	0 $\overline{\text{ABB}}$, $\overline{\text{DBB}}$ active 1 $\overline{\text{IRQ}}$[4–5] active
MMR 18	0	**Mask Masters Requests** Defines the initial value of SIUMCR[MMR].	0 No masking on bus request lines. 1 All external bus requests masked (boot master is the one of the internal cores).
TTPC 20	0	**Transfer Type Pin Configuration** Defines the initial value of SIUMCR[TTPC].	0 TT[0, 2–4] active. 1 $\overline{\text{CS}}$[5–7] active.
CS5PC 21	0	**Chip Select 5 Pin Configuration** Defines the initial value of SIUMCR[CS5PC].	0 $\overline{\text{CS5}}$ active. 1 $\overline{\text{BCTL1}}$ active.
TCPC 22–23	0	**Transfer Code Pin Configuration** Defines the initial value of SIUMCR[TCPC].	00 TC[0–2] active. 10 BNKSEL[0–2] active.
LTLEND 24	0	**Little Endian** Defines the host Endian mode of operation.	0 Big-endian. 1 Little-endian.
PPCLE 25	0	**Munged Little Endian** When the LTLEND bit is set, PPCLE specifies whether the host is a Little Endian host or a host that works in Munged Little Endian mode.	0 True little-endian host. 1 Munged little-endian host.
— 26	0	Reserved. Write to zero for future compatibility.	
DLLDIS 27	0	**DLL Disable** Defines whether the DLL mechanism is disabled.	0 No DLL bypass. 1 DLL bypass.
MODCK[3–5] 28–30	0	**MODCK High Order Bits** High-order bits of the MODCK bus, which determine the clock reset configuration. Refer to the chapter on clocks in the *MSC8102 Reference Manual*.	

Table 1. Hard Reset Configuration Word (HRCW) (Continued)

Name	Reset	Description	Settings
— 31	0	Reserved. Write to zero for future compatibility.	

2 Power

This section covers power supply, power consumption, power sequencing, power planes, decoupling, and power supply filtering. It also presents a recommended power supply design and low-power options. For information on AC/DC electrical specifications and thermal characteristics, refer to the data sheet.

- *Power Supply.* The MSC8102 has a core voltage, V_{DD}, that operates at a lower voltage than the I/O voltage V_{DDH}. You should supply the MSC8102 core voltage V_{DD} via a variable switching supply or regulator to allow for future compatibility with possible core voltage changes on future silicon revisions. The core voltage is supplied across V_{DD} and V_{SS} (GND). The core supply voltage must be between 1.55 V and 1.7 V.
- The I/O section of the MSC8102 is supplied with 3.3 V (± 5%) across V_{DDH} and V_{SS} (GND). Typically, this voltage is supplied by a simple linear regulator, which increases system complexity because multiple power supplies are required for the design. External signals on the MSC8102 are not 5 V tolerant. All input signals must meet the V_{IN} DC spec (–0.2 V to V_{DDH} + 0.2).
- *Power Sequencing*. For details, consult the “Design Considerations” section of the *MSC8102 Technical Data* sheet.
- *Suggested Power Supply Design.* One of the most common ways to derive power is to use either a simple fixed or adjustable linear regulator. For the system I/O voltage supply, a simple fixed 3.3 V supply can be used. However, a separate adjustable supply for the core voltage V_{DD} should be implemented. As **Figure 1** shows, an adjustable linear regulator supply can be used. To support future MSC8102 silicon revisions with lower core voltages for lower power, V_{OUT} can be adjusted by modifying the values of R_{2ADJ}. In **Figure 1**, the values R_1 = 150 Ω, R_2 = 390 Ω, and R_{2ADJ} = 0–1 KΩ generate an output voltage of 1.36–1.7 V.

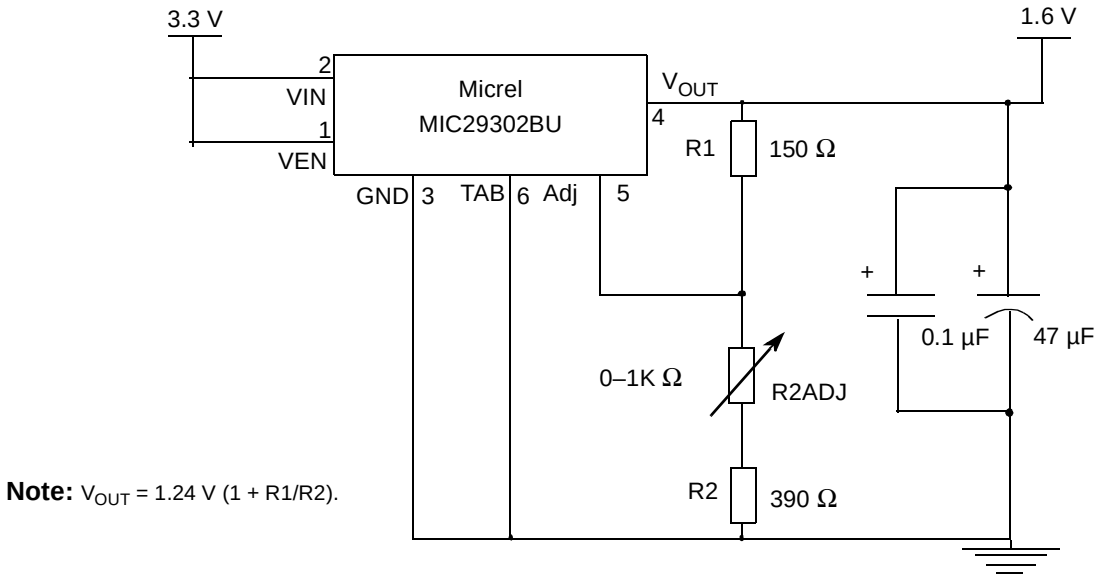

Figure 1. Core Power Supply Using Adjustable Linear Regulator

- *Power Planes.* Each V_{CC} and V_{DD} pin should have a low-impedance path to the board power supply. Each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the device. The MSC8102 V_{CC} power supply pins should be bypassed to ground using decoupling capacitors. The capacitor leads and associated printed circuit traces connecting to chip V_{CC}, V_{DD}, and GND should be kept to less than half an inch per capacitor lead. A minimum four-layer board that employs two inner layers as V_{CC} and GND planes is recommended. For details on MSC8102 layout, consult the “Power Supply Design Considerations” section of the *MSC8102 Technical Data* sheet.
- *Decoupling.* Both the I/O voltage (V_{DDH}) and core voltage (V_{DD}) should be decoupled for switching noise. For I/O decoupling, use standard capacitor values of 0.01 µF for every two to three voltage pins. For core voltage decoupling, use two levels of decoupling (see **Figure 2**). The first level should consist of a 0.01 µF high frequency capacitor (with low ESR and ESL) for every two to three voltage pins. The second decoupling level should consist of no less than three 150 µF bulk/tantalum decoupling capacitors (with low ESR and ESL) mounted as closely as possible to the MSC8102 voltage pins. Following this guideline, approximately twelve 0.01 µF capacitors should be used on the I/O (V_{DDH}) supply and placed as closely as possible to the MSC8102 device. Approximately seventeen 0.01 µF capacitors should be used on the core (V_{DD}) supply, placed as closely as possible to the MSC8102 device.

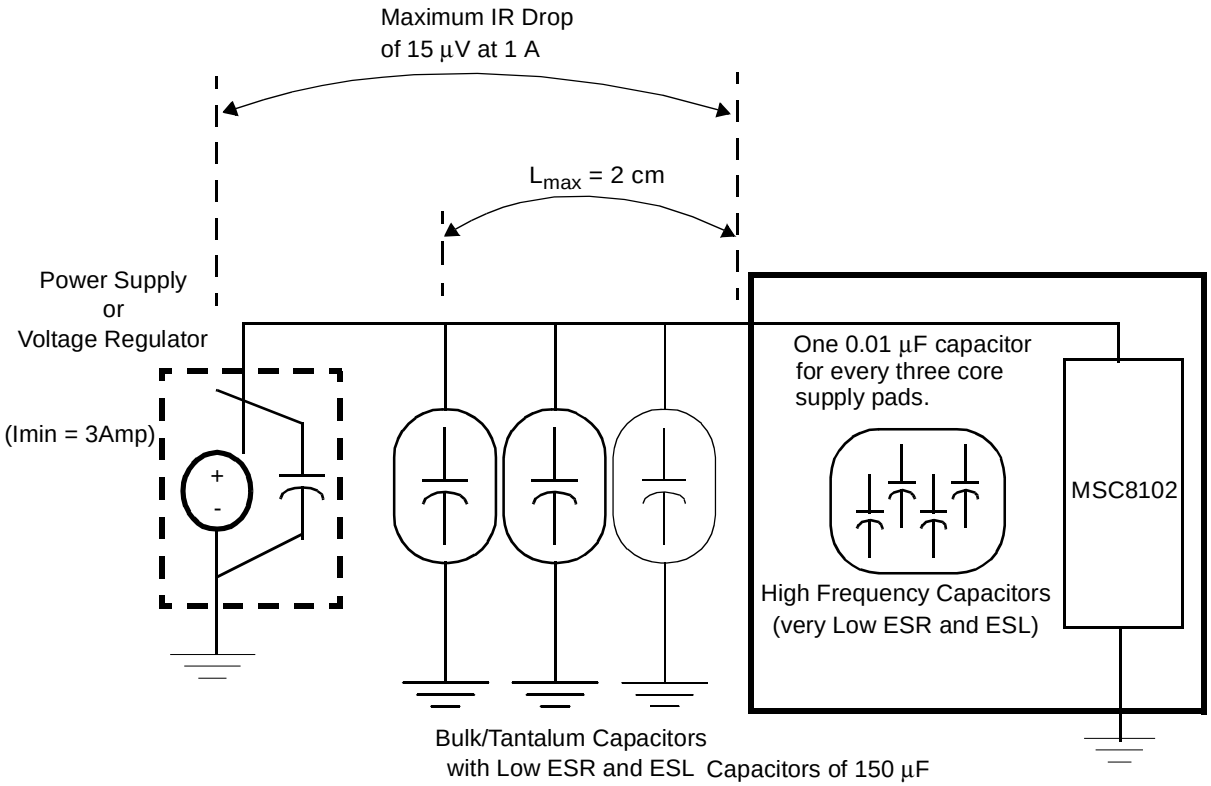

Figure 2. On-Board Power Supply Decoupling

- *PLL Power Supply Filtering.* The MSC8102 V_{CCSYN} power signal provides power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to this pin should be filtered with capacitors that have low and high frequency filtering characteristics (0.01 µF and 10 µF). V_{CCSYN} can be connected to V_{DD} through a 10Ω resistor. GND_{SYN} can be tied directly to the V_{SS} (GND) plane. A circuit similar to the one shown in **Figure 3** is recommended. The PLL loop filter should be placed as closely as possible to the V_{CCSYN} pin to minimize noise coupled from nearby circuits.The

0.01 µF capacitor should be closest to V_{CCSYN}, followed by the 10 µF capacitor, the 10-nH inductor, and finally the 10-Ω resistor to V_{DD}. These traces should be kept short. GND_{SYN} should be provided with an extremely low impedance path to ground and should be bypassed to V_{CCSYN}, respectively, by a 0.01 µF capacitor located as closely as possible to the device package.

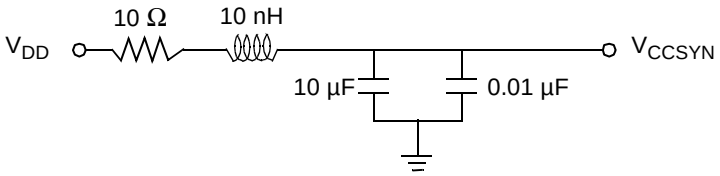

Figure 3. PLL Power Supply Filter Circuit

- *Power Consumption.* The *MSC8102 Technical Data* sheet provides preliminary power dissipation estimates for various configurations. You can take the following steps to reduce power consumption in your design.
  - *Stop mode for SC140 cores*. Any SC140 core can be placed into Stop mode when it is not in use. However, the core can be taken out of Stop mode only through a device reset such as $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, or $\overline{\text{SRESET}}$.
  - *CLKOUT disable*. If the system bus clock output is not needed in a system design, it can be masked by setting the SIUMCR[CLKOD] bit. Masking the clock output not only reduces power consumption but also noise in the design.
  - *Disable unused IP peripherals*. All IP bus peripherals have a control bit to mask their clock. Any unused peripherals should be programmed to Stop mode. For details, see the IPBus chapter of the *MSC8102 Reference Manual*.

3 Clocks

All inputs and outputs (except those associated with a serial clock) are referenced to REFCLK. In DLL-enabled mode REFCLK is DLLIN. In DLL-disabled mode REFCLK is CLKOUT.

- *MODCK[1–2]*. The MODCK[1–2] pins are sampled at the rising edge of $\overline{\text{PORESET}}$ (while $\overline{\text{HRESET}}$ is still asserted). Their value can be set using pull-ups/pull-downs. Therefore, open collector drivers are not needed.
- *MODCK[3–5]*. MODCK[3–5] can be set in the HRCW (or take the default value). Collectively, the MODCK[3–5] and MODCK[1–2] fields define the multiplication of the input clock (CLKIN) to derive the SC140 core and system bus clock ratios. Note that the SPLL multiplication value is set only during an initial $\overline{\text{HRESET}}$ caused by a $\overline{\text{PORESET}}$, so the SPLL does not change during subsequent assertions of $\overline{\text{HRESET}}$.

Refer to the *MSC8102 Reference Manual* for the most up-to-date clock configuration mode tables.

4 Reset

This section describes the reset recommendations for configuring the MSC8102 at reset.

4.1 Power-On-Reset Circuit

There is no power-up detector on the MSC8102 device. Optionally, a power-on-reset chip to monitor the power plane and drive $\overline{\text{PORESET}}$ can be used. $\overline{\text{HRESET}}$ is a bidirectional signal and, if driven as an input, should be driven with an open collector or open drain device. For an open-drain output such as $\overline{\text{HRESET}}$, take care when driving many buffers that implement input bus-hold circuitry. The bus-hold currents can cause enough voltage drop across the pull-up resistor to change the logic level to low. Either a smaller value of pull-up or less current loading from the bus-hold drivers overcomes this issue. To avoid exceeding the MSC8102 output current, the pull-up value should not be too small (a 1 KΩ pull-up is used in the MSC8102ADS reference design).

$\overline{\text{SRESET}}$ is a bidirectional signal and, if driven as an input, should be driven with an open collector or open-drain device. The MSC8102 device drives $\overline{\text{SRESET}}$ if the $\overline{\text{PORESET}}$ line or the $\overline{\text{HRESET}}$ line is asserted. A software watchdog timeout, bus monitor timeout, JTAG reset, or external soft reset can also drive $\overline{\text{SRESET}}$.

4.2 Reset Configuration Pins

The default HRCW (0x0000_0000) can be taken by connecting CNFGS to 0 and $\overline{\text{RSTCONF}}$ to a logic 1 on the rising edge of $\overline{\text{PORESET}}$. In this case, no accesses are made to the PROM connected to $\overline{\text{CS0}}$. The default case for the device is single MSC8102 mode. If the configuration word is not written via the 60x system bus during 1024 CLKIN cycles, the MSC8102 gets the default configuration word value.

Initial values other than the default can be obtained by selecting a different combination for the CNFGS and $\overline{\text{RSTCONF}}$ pins. $\overline{\text{BCTL0}}$ is active (functioning as W/$\overline{\text{R}}$) during the HRCW write. Take care to avoid bus contention during this time if buffers on the board are under $\overline{\text{BCTL0}}$ control. $\overline{\text{BCTL1}}$ should not be used during the reset configuration procedure. For details, refer to the Reset chapter of the *MSC8102 Reference Manual*.

Table 2. Reset Configuration Modes

CNFGS, $\overline{\text{RSTCONF}}$	Reset Configuration Word Source
00	Reset configuration via system bus. MSC8102 is configuration master.
01	Reset configuration via system bus. MSC8102 is configuration slave.
10	Reset configuration via write through DSI.
11	Reserved.

Table 2 shows the reset configuration mode options. If both CNFGS and $\overline{\text{RSTCONF}}$ are pulled to logic “0” on the rising edge of $\overline{\text{PORESET}}$, the MSC8102 device is a configuration master. In this case, the HRCW is read from the PROM connected to $\overline{\text{CS0}}$ at addresses 0x00, 0x08, 0x10, and 0x18. These four bytes are written to the fields of the HRCW. The MSC8102 device can act as a configuration master to configure up to seven MSC810x configuration slaves by individually connecting the $\overline{\text{RSTCONF}}$ lines of up to seven slaves to the most significant 7 address bits of the configuration master address bus. The master continues to read bytes starting at 0x20, configures the next slave while driving the $\overline{\text{RSTCONF}}$ line of the slave, and writes a 32-bit configuration word to that slave while the master drives the $\overline{\text{HRESET}}$ asserted to the slave. This is repeated from addresses 0x40, 0x60, 0x80, 0xA0, 0xC0, and 0xE0 for the remaining six slaves. The configuration master drives the full 32-bit configuration word on the 60x data bus after each of the 4-byte reads from the PROM. Avoid any contention on the bus that would affect the configuration word. No pull-ups are required on the address bus because it is actively driven during this operation.

If $\overline{\text{CNFGS}}$ is logic 1 and $\overline{\text{RSTCONF}}$ is logic 0 on the rising edge of $\overline{\text{PORESET}}$, the MSC8102 slave can be configured to receive the HRCW via the DSI. The host drives the HCID[0–3] signals to indicate which MSC8102 slave it is configuring. These signals can be driven by the host address lines. Alternatively, the host can write the HRCW to all MSC8102 slaves at once using the host broadcast chip select ($\overline{\text{HBCS}}$). The MSC8102 slave remains in reset state until it receives its HRCW.

4.3 Boot

The MSC8102 can be booted from memory on the system bus, a host on the system bus, a host via the direct slave interface (DSI), or via the time-division multiplexing module (TDM) or universal asynchronous receiver/transmitter (UART) ports. The boot source is determined by the state of the BM[0–2] signals sampled at the rising edge of $\overline{\text{PORESET}}$.

Table 3. Boot Mode Settings

BM0	BM1	BM2	Boot Sequence
0	0	0	External Memory on the system bus
0	0	1	External host via DSI or system bus
0	1	0	TDM
0	1	1	UART
1	x	x	Reserved

The MSC8102 device can boot from memory that is 8, 16, 32, or 64 bits wide. When an internal memory controller is to be used, the memory should be attached to $\overline{\text{CS0}}$, which functions as the global boot select, and be of the type that can be controlled by a GPCM machine (EPROM or Flash memory). The HRCW[BPS] bit sets the width of the $\overline{\text{CS0}}$ space. After configuration, SC140 core 0 fetches the address of the boot routine from location 0xFE000110.

If the MSC8102 device is booted from a host via the DSI or 60x system bus interface, the host polls the BR10[V] bit to determine when the boot program is finished. The host then begins its initialization procedure by loading code and data to the MSC8102 device. When done, it notifies the MSC8102 by sending VIRQ1 to SC140 core 0.

If the MSC8102 device is booted via the TDM, the TDM boot master writes blocks of code and data into MSC8102 internal memory. The transaction requires set up of the TDM physical layer as well as implementation of the TDM logical layer handshake. The boot master transmits messages to a single MSC8102 or multiple MSC8102 devices on TDM channel 0. The MSC8102 slave devices transmit back to the host on the TDM channel associated with their CHIP_ID. When the TDM session is complete, the valid bit of Bank 10 (BR10) is set to 1.

If the MSC8102 device is booted from a UART device, a UART boot master writes blocks of code and data into MSC8102 internal memory. Similar to the TDM boot option, the transaction requires set up of the physical layer and a UART logical layer handshake. When the UART session is complete, the valid bit of Bank 10 (BR10) is set to 1. For both the boot via TDM and boot via UART options, the boot code configures the GPIO pin multiplexing as required for external communication to boot in these modes. As a result, these GPIO configurations become the default pin multiplexing option for the affected signals in these two boot modes. For details, see the “Boot Program” chapter of the *MSC8102 Reference Manual*.

5 Bit and Byte Lane Ordering

This section describes the system bus bit and byte lane ordering.

- *Address/Data nomenclature*. It is recommended that schematics use documented terminology for the system bus as defined the chapter on “External Signals,” in the *MSC8102 Technical Data* sheet.
- *System bus*. The highest-order address bit is A0. The lowest-order address bit is A31. All 32 address pins are valid in a byte access. In a 64-bit access, only the upper 29 A[0–28] address pins are valid, and A[29–31] are driven low. For the 60x data bus, the highest-order data bit is D0 and the lowest-order data bit is D63.
- *Data byte lane ordering*. D[0–7] is the highest-order byte lane on the data bus, and D0 is the highest-order bit of that byte lane. D[0–7] corresponds to write enable 0 ($\overline{\text{PWE0}}$) and byte lane select 0 ($\overline{\text{PSDDQM0}}$). **Table 1** provides the data byte lane ordering for both the system bus and local bus.

Table 4. 60x Bus Data Byte Lane Ordering

Data Bus Signals	Byte Lane	External Pins (Byte Lane Select)
D[0–7]	0	$\overline{\text{PWE0}}$/$\overline{\text{PSDDQM0}}$/$\overline{\text{PBS0}}$
D[8–15]	1	$\overline{\text{PWE1}}$/$\overline{\text{PSDDQM1}}$/$\overline{\text{PBS1}}$
D[16–23]	2	$\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$
D[24–31]	3	$\overline{\text{PWE3}}$/$\overline{\text{PSDDQM3}}$/$\overline{\text{PBS3}}$
D[32–39]	4	$\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$
D[40–47]	5	$\overline{\text{PWE5}}$/$\overline{\text{PSDDQM5}}$/$\overline{\text{PBS5}}$
D[48–55]	6	$\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$
D[56–63]	7	$\overline{\text{PWE7}}$/$\overline{\text{PSDDQM7}}$/$\overline{\text{PBS7}}$

- *Memory controller byte lanes*. The memory controllers can access memories that are 8, 16, 32, and 64 bits wide without creating any “holes” in the memory space on the system bus. All memories should be placed into the most significant byte lanes as shown in **Table 2**.

Table 5. Byte Lanes for Memory Widths

Memory Width	Byte Lanes
Byte (8-bits)	0
2 Bytes (16-bits)	0, 1
4 Bytes (32-bits)	0, 1, 2, 3
8 Bytes (64-bits)	0, 1, 2, 3, 4, 5, 6, 7

- *Flash Memory Devices*. The data lines of most Flash memory devices are connected to the MSC8102 with byte lanes bit-reversed for programming algorithm purposes. A 32-bit example is shown in **Figure 4**. The figure is correct for a Flash SIMM composed of 8-bit Flash devices. Adjust the byte lanes as necessary for the memory used in your design. In addition, the Flash memory interface requires a reset input. The reset input should connect to the MSC8102 $\overline{\text{PORESET}}$.

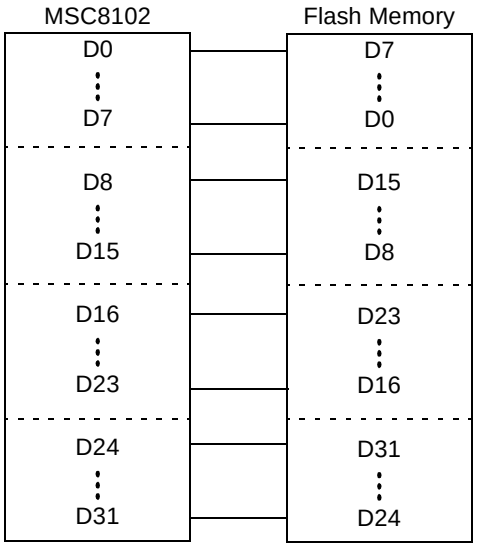

Figure 4. MSC8102 to Flash Memory Byte Lane Reversal

Bringing up a board with blank Flash memory and no host processor requires a switch or other method to force $\overline{\text{RSTCONF}}$ to a logic 1 and CNFGS to 0 to bring up the MSC8102 in the default state. Otherwise, invalid PLL values can be loaded. Once the device comes out of reset in the default state, the flash memory can be programmed. For subsequent resets, the $\overline{\text{RSTCONF}}$ and CNFGS signals can be set appropriately for resetting from Flash memory.

6 Memory

This section provides design considerations for the MSC8102 associated memories.

6.1 60x Bus Signals and Memory Transactions

The MSC8102 is not 5 V tolerant. All input signals must meet V_{IN} DC specifications (–0.2 V to V_{DDH} + 0.2).

- *Port Size Data.* The memory controller drives $\overline{\text{PSDVAL}}$ for an access to an MSC8102-controlled resource (internal space or chip-selects). $\overline{\text{PSDVAL}}$ is used only by external devices that implement the MSC8102 memory bank-based bus sizing protocol (for example, an external MSC8102). Devices that do not implement this memory bank-based bus sizing do not use $\overline{\text{PSDVAL}}$.
- *Non-MSC8102 masters.* MSC8102 designs incorporating devices that do not implement the MSC8102 memory bank-based bus sizing protocol must either use 64-bit accesses on the system bus or ensure that only MSC8102-initiated transactions can access the 8-, 16-, or 32-bit memory mapped slaves on the system bus.
- *Write enable.* $\overline{\text{PWE[0–7]}}$ should be used to control the R/$\overline{\text{W}}$ lines of memories, due to timing flexibility. For buffer direction control, use the $\overline{\text{BCTL[0–1]}}$ signals.
- *Pipelining.* The bus can be pipelined up to two address cycles deep (for example, it can have a $\overline{\text{TS}}$, an $\overline{\text{AACK}}$, and another $\overline{\text{TS}}$ before the first $\overline{\text{TA}}$). Because the address is valid only during the address phase ending with $\overline{\text{AACK}}$, external latches and multiplexes are necessary for SDRAM, and so on. On accesses to internal slaves such as CPM dual-port RAM, as well as SDRAM page hits, $\overline{\text{TA}}$ can come before $\overline{\text{AACK}}$. In fact, $\overline{\text{AACK}}$ and $\overline{\text{TA}}$ are not guaranteed to be in order.
- *Single MSC8102 mode.* In single MSC8102 bus mode, the bus operation is the same as the in 60x bus mode, except that the address that is driven on A[0–31] is latched and possibly multiplexed inside the

MSC8102. Therefore, the address is valid throughout the data phase of the cycle beginning with $\overline{\text{AACK}}$ and ending with the data phase of the next access. Single MSC8102 mode does not support mastering of the 60x system bus by any other resource, including an additional MSC8102 device.

- *Local bus.* The local bus does not burst when an external master accesses it through the 60x bus bridge. Accesses to the local bus are not snooped by the SC140 core.
- *Bursts.* Burst accesses by 60x masters to registers or to the local bus are terminated with $\overline{\text{TEA}}$.
- *Address acknowledge.* The MSC8102 asserts $\overline{\text{AACK}}$ for all accesses to external memory that match a BR/OR range in the memory controller (and also drives $\overline{\text{TA}}$ unless programmed otherwise).

6.2 BADDRx in 60x Mode

In 60x-bus-compatible mode, the BADDR [27–31] pins must be used—not the standard address A[27–31] pins—to address memories when the GPCM and UPM machines are in use. This is necessary because 60x masters (including the internal SC140 core) do not dynamically adjust the transaction for bus size. The 60x masters drive only the starting address on a burst, and thus the address lines do not increment. The GPCM memory controller accesses the memory as single accesses. Both the GPCM and the UPM increment the BADDRx lines to gather the bytes that the 60x master requests. In single MSC8102 mode, the memory controllers handle driving the address lines for small port sizes and increments for bursts. Therefore, the BADDRx pins are not needed in this mode.

6.3 Bank Selects Versus Address Lines

In single MSC8102 mode, use the BNKSEL lines to interface to SDRAM to support different SDRAM densities without requiring board wiring changes. Also, use the BNKSEL lines and set the BCR[EAV] bit so that logic analyzers can view the nonmultiplexed address of the access.

6.4 Page Versus Bank Interleaving

Page interleaving is the preferred method for connecting to SDRAM. Bank interleaving generally offers lower performance than page interleaving and is included for compatibility with designs that used this mode before page interleaving became available.

7 EOnCE/JTAG Interface

The MSC8102 device includes an enhanced on-chip emulation module (EOnCE), a feature common to all Freescale processors with the SC140 core. EOnCE gives internal access to scan chains for debug purposes and also provides a serial connection to the SC140 core for emulator support. An EOnCE/JTAG connection adds little or no cost to a system but adds significant advantages during early system development. This interface is implemented using a standard 14-pin header as shown in **Figure 5**.

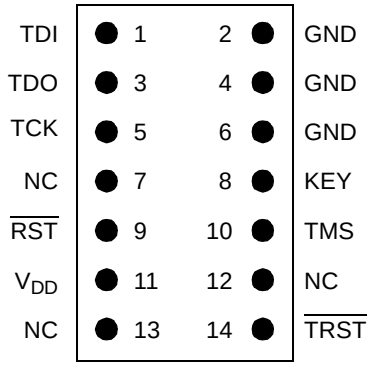

Figure 5. 14-Pin Header for JTAG/EOnCE Interface

The EOnCE interface connects through the JTAG port on the MSC8102 device with some additional status monitoring signals. **Table 6** shows the pin definitions and recommendations.

Table 6. JTAG/EOnCE Interface Pin Definitions

Pins	Connection	Description	Recommendations
1	TDI	Test Data In	If multiple devices on the JTAG chain, connect TDI to TDO of previous device in the chain.
2,4,6	GND	System Ground Plan	Connect to digital ground.
3	TDO	Test Data Out	If multiple devices on the JTAG chain, connect TDO to TDI of next device in the chain.
5	TCK	Test Clock	Add 10 KΩ pull-up resistor.
7,13,12	NC	No Connect	Leave unconnected.
8	KEY	Mechanical Keying	Pin should be removed.
9	$\overline{\text{RST}}$	Reset	May be tied to $\overline{\text{HRESET}}$.
10	TMS	Test Mode Select	None.
11	V_{DD}	I/O Power Supply	Connect to MSC8102 I/O Voltage V_{DDH} through a 220 Ω current limiting resistor.
14	$\overline{\text{TRST}}$	Test Reset	$\overline{\text{TRST}}$ has an internal pull-up, so no external pull-up or pull-down is required. However, it is recommended to add a 10k pull-down to GND on this signal to keep the JTAG in reset mode while the device is operating normally.

Connecting multiple devices via their JTAG port is commonly referred to as “daisy chaining.” Multiple target DSP devices can be connected in series so that a single command converter and JTAG connector can control multiple target DSPs. Daisy chaining should be considered for a board with multiple DSPs. In a daisy chain configuration, such as that shown in **Figure 6**, a serial path is formed by the connection of the serial Test Data In (TDI) and Test Data Out (TDO) pins. Essentially, the path formed by TDI and TDO connects the JTAG registers of the devices serially. The input pin to the entire chain is TDI, and the output pin from the entire chain is TDO. The Test Clock (TCK) and Test Mode Select (TMS) pins of all the devices are wired in parallel so that there is a single TCK input and a single TMS input. In this configuration, if a device in the daisy chain is reset, all devices on the chain are reset since the $\overline{\text{RESET}}$ signals are connected together.

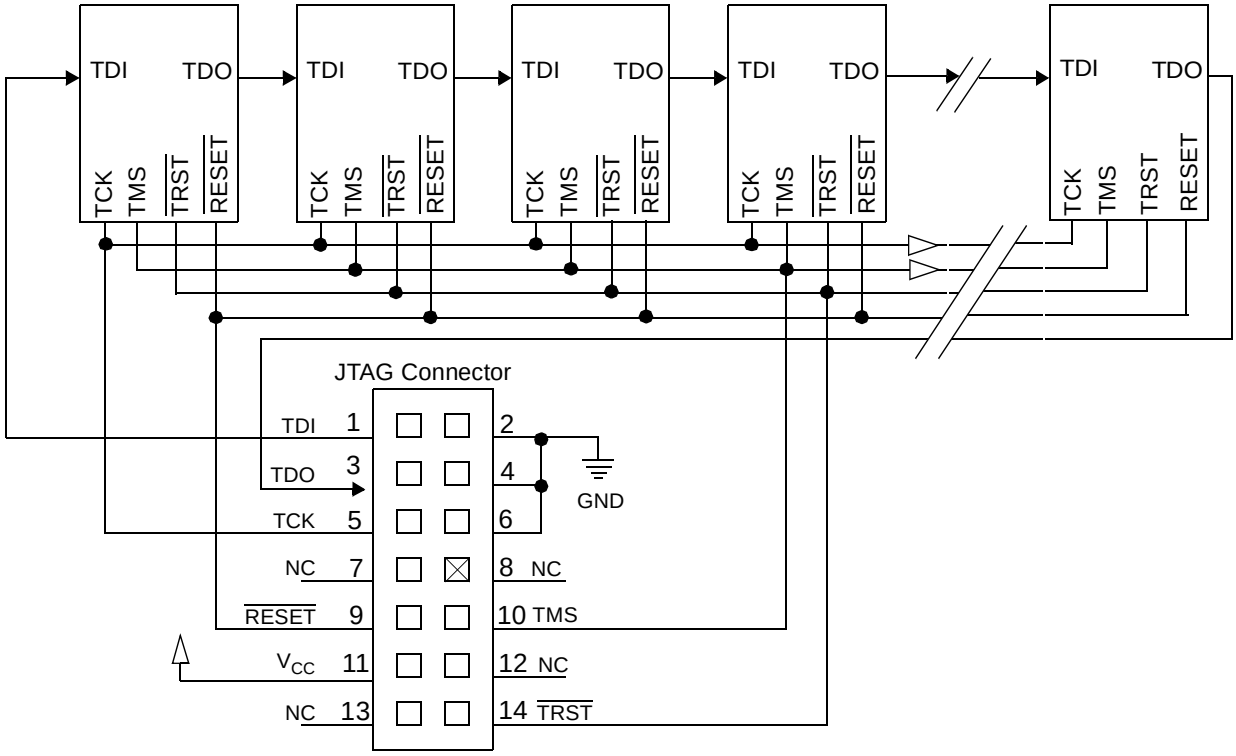

Figure 6. Multiple Target DSP Connection

Since the MSC8102 is a multi-core device, each SC140 core has its own link on the JTAG chain. Therefore, when designing a daisy chain, remember that each MSC8102 provides four indices to the chain. This is also important to remember when setting up JTAG chain initialization in software.

8 Signal Connectivity

This section summarizes the connections and special conditions (such as pull-up or pull-down resistors) for the MSC8102. **Table 7** lists the states of all of the signals during $\overline{\text{HRESET}}$ along with their recommended terminations. Following are guidelines for signal groups and configuration settings:

- Clock signals:
  - MODCK[1–2] configure the MSC8102 device and are sampled on the deassertion of $\overline{\text{PORESET}}$, so they should be tied to V_{CC} or GND either directly or through pull-up or pull-down resistors until the deassertion of $\overline{\text{PORESET}}$. After $\overline{\text{PORESET}}$ is deasserted, these signals can be floating.
  - DLLIN synchronizes to an external device. If no external device is used for synchronization, this signal should be connected to CLKOUT.
- Reset, configuration, and EOnCE signals:
  - SWTE/HD0, DSISYNC/HD1, DSI64/HD2, and CNFGS/HD5 configure the MSC8102 and are sampled on the deassertion of $\overline{\text{PORESET}}$, so they should be tied to V_{CC} or GND either directly or through pull-up or pull-down resistors until $\overline{\text{PORESET}}$ is deasserted. After $\overline{\text{PORESET}}$, these signals can be used as DSI interface data bus signals and can be left floating.

— $\overline{\text{RSTCONF}}$, CHIPID[0–3], and BM[0–2] configure the MSC8102 and are sampled until $\overline{\text{PORESET}}$ is deasserted, so they should be tied to V_{CC} or GND either directly or through pull-up or pull-down resistors until $\overline{\text{PORESET}}$ is deasserted. After $\overline{\text{PORESET}}$ is deasserted, these signals can be floating.

— $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ should be pulled up.

- Interrupt signals:
  — $\overline{\text{INT\_OUT}}$, $\overline{\text{NMI\_OUT}}$, and $\overline{\text{IRQxx}}$ should be pulled up.
- 60x-compatible system bus signals:
  — The following signals can be disconnected in single-master mode (BCR[EBM] is cleared): $\overline{\text{BG}}$, $\overline{\text{DBG}}$, $\overline{\text{EXT\_BG[2–3]}}$, $\overline{\text{EXT\_DBG[2–3]}}$, $\overline{\text{GBL}}$ and $\overline{\text{TS}}$. Also, in this mode $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ can be programmed as $\overline{\text{IRQ}}$ inputs (HRCW[BBD]=1) and should be connected to the non-active value. Otherwise, these two signals must be pulled up.
  — If BCR[EBM] is set, the following signals should be pulled up: $\overline{\text{BG}}$, $\overline{\text{BR}}$, $\overline{\text{DBG}}$, $\overline{\text{EXT\_BG[2–3]}}$, $\overline{\text{EXT\_DBG[2–3]}}$, $\overline{\text{EXT\_BR[2–3]}}$, $\overline{\text{TS}}$.
  — The following signals must be pulled up: $\overline{\text{ARTRY}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{PSDVAL}}$, $\overline{\text{AACK}}$.
  — If the system bus is not used and SIUMCR[PBSE] is set, $\overline{\text{PPBS}}$ can be disconnected. Otherwise, it should be pulled up.
- Direct Slave Interface (DSI):
  — If the DSI is unused, $\overline{\text{HCS}}$ and $\overline{\text{HBCS}}$ must be tied to V_{DD}. Remaining DSI signals can be left disconnected.
  — If using DSI in synchronous mode $\overline{\text{HTA}}$ must be pulled up. In asynchronous mode, it should either be pulled up or down, depending on design requirements.
  — If DSI is in asynchronous mode $\overline{\text{HBRST}}$ and HCLKIN should be disconnected or tied to V_{DD}.
  — If the DSI is in Big Endian mode HDST can be disconnected. It can also be disconnected if the DSI is in Little Endian mode and DCR[DSRFA] is set.
  — If the DSI is in 64-bit data bus mode and DCR[2]:BEM is cleared (single byte enable signal used), the DSI byte enable signals must be tied to V_{DD}. These signals include $\overline{\text{HWBS[1–3]}}$/$\overline{\text{HDBS[1–3]}}$/$\overline{\text{HWBE[1–3]}}$/$\overline{\text{HDBE[1–3]}}$ and $\overline{\text{HWBS[4–7]}}$/$\overline{\text{HDBS[4–7]}}$/$\overline{\text{HWBE[4–7]}}$/$\overline{\text{HDBE[4–7]}}$/$\overline{\text{PWE[4–7]}}$/$\overline{\text{PSDDQM[4–7]}}$/$\overline{\text{PBS[4–7]}}$.
  — If the DSI is in 32-bit data bus mode and DCR[BEM] is cleared (single byte enable signal used), $\overline{\text{HWBS[1–3]}}$/$\overline{\text{HDBS[1–3]}}$/$\overline{\text{HWBE[1–3]}}$/$\overline{\text{HDBE[1–3]}}$ must be tied to V_{DD}.
- General-Purpose I/O signals: All unused GPIO pins should be tied to GND.

9 Signal Terminations

In **Table 7**, signal connections are classified as follows:

- *xx–yyW VDDH*. A pull-up resistor to the V_{DDH} power supply, with a value between xx and yy Ω. You can select the value on the basis of system requirements, such as noise immunity.
- *xx–yyW GND*. A pull-down resistor to the ground power connection with a value between xx and yy Ω. Again, you can specify the value.
- O*pen*. The signal should/must be left unconnected. The Notes column in **Table 7** specifies whether it is a requirement.

- *As needed*. The connection is determined principally by the system. It connects to the system controller logic, whether from Freescale Semiconductor or one of several third-parties who make such logic. If not designated, a pull-up should be between 1–10 KΩ and connected to V_{DDH} and a pull-down between 100 Ω–1 KΩ and connected to GND.

Unused inputs should be tied high or low, but not left floating. Unused inputs can be tied directly to GND but a pull-up resistor is recommended if it is tied high. Generally, it is good practice to tie any unused input to GND or V_{DDH} through a resistor for board testability purposes. The following signals are active during the reset configuration period of $\overline{\text{HRESET}}$: A[0–31], $\overline{\text{BCTL0}}$, $\overline{\text{BCTL1}}$, D[0–63], $\overline{\text{CS0}}$, $\overline{\text{POE}}$, and BADDRx. All signals can be turned off using the HIGHZ JTAG command. Input-only signals such as $\overline{\text{PORESET}}$ or signals configured in an input-only mode, such as $\overline{\text{IRQx}}$ or $\overline{\text{EXT\_BRx}}$, do not require pull-up/pull-down resistors if they are actively driven. However, in the interest of caution, pull-up resistors are recommended in **Table 7**. You should exercise discretion. The hard reset signal states provided do not include the states during reset configuration. During the assertion of $\overline{\text{PORESET}}$, configurable signals have their default configuration (and are therefore tri-stated or high impedance). During reset configuration, configurable signals still have their default configuration, and certain memory controller signals operate to perform the reset configuration function (A[0–31], $\overline{\text{BCTL0}}$, $\overline{\text{BCTL1}}$, D[0–63], $\overline{\text{CS0}}$, $\overline{\text{POE}}$, BADDRx).

Table 7. Signal States and Recommended Termination

Signal	Function (See Note)	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
NOTE: I = input, O = output, B = bidirectional three-state, OD = open-drain. Most multi-function pins are bidirectional three-state. This does not imply that they are all shared signals—only that they can be used as inputs or outputs.					
$\overline{\text{BR}}$	B	Tri-stated, EARB = 0 High, EARB = 1	1–10 KΩ V_{DDH}		Pull up if EARB = 0.
$\overline{\text{BG}}$	B	High, EARB = 0 Tri-stated, EARB = 1	1–10 KΩ V_{DDH}		Pull up if HRCΩ:EARB = 1.
$\overline{\text{ABB}}$/$\overline{\text{IRQ4}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up.
$\overline{\text{TS}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up. In single-master mode, no pull-up resistor is required.
A[0–31]	B	Low	As needed	Open	No requirement.
TT0	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up in multi-master mode.
TT1	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up in multi-master mode.
TT[2–4]/$\overline{\text{CS[5–7]}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up TT[2–4] in multi-master mode.
$\overline{\text{TBST}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up.
TSIZ[0–3]	B	Tri-stated	As needed	Open	The TSIZ bus can be pulled up or down. Pull down TSIZ0 (100 Ω) if an external master exists. Otherwise, there is no requirement. In Single-Master mode, and these signals can be left open.
$\overline{\text{AACK}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up
$\overline{\text{ARTRY}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up
$\overline{\text{DBG}}$	B	High, EARB = 0 Tri-stated, EARB = 1	1–10 KΩ V_{DDH}		Pull up
$\overline{\text{DBB}}$/$\overline{\text{IRQ5}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up

Table 7. Signal States and Recommended Termination (Continued)

Signal	Function (See Note)	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
NOTE: I = input, O = output, B = bidirectional three-state, OD = open-drain. Most multi-function pins are bidirectional three-state. This does not imply that they are all shared signals—only that they can be used as inputs or outputs.					
D[0–31]	B	Tri-stated	As needed	Open	No requirement
HD[32–63]/ D[32–63]	B	Tri-stated	As needed	Open	No requirement
DP0/DREQ1/ EXT_BR2	B	High, DPPC = 11 Tri-stated Otherwise	As needed	Open	Pull up if used as EXT_BR2.
IRQ1/DP1/DACK1/ EXT_BG2	B	High, DPPC =11 Tri-stated, Otherwise	As needed	Open	Pull up if used as IRQ1 or DACK1. Pull up EXT_BG2 in multi-master mode.
IRQ2/DP2/DACK2/ EXT_DBG2	B	High, DPPC = 11 Tri-stated, Otherwise	As needed	Open	Pull up if used as IRQ2 or DACK2. Pull up EXT_DBG2 in multi-master mode.
IRQ3/DP3/ DREQ2/ EXT_BR3	B	High, DPPC = 11 Tri-stated, Otherwise	As needed	Open	Pull up if used as IRQ3 or EXT_BR3.
IRQ4/DP4/ DACK3/ EXT_BG3	B	High, DPPC = 11 Tri-stated, Otherwise	As needed	Open	Pull up if used as IRQ4 or DACK3. Pull up EXT_BG3 in multi-master mode.
IRQ5/DP5/ DACK4/ EXT_DBG3	B	High, DPPC = 11 Tri-stated, Otherwise	As needed	Open	Pull up if used as IRQ5 or DACK4. Pull up EXT_DBG3 in multi-master mode.
IRQ6/DP6/DREQ3	B	High, DPPC = 11 Tri-stated, Otherwise	As needed	Open	Pull up if used as IRQ6.
IIRQ7/DP7/ DREQ4	B	High, DPPC = 11 Tri-stated, Otherwise	As needed	Open	Pull up if used as IRQ7.
PSDVAL	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up
TA	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up
TEA	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up
GBL/IRQ1	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up
BADDR29/IRQ5	B	Low	As needed	Open	Pull up if used as IRQ5.
BADDR30/IRQ2	B	Low	As needed	Open	Pull up if used as IRQ2.
BADDR31/IRQ3	B	Low	As needed	Open	Pull up if used as IRQ3.
CS[0–4]	O	High	As needed	Open	No requirement
BCTL1/CS5	O	High	As needed	Open	No requirement

Table 7. Signal States and Recommended Termination (Continued)

Signal	Function (See Note)	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
NOTE: I = input, O = output, B = bidirectional three-state, OD = open-drain. Most multi-function pins are bidirectional three-state. This does not imply that they are all shared signals—only that they can be used as inputs or outputs.					
BADDR[27–28]	O	Low	As needed	Open	No requirement
ALE	O	High	As needed	Open	No requirement
$\overline{\text{BCTL0}}$	O	Low	As needed	Open	No requirement
$\overline{\text{PWE}}$[0–3]/ $\overline{\text{PSDDQM}}$[0–3]/ $\overline{\text{PBS}}$[0–3]	O	High	As needed	Open	No requirement
PSDA10/PGPL0	O	High	As needed	Open	No requirement
$\overline{\text{PSDWE}}$/PGPL1	O	High	As needed	Open	No requirement
$\overline{\text{POE}}$/$\overline{\text{PSDRAS}}$/ PGPL2	O	High	As needed	Open	No requirement
$\overline{\text{PSDCAS}}$/PGPL3	O	High	As needed	Open	No requirement
PGTA/PUPMWAIT/ PPBS/PGPL4	B	Tri-stated	As needed	Open	Pull up if used as PUPMWAIT or PGTA.
PSDAMUX/PGPL5	O	Low	As needed	Open	No requirement
HD0/SWTE	B	Tri-stated	As needed	—	Pull up or pull down at $\overline{\text{PORESET}}$ to enable/disable software watchdog.
HD1/DSISYNC	B	Tri-stated	As needed	—	Pull up or pull down at $\overline{\text{PORESET}}$ to enable/disable DSI synchronous mode.
HD2/DSI64	B	Tri-stated	As needed	—	Pull up or pull down at $\overline{\text{PORESET}}$ to set the width of the DSI and system buses.
HD3/MODCK1	B	Tri-stated	10KΩ	—	Pull up or pull down per desired clock configuration.
HD4/MODCK2	B	Tri-stated	10KΩ	—	Pull up or pull down per desired clock configuration.
HD5/CNFGS	B	Tri-stated	As required by reset configuration mode	—	$\overline{\text{RSTCONF}}$ and CNFGS define the MSC8102 reset configuration mode and should be either pulled up or pulled down as appropriate for reset mode. For details, see **Section 4**.
HD[6–31]	B	Tri-stated	As needed	Open	
HA[11–29]	I	Tri-stated	As needed	Open	
$\overline{\text{HWBS}}$[0–3]/ $\overline{\text{HDBS}}$[0–3]/ $\overline{\text{HWBE}}$[0-3]/ $\overline{\text{HDBE}}$[0–3]	I	Tri-stated	As needed	Open	Pull up
$\overline{\text{HWBS}}$[4–7]/ $\overline{\text{HDBS}}$[4–7]/ $\overline{\text{HWBE}}$[4–7]/ $\overline{\text{HDBE}}$[4–7]/ $\overline{\text{PWE}}$[4–7]/ $\overline{\text{PSDDQM}}$[4–7]/ $\overline{\text{PBS}}$[4–7]	B	Tri-stated	As needed	Open	Pull up
$\overline{\text{HRDS}}$/HRW/ HRDE	I	Tri-stated	As needed	Open	Pull up

Table 7. Signal States and Recommended Termination (Continued)

Signal	Function (See Note)	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
NOTE: I = input, O = output, B = bidirectional three-state, OD = open-drain. Most multi-function pins are bidirectional three-state. This does not imply that they are all shared signals—only that they can be used as inputs or outputs.					
HBCS	I	Tri-stated	As needed	Tie to V_{DD}	When used with a pull up, a 2.2 KΩ pull up is recommended.
$\overline{\text{HTA}}$	O	Tri-stated	As needed	Open	Pull up in synchronous mode.
$\overline{\text{HBRST}}$	I	Tri-stated	As needed	Open	
HCID[0–3]	I	Tri-stated	As needed	Open	
HCLKIN	I	Tri-stated	As needed	Open	
$\overline{\text{HCS}}$	I	Tri-stated	As needed	Tie to V_{DD}	
HDST0	I	Tri-stated	As needed	Open	Can be left disconnected if the DSI is in Big Endian mode.
HDST1	I	Tri-stated	As needed	Open	Can be left disconnected if the DSI is in Big Endian mode.
GPIO0/ $\overline{\text{CHIP\_ID0}}$/ $\overline{\text{IRQ4}}$	B	Tri-stated	As needed	Tie to GND	Configure as needed to define the MSC8102 chip ID.
GPIO1/TIMER0/ $\overline{\text{CHIP\_ID1}}$/ $\overline{\text{IRQ5}}$	B	Tri-stated	As needed	Tie to GND	Configure as needed to define the MSC8102 chip ID.
GPIO2/TIMER1/ CHIP_ID2/$\overline{\text{IRQ6}}$	B	Tri-stated	As needed	Tie to GND	Configure as needed to define the MSC8102 chip ID.
GPIO29/ CHIP_ID3	B	Tri-stated	As needed	Tie to GND	Configure as needed to define the MSC8102 chip ID.
Remaining GPIO signals	B	Tri-stated	As needed	Tie to GND	Leave any unused GPIO signals as input and tie them to GND.
$\overline{\text{NMI}}$	I	Tri-stated	1K–10KΩ VDDH		Pull up
$\overline{\text{NMI\_OUT}}$	O	Tri-stated	As needed	Open	Pull up
$\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$	B	High, IRQ7INT = 0 Otherwise: Tri-stated.	As needed	Open	Pull up
$\overline{\text{TRST}}$	I	Internal pull-up resistor	100–1 KΩ to GND		See **Table 6**.
TCK	I	Tri-stated	1–10 KΩ to GND		See **Table 6**.
TMS	I	Internal pull-up resistor	1–10 KΩ to V_{DDH}		See **Table 6**.
TDI	I	Internal pull-up resistor	1–10 KΩ to V_{DDH}		See **Table 6**.
TDO	O	Tri-stated	As needed	Open	See **Table 6**.
TEST	I	Tri-stated	0Ω to V_{SS}		See **Table 6**.
$\overline{\text{PORESET}}$	I	Tri-stated	1–10 KΩ to V_{DDH}		Pull up
$\overline{\text{HRESET}}$	OD	Low	1–10 KΩ to V_{DDH}		Pull up
$\overline{\text{SRESET}}$	OD	Low	1–10 KΩ το V_{DDH}		Pull up

Table 7. Signal States and Recommended Termination (Continued)

Signal	Function (See Note)	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
NOTE: I = input, O = output, B = bidirectional three-state, OD = open-drain. Most multi-function pins are bidirectional three-state. This does not imply that they are all shared signals—only that they can be used as inputs or outputs.					
$\overline{\text{RSTCONF}}$	I	Tri-stated	As required by reset configuration mode	—	$\overline{\text{RSTCONF}}$ and CNFGS define the MSC8102 reset configuration mode and should be either pulled-up or pulled-down as appropriate for reset mode. See **Section 4** for details.
EE0	I	Active	1–10 KΩ to V_{SS}		Pull down
EE1	O	Active	As needed	Open	
BM[0–2/TC[0–2]/ BNKSEL[0–2]	B	Tri-stated	As needed	—	Pull up or pull down per desired boot mode configuration.
CLKIN	I	Tri-stated	As needed	—	Provide appropriate clock.
CLKOUT	O	Active	As needed	Open	
DLLIN	I	Tri-stated	As needed	Open	Bypass DLL by setting bit 27 of hard reset configuration word.

10 Related Reading

The reference materials listed in **Table 8** can be obtained at the web site listed on the back cover of this document. Visit the relevant product summary page or search by title or document identification number.

Table 8. Related Reading

Document Category	Document Title	Document ID
Data Sheet (Hardware Specifications)	*MSC8102 Technical Data* sheet	MSC8102
Errata (device)	MSC8102 Silicon Errata	MSC8102CEK94M
Manuals	*MSC8102 Reference Manual*	MSC8102RM
	MSC8102 User's Guide	MSC8102UG
	SC140 DSP Core Reference Manual	MNSC140CORE
Application Notes	List available on the Freescale web site.	
Reference Design	*MSC8102 Application Development System User's Manual*	MSC8102ADSUM

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AN2506
Rev. 3
4/2005