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Configuring Freescale PrMC Cards

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This application note describes the features of the Freescale PrPMC (processor PCI mezzanine card) family for the Sandpoint evaluation platform. PrPMC cards are used with the Sandpoint evaluation system to evaluate the performance and develop software for PowerPC™ processors. In particular, it covers the configurable settings each card permits. Particular emphasis is on the flash memory resources available to those cards, and the various ways the devices can be programmed or used for software/applications purposes.

PrPMC cards have several features to evaluation different system configurations. This application note discusses several configuration and usage issues for the Freescale PrPMC family, including:

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1 Overview

Freescale PrPMC cards have a fairly standardized architecture, with minor variations to support certain important chip-specific features. In general, all PrPMC cards have local boot flash and SDRAM; everything that would be above the PCI interface of the northbridge of a typical computer system. All high speed design issues are resolved on the PrPMC card, with differentiation made at the PCI interface level.

Figure 1 shows a block diagram of the typical PrPMC card.

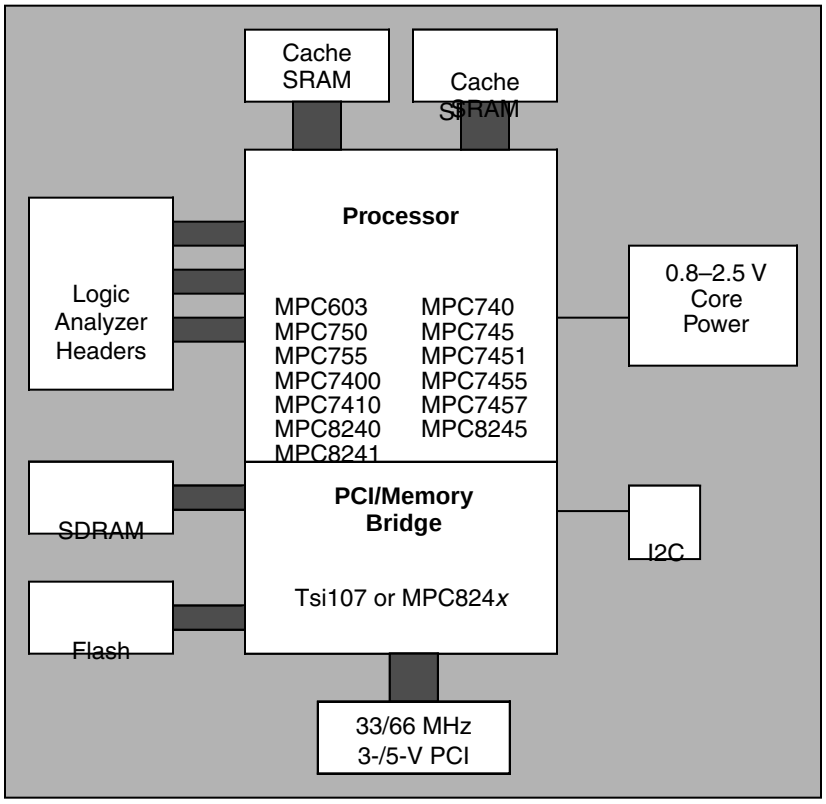

Figure 1. PrPMC Block Diagram

Not all cards implement all of the above features, and some PrPMC cards differ in small ways (such as, the use of SODIMMs for SDRAM memory versus discrete (on-board) memory).

2 Freescale PrPMC Family Members

Table 1 shows the members of the Freescale PrPMC cards supported on the Sandpoint platform, along with various features and capabilities.

Table 1. Freescale PrPMC Family Members

PrPMC Card	Ver. [1]	PrPMC Name	Cache	Flash	SDRAM	Debug	Serial	Stand-alone [2]	Notes
Altimus	X1	MPMC750 MPMC755 MPMC7400	1 MB SDR PB2	1 MB boot	SODIMM: 32 MB PC100 No ECC/Parity	Yes	No	No	3
	X2	MPMC750 MPMC755 MPMC7400	1 MB SDR PB2	1 MB boot	SODIMM: 32 MB PC100 No ECC/Parity	No			
	X3 X3B	MPMC750 MPMC755 MPMC7400 MPC7410	1 MB SDR PB2	1 MB boot 1–4 MB user	Components: >=64 MB PC133 ECC/Parity	Yes			4
Gyrus	X2	MPMC7441 MPMC7445	None	1 MB boot 1–4 MB user	Components: >=64 MB PC133 ECC/Parity	Yes	No	No	
Talos	X1	MPMC603 MPMC745	None	1 MB boot 1 MB user	SODIMM: >=64 MB PC133 No ECC/Parity	No	Yes	No	
Unity	X1	MPMC8240	None	1 MB boot	SODIMM: 32 MB PC100 No ECC/Parity	Yes	No	No	3
	X2	MPMC8240	None	1 MB boot	SODIMM: 32 MB PC100 No ECC/Parity	Yes	No	No	5
	X4	MPMC8240 MPMC8245	None	1 MB boot 1 MB user	SODIMM: >=64 MB PC133 No ECC/Parity	No	Yes	Yes	6
UnityLC	X1	MPMC8241	None	1 MB boot 1 MB user	SODIMM: 128 MB PC133 No ECC/Parity	Yes	Yes	Yes	6
Valis	X1 X2 X3	MPMC7450 MPMC7455	2 MB DDR MSUG	1 MB boot 1–4 MB user	Components: >=64 MB PC133 ECC/Parity	Yes	No	No	

1 Some board revisions were never made public and so are not listed here.

2 Standalone refers to the ability to operate without the attached Sandpoint motherboard; refer to Freescale Application Note AN2207, *Using the MPMC8245 Card in Standalone Mode*, for details.

3 Does not support local flash programming via the PROGMODE switch or ‘fu’ command.

4 Only Altimus X3B supports 2.5-V IO for the MPC7410.

5 Supports external UART on RCS1 space.

6 Supports internal UART in MPC8241/MPC8245 only.

3 Resources

Table 2 lists resources that are available on the PrPMC card. There may be other resources available, particularly IO and NVRAM on the Sandpoint motherboard. Refer to the *Sandpoint System User's Manual* for a composite memory map.

Table 2. Freescale PrPMC Resources

Start Address	End Address	Resource	Attributes	Comments
0000_0000	01FF_FFFF	SDRAM	64–128 MB 3/1/1/1	CL = 3 is bus-speed dependent. Size may be larger.
0300_0000	07FF_FFFF	SDRAM	128 MB 2/1/1/1	Larger SDRAM is usually faster.
7C00_0000	7FFF_FFFF	Flash	1–8 MB, 90 ns	Only on systems that are based on the Tundra Tsi107™ PowerPC host bridge or MPC8245, and only when switched from FF00_0000-up range.
8000_0000	FBFF_FFFF	PCI memory	I/O	PCI memory access
FC00_0000	FCFF_FFFF	EUMBBAR	I/O	Embedded utilities base
FE00_0000	FE00_FFFF	PCI IO	I/O	PCI IO access
FEC0_0000	FEDF_FFFF	PCI config.	Address	PCI configuration cycles
FEE0_0000	FEEF_FFFF		Data	
FEF0_0000	FEFF_FFFF	Interrupt ack.	—	Interrupt acknowledge broadcast
FF00_0000	FF7F_FFFF	User flash	1–4 MB, 90 ns	If 1 MB in size, there are aliased copies as noted for boot flash below.
FF80_0000	FF8F_FFFF	Boot flash	1 MB, 90 ns	Aliased copies of FFF0_0000-FFFF_FFFF due to flash smaller than maximum. Some PrPMCs may have 4 MB boot flash.
FF90_0000	FF9F_FFFF			
FFA0_0000	FFAF_FFFF			
FFB0_0000	FFBF_FFFF			
FFC0_0000	FFCF_FFFF			
FFD0_0000	FFDF_FFFF			
FFE0_0000	FFEF_FFFF			
FFF0_0000	FFFF_FFFF			Boot flash begins

Note that some PrPMC cards contain either one or two 8-bit flash memories, 1 to 4 MB in size. The Sandpoint hosts a smaller, 5-V, 512-KB flash in a PLCC32 socket, typically containing the DINK32 debug monitor. In order to boot from one of these three sources, configuration switches must be set to route the boot chip select ($\overline{\text{RCS0}}$) accordingly. See the *Sandpoint System User's Manual* for details.

4 Configuration

Each PrPMC card has several slide switches, which are used to set PLLs for the processor and the Tsi107 host bridge (except for integrated parts). In addition, switches set numerous options which are general to the PrPMC card architecture. Table 3 lists the PrPMC option switch settings.

Table 3. General PrPMC Option Switches

Setting	Definition	Default Setting	Notes
ROMLOC	Boot flash location	ON = boot from PCI flash	
MAPSEL	How processor addresses are handled	OFF = Map B/CHRP	
PMCTYPE	Select MPMC or PrPMC modes	OFF = PrPMC	1
AGENT	Select host or agent modes	OFF = host	
PROGMODE	Select programming mode	OFF = normal	
ROMSEL	Swap local flash devices	OFF = normal	
M66EN	PCI 66-MHz enable/disable	OFF = allow 66 MHz	2
SYSRST	COP reset mode selection	ON = reset entire system	3
107PLL	PCI->bus clock multiplier	Varies	
CPUPLL	Bus->core clock multiplier	Varies	

1 Must be matched with corresponding Sandpoint settings. The default is 'ON = PrPMC' for Sandpoint motherboard with serial numbers less than 6000.

2 Ignored by Sandpoint X1/X2/X3/X3B.

3 Not supported on Altimus X1 or Unity X1/X2.

Some boards have switch settings that are not described in Table 3. Generally these settings are specialized and should not be changed.

4.1 ROMLOC

All PrPMC cards support the ability to redirect the processor reset vector fetch (always from 0xFFF0_0100) to either the local boot flash or to the PCI bus boot flash. Figure 2 shows how the ROMLOC switch guides the destination for reset vector code fetches.

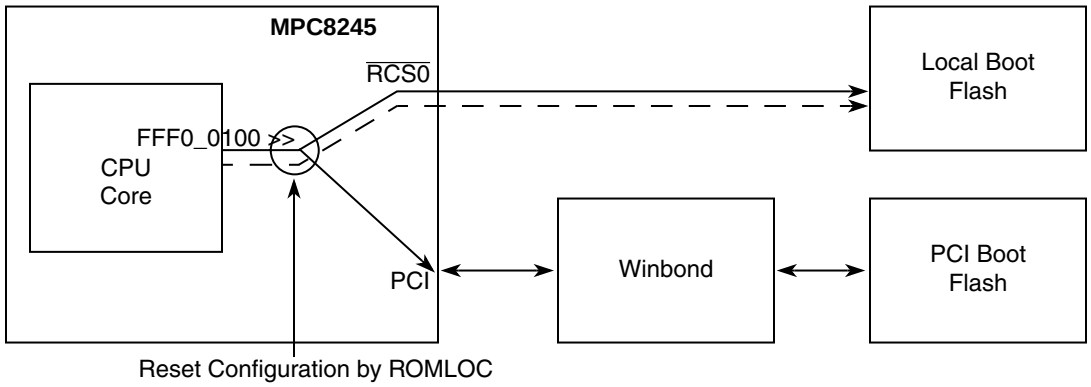

Figure 2. ROMLOC Diagram

Most Sandpoint systems use DINK or other methods to store applications and operating systems in the local flash device. By switching the ROMLOC switch, the user can select between the DINK debugger and the application under development. Table 4 shows the ROMLOC settings.

Table 4. ROMLOC Settings

Setting	Definition	Default?	Comments
ON/0	Forward addresses from 0xFF80_000 to 0xFFFF_FFFF to the PCI bus	Yes	On reset, the DINK code in the 512K 32-pin PLCC Sandpoint flash is executed.
OFF/1	Forward addresses from 0xFF80_000 to 0xFFFF_FFFF to the local bus	—	On reset, user-code on the local flash is executed. As shipped, the flash is empty.

Note that ROMLOC does not affect any other addresses.

This facility is implemented by controlling the $\overline{\text{RCS0}}$ pin during reset. Changes to this switch are only detected on system power up or system reset. More information about this configuration option can be found in the Tundra Tsi107 host bridge or the MPC824*x* user's manuals. For more information about Tundra documentation, see http://www.tundra.com.

4.2 MAPSEL

The MAPSEL switch selects between address Map B/CHRP and the older, now obsolete Map A. Address maps determine how particular address ranges are handled; whether send to memory, PCI or device interfaces.

All systems should be set to Map B unless specifically required by software. Several advanced features of the MPC8245 and the Tsi107 host bridge are not available unless the system is in Map B. Table 5 shows the MAPSEL settings.

Table 5. MAPSEL Settings

Setting	Definition	Default?	Comments
ON/0	Map A is selected	—	Not recommended
OFF/1	Map B is selected	Yes	

Refer to the Tsi107 host bridge or MPC824*x* user's manuals for details on each map selection.

4.3 PMCTYPE

The PMCTYPE switch selects between the Freescale MPMC mode or the VITA PrPMC mode. Freescale's MPMC extensions to the PMC standard were submitted to the VITA committee for standardization. As changes were made by VITA after all the MPMC cards were designed, there are two slightly different standards: VITA PrPMC and Freescale MPMC. Sandpoint X3B systems support PrPMC as the default, though Sandpoint systems may be configured to MPMC mode if the Sandpoint X3B motherboard has a serial number less than 6000.

Table 6 shows the allowed PMCTYPE settings.

Table 6. PMCTYPE Settings

Setting	Definition	Default?	Comments
ON/0	Freescale MPMC	No	
OFF/1	VITA PrPMC	Yes	Not guaranteed compatible

In addition, redirecting the PCI arbiter from the PrPMC card to the Sandpoint motherboard (specifically, the Winbond 82C553) requires configuring the Sandpoint to match the settings listed in Table 6, as shown in Table 7.

Table 7. PMCTYPE and Sandpoint AMODE Settings

PrPMC Setting	Sandpoint Serial No. 5999 or Lower AMODE Settings Allowed	Sandpoint Serial No. 6000 or Higher AMODE Settings Allowed
Freescale MPMC	AMODE = 00 (full) AMODE = 01 (partial)	AMODE = xx (Winbond)
VITA PrPMC	AMODE = 10 (Winbond)	

No other combinations are supported.

4.4 AGENT

The AGENT switch determines how a PrPMC behaves under some conditions:

- When a Sandpoint with a serial number of 5999 or lower is configured for AMODE = 10 (Winbond)
- When a Sandpoint with a serial number of 6000 or higher is used
- When installed in a PCI slot using a PMC-to-PCI adapter

In the first two conditions, the PrPMC signal $\overline{\text{SYSCON}}$ is no longer asserted to the PrPMC to indicate it must be a host and proceed with system initialization. Instead, the AGENT switch is used to select between host and agent modes. In these situations, HOST should be used. Only one PCI device, such as the PrPMC card should be designated as the PCI host.

The last condition is when a PrPMC card is installed in a PCI slot using a PMC-to-PCI adapter, such as those sold by Technobox (www.technobox.com). For peer-to-peer operation, setting the agent to free agent mode allows it to perform PCI transactions at will; this generally requires dedicated local programming in the local flash and careful system architecture. Table 8 shows the AGENT settings.

Table 8. AGENT Settings

Setting	Definition	Default?	Comments
ON/0	Agent mode	—	
OFF/1	Host mode and FreeAgent mode	Yes	Required for SPX3 AMODE = 10

Note that if the system is configured for standard PrPMC operation, the PrPMC slot is a host by default and the host mode switch is ignored.

4.5 PROGMODE

The PROGMODE switch allows users of DINK (which usually means booting from PCI) to recover access to the flash device attached to $\overline{\text{RCS0}}$. When ROMLOC is set ON, indicating the device is booting from the PCI/Sandpoint flash, the device attached to $\overline{\text{RCS0}}$ is unavailable. The PROGMODE switch moves it to $\overline{\text{RCS1}}$ (and vice-versa for dual flash PrPMCs), as illustrated in Figure 3.

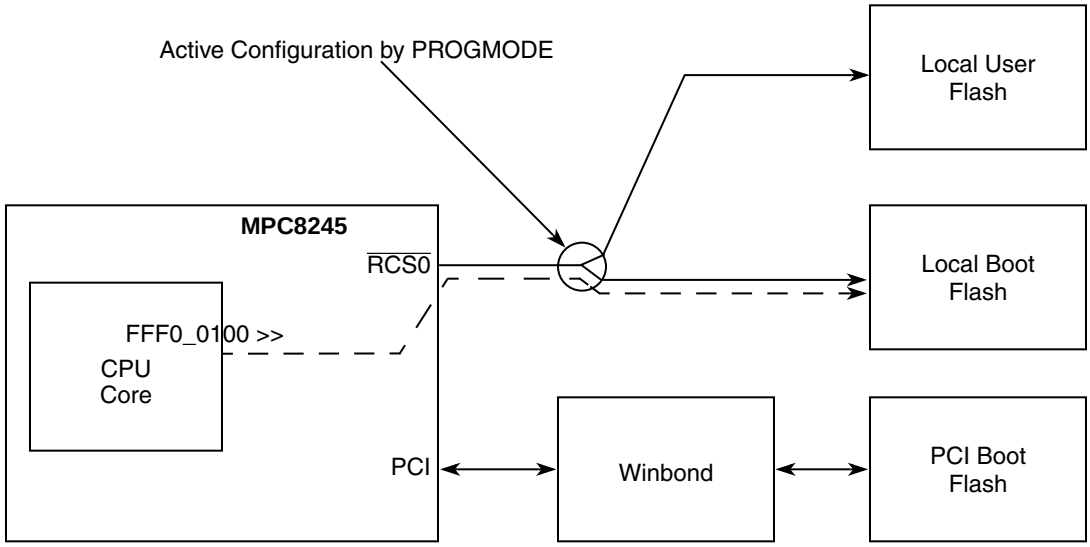

Figure 3. PROGMODE Diagram

The PROGMODE switch settings are summarized in Table 9.

Table 9. PROGMODE Settings

Setting	Definition	Default?	Comments
ON/0	ProgMode is selected: Flash at $\overline{\text{RCS0}}$ is now at $\overline{\text{RCS1}}$ Flash at $\overline{\text{RCS1}}$ is now at $\overline{\text{RCS2}}$	—	
OFF/1	ProgMode is off: Flash at $\overline{\text{RCS0}}$ is still at $\overline{\text{RCS0}}$ Flash at $\overline{\text{RCS1}}$ is still at $\overline{\text{RCS1}}$	Yes	

PROGMODE is a dynamic switch and may be toggled without powering down or resetting the system. However, do not change it during programming.

4.6 ROMSEL

The ROMSEL switch expands on the swap function of the PROGMODE switch for PrPMCs with two flash devices. When PROGMODE is off, ROMSEL exchanges the two devices attached to $\overline{\text{RCS0}}$ and $\overline{\text{RCS1}}$. If DINK is in one flash and an operating system is in the other, ROMSEL allows selecting which device is attached to the boot chip select ($\overline{\text{RCS0}}$) and is executed after reset.

Alternately, if PROGMODE is on, ROMSEL trades which of the two locals is attached to $\overline{\text{RCS1}}$, and places the other on $\overline{\text{RCS2}}$ (making both local and PCI flashes accessible), this is illustrated in Figure 4.

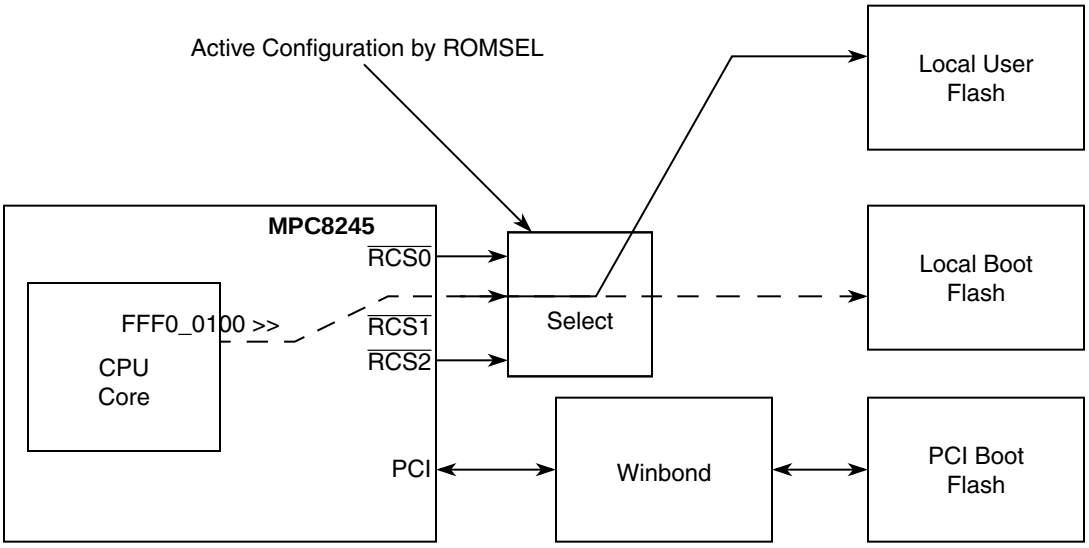

Figure 4. ROMSEL Diagram

The ROMSEL switch settings are summarized in Table 10.

Table 10. ROMSEL Settings

Setting	Definition	Default?	Comments
ON/0	If ProgMode is selected: Flash at $\overline{RCS0}$ is now at $\overline{RCS2}$ Flash at $\overline{RCS1}$ is still at $\overline{RCS1}$ If ProgMode is not selected: Flash at $\overline{RCS0}$ is now at $\overline{RCS1}$ Flash at $\overline{RCS1}$ is now at $\overline{RCS0}$	—	
OFF/1	If ProgMode is selected: Flash at $\overline{RCS0}$ is now at $\overline{RCS1}$ Flash at $\overline{RCS1}$ is now at $\overline{RCS0}$ If ProgMode is not selected: Flash at $\overline{RCS0}$ is still at $\overline{RCS0}$ Flash at $\overline{RCS1}$ is still at $\overline{RCS1}$	Yes	

Since ROMSEL literally exchanges the connections of the local flash devices and $\overline{RCS0}$/$\overline{RCS1}$, it is less important to remember which physical device is connected where. Instead, just note that changing ROMSEL ‘moves’ the boot flash to the other flash.

ROMSEL is a dynamic switch and may be toggled without powering down or resetting the system. However, do not change it during programming.

4.7 M66EN

The M66EN switch controls the M66EN PCI signal, which in turn controls whether the PCI bus is allowed to run at 66 MHz. All Sandpoint systems must run at 33 MHz, so PrPMCs shipped with Sandpoint have this switch on by default. PrPMCs used on Arcadia and other platforms may have it off.

The M66EN switch settings are shown in Table 11.

Table 11. M66EN Settings

Setting	Definition	Default?	Comments
ON/0	33 MHz only	Varies	
OFF/1	66 MHz allowed	Varies	

4.8 SYSRST

The SYSRST switch controls whether the local reset switch (for those PrPMC cards which support one), and the COP connector $\overline{\text{HRESET}}$ signal, should reset just the local CPU or should reset the CPU, the PrPMC card, and the Sandpoint system. The former allows resetting the CPU without interfering with system initialization or other CPU cards present, while the latter allows complete recovery from error conditions.

Some COP controllers expect one behavior, while some expect the other. Refer to the COP controller documentation to see which one is expected.

Generally, SYSRST is left on since the Winbond PCI/ISA controller may be confused if the PCI bus is disconnected permanently between $\overline{\text{FRAME}}$ and $\overline{\text{IRDY}}$. Enabling SYSRST prevents this from occurring. The SYSRST switch settings are shown in Table 12.

Table 12. SYSRST Settings

Setting	Definition	Default?	Comments
ON/0	COP $\overline{\text{HRESET}}$ resets entire system	Yes	
OFF/1	COP $\overline{\text{HRESET}}$ resets only CPU	—	

4.9 107PLL

The 107PLL switches (4) control the PLL settings of the Tsi107 host bridge, on those systems with a Tsi107 host bridge. This setting multiplies the PCI bus clock, which is 33 or 66 MHz, and produces the system bus clock and memory bus clock (always the same speed) which may range from 33 to 133 MHz.

The settings are directly based on the PLL table in the *Tsi107 PowerPC Host Bridge Hardware Specifications*, and is also summarized in Freescale Application Note AN2207, *Standalone Mode Conversion Guide*. Refer to either document for further details.

To set the PLL values, set the switch ON to set the PLL_CFG[0:3] pin to 0 and OFF to set it to 1. Be sure to note the orientation of the PLL_CFG table and the switches; some boards, particularly earlier ones, may number the bits from 0–3 or 3–0. Always check the configuration guide.

4.10 CPUPLL

The CPUPLL switches (4 or 5) control the PLL settings of the processor. The processor bus clock (derived from the PCICLK signal by the Tsi107 host bridge or the core logic of the MPC824*x*) is multiplied by the PLL settings to produce the core clock speed, currently anywhere from 100 MHz to 1 GHz. Each CPU has a different encoding for the PLL switches.

The settings are directly based on the PLL table in the corresponding processor hardware specification, and is also summarized in Freescale Application Note AN2207, *Standalone Mode Conversion Guide*. Refer to either document for further details.

To set the PLL values, set the switch ON to set the PLL_CFG[0:3]/PLL_CFG[0:4] pin to 0 and OFF to set it to 1. Be sure to note the orientation of the PLL_CFG table and the switches; some may appear backwards as drawn on the configuration guide.

5 Flash Configuration

The previous sections have highlighted the flexibility in using and allocating several flash devices among the chip selects provided by the Tsi107 host bridge and MPC824*x* members. Table 13 summarizes the available options.

Table 13. Flash Configuration Settings

ROMLOC	PROGMODE	ROMSEL	FF80_0000 ... FFFF_FFFF	FF00_0000 ... FF7F_FFFF	7C00_0000 ... 7FFF_FFFF [1]	Notes
ON	ON	ON	PCI flash	Local user flash	Local boot flash	[2]
ON	ON	OFF	PCI flash	Local boot flash	Local user flash	
ON	OFF	ON	PCI flash	Local boot flash	N/A	[2]
ON	OFF	OFF	PCI flash	Local user flash	N/A	
OFF	ON	ON	N/A	Local user flash	Local boot flash	[2, 3]
OFF	ON	OFF	N/A	Local boot flash	Local user flash	[3]
OFF	OFF	ON	Local user flash	Local boot flash	N/A	[2]
OFF	OFF	OFF	Local boot flash	Local user flash	N/A	

[1] Not supported on the MPC8240.
[2] Not supported on the Unity X2 or earlier.
[3] System will not start if ROMLOC = OFF and PROGMODE = ON.

6 Local Flash Programming

All PrPMC cards support the ability to program the local boot and user flash devices under DINK32, even when booting from the PCI flash and $\overline{\text{RCS0}}$-controlled memory is normally unavailable. This facility is handled via the PROGMODE + ROMSEL switches, and is documented in more detail in Freescale Application Note AN1806, *Initializing Blank Flash Devices*.

6.1 Local Flash Programming via DINK32

Sandpoint systems are generally configured to boot from the PCI-hosted 512K 5-V flash. This allows the local flash devices to be reserved for user code. To program such code into the local flash devices, follow these steps:

1. Download the binary or S-record image to be programmed into main memory.

```
DINK32 [MPC8245] {3} >> sb -k 115200
DINK32 [MPC8245] {4} >> dl -k -b -o 100000
```

```
DINK32 [MPC8245] {5} >>
```

2. Set the PROGMODE switch to ON. It is not necessary to turn the power off to do this first, though the chassis needs to be opened.
3. Issue the flash utility command ‘fu.’ The first address is the source address, the address to which the image was downloaded in step 1.

   The second address is the base address (or portion) of the flash when in PROGMODE. In PROGMODE, boot flash moves from the default address range [0xFF800000–0xFFFFFFFF] to the alternate address range [0xFF000000–0xFF7FFFFF].

   The third parameter is the size; enter the actual size rounded up to an 8-byte boundary.

   ```
   DINK32 [MPC8245] {3} >> fu -l 100000 ff000000 FFF00
   ```

   Upon completion with no errors, the code can be examined or used at 0xFF00_0000 and up, except for MPC8240 and MPC8245 systems running DINK 12.3 or earlier. Those systems configure the alternate flash to be 64-bits, which is the only size supported on the MPC8240. The flash utility handles the missing 56 bits, and when displayed the source image will appear 1 byte every 8 bytes. This code cannot be executed until restored to the boot flash address range.

   Starting with DINK 13.0, the MPC8245 sets $\overline{\text{RCS1}}$ to 8 bits and programs it correspondingly. The DBUS_SIZ(2) bit can be set using the ‘RD NB FC’ command to force it (MPC8245 only).
4. Set the PROGMODE switch to OFF. Again, it is not necessary to turn the power off to do this first, though the chassis needs to be opened.
5. Set the ROMLOC switch to OFF.
6. Press the RESET button on the chassis or motherboard. The programmed code will be executed out of reset, instead of DINK32.

If the programmed code does not appear to work, make sure that the code performs system initialization. Using the above sequence, DINK32 does not run at all, nor is there any BIOS to perform system setup—it is, instead, the responsibility of the boot firmware. Some firmware, such as QNX and VxWorks, do perform this step. Others, such as MontaVista Linux, expect DINK to do a great deal of setup for it. For the latter case, it is best to skip step 5 above. This allows DINK to start, then the programmed code can be executed from flash via ‘go ff000000.’

6.2 Local Flash Programming via COP/JTAG

When programming via an external COP/JTAG controller, the extra features provided by the PROGMODE and ROMSEL switches are not needed. Instead, the best way to configure the system is to set the following switches as shown in Table 14.

Table 14. COP/JTAG Flash Programming Settings

ROMLOC	PROGMODE	ROMSEL	FF80_0000 ... FFFF_FFFF	FF00_0000 ... FF7F_FFFF	7C00_0000 ... 7FFF_FFFF
OFF	OFF	OFF	Local boot flash	Local user flash	N/A

DINK is not involved in this setup; the COP controller is solely responsible for initializing the system and performing the flash programming algorithm. Flash is accessed in exactly the same manner it will be used by the target software—that is, there is a boot flash at 0xFFF0_0000 and a user flash at 0xFF00_0000.

6.3 Transferring DINK to Local Flash

Sandpoint systems have a PCI-hosted 512K, 5-V flash which contains the DINK debugger. Occasionally, new versions of DINK are released with enhanced functions and bug fixes. The ‘fu -h’ function of the flash utility allows programming this flash.

Since this flash does not contain any backup images, if an error occurs during the upgrade procedure, the DINK flash will be lost and the ability to use the system will be severely limited. Only an external programming device (such as a DataIO machine) or the COP header can be used to recover the system.

For this reason, it is highly recommended that DINK be copied to the local flash prior to performing any DINK upgrade procedures. To do this, follow these steps:

1. Set the PROGMODE switch to ON. It is not necessary to turn the power off to do this first, though the chassis needs to be opened.
2. Issue the flash utility command ‘fu,’ using the start of the boot code as the starting address.

```
DINK32 [MPC8245] {3} >> fu -l FFF00000 FF700000 FFF00
```

3. Set the PROGMODE switch to OFF. DINK is safely backed up in the local boot flash.

Now, if the DINK upgrade facility fails for any reason and the contents cannot be used, you may:

1. Set the ROMLOC switch to OFF.
2. Press the RESET button on the chassis or motherboard. The local flash copy of DINK is executed out of reset, instead of DINK32.

Note that due to interactions between the memory maps of the Tsi107 host bridge or the MPC8245 and the Winbond 82C553, the Sandpoint 512K host flash cannot be updated when DINK is running from the local flash.

7 Operating as an Agent

PrPMC cards have the ability to operate as an agent in a PCI backplane, such as the one on Sandpoint. This requires purchasing a PMC->PCI adapter board, such as Technobox Model No. 2938 or equivalent (refer to http://www.technobox.com/).

When operating as an agent, the PrPMC card reverts to non-SYSCON/non-MONARCH mode and does not collect interrupts. To disable the on-PrPMC arbitration, set the board type to VITA mode and agent mode to agent.

On startup, DINK32 configures any PrPMC that is detected in a slot and is based on MPC824*x* or the Tsi107 host bridge, and enables it to perform PCI access cycles. This allows the cards to boot from the PCI-hosted DINK32, or to access Sandpoint motherboard-based IO (for local flash programs).

When the PMC/PCI cards boot DINK from the PCI flash, they will configure themselves to communicate over COM2 rather than COM1. However, since all boards will do this, only one PrPMC can be used in this manner.

8 Standalone Mode

As discussed in Freescale Application Note AN2207, *Using the MPMC8245 Card in Standalone Mode*, some PrPMC cards can be operated in a standalone manner; that is, without being attached to the Sandpoint motherboard. Refer to the application note for more details.

9 References

Useful reference documentation is shown in Table 15.

Table 15. Reference Documentation

Title	Location
Using the MPMC8245 Card in Standalone Mode (AN2207/D)	http://e-www.freescale.com/brdata/PDFDB/docs/AN2207.pdf
Sandpoint System User's Manual	http://e-www.freescale.com/collateral/SPX3UM.pdf
Sandpoint/MPMC Website	http://e-www.freescale.com/webapp/sps/site/prod_summary.jsp?code=SANDPOINTX3
Tsi107™ PowerPC Host Bridge User Manual	http://www.tundra.com

For reference purposes, many designers may refer to the application notes and example/reference designs available on the Freescale website.

10 Revision History

Table 16 provides a revision history for this application note.

Table 16. **Document Revision History**

Rev. No.	Substantive Change(s
0	Initial release.
1	Incorporated comments from IE and MO.
	Added programming FAQ.
	Updated template and added PowerPC trademark information.
1.1	Nontechnical reformatting.

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