Application Note

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Connecting Multiple MSC8102 Devices on a System Bus

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This application note describes how to connect up to eight MSC8102 devices in a system, each configured differently. No additional glue logic is needed for reset configuration. In a typical multi-MSC8102 system, one MSC8102 device acts as the configuration master and all other MSC8102 devices act as configuration slaves. The configuration master reads the various configuration words from EPROM and uses them to configure itself as well as the configuration slaves.

To configure a multiple-MSC8102 system, you must complete the following tasks:

- Connect the CNFGS, $\overline{\text{RSTCONF}}$, and $\overline{\text{HRESET}}$ signals properly.
- Connect the 60x-compatible data bus between all MSC8102 devices.
- Configure the Hard Reset Configuration Word (HRCW) for all MSC8102 devices at the correct addresses.

1 Connecting the CNFGS and $\overline{\text{RSTCONF}}$ Pins

The reset mode determines the behavior of the MSC8102 devices during a reset configuration write through the system bus and is specified by the value of the CNFGS and $\overline{\text{RSTCONF}}$ input pins when $\overline{\text{PORESET}}$ is deasserted. During system bus configuration, the $\overline{\text{RSTCONF}}$ input of the configuration master is tied to ground, and the $\overline{\text{RSTCONF}}$ inputs of the other devices connect to the high-order address bits of the configuration master, as shown in **Table 1**.

Table 1. $\overline{\text{RSTCONF}}$ Connections in Multi-MSC8102 Systems

Configured Device	$\overline{\text{RSTCONF}}$ Connection
Configuration master	GND
First configuration slave	A0
Second configuration slave	A1
Third configuration slave	A2
Fourth configuration slave	A3
Fifth configuration slave	A4
Sixth configuration slave	A5
Seventh configuration slave	A6

2 Assigning Hard Reset Configuration Word Addresses

Table 1 shows the addresses used to configure the various MSC8102 devices. The values are always read on byte lane D[0–7], regardless of the port size.

Table 2. Configuration EPROM Addresses

Configured Device	Byte 0 Address	Byte 1 Address	Byte 2 Address	Byte 3 Address
Configuration master	0x00	0x08	0x10	0x18
First configuration slave	0x20	0x28	0x30	0x38
Second configuration slave	0x40	0x48	0x50	0x58
Third configuration slave	0x60	0x68	0x70	0x78
Fourth configuration slave	0x80	0x88	0x90	0x98
Fifth configuration slave	0xA0	0xA8	0xB0	0xB8
Sixth configuration slave	0xC0	0xC8	0xD0	0xD8
Seventh configuration slave	0xE0	0xE8	0xF0	0xF8

The configuration master reads a value from address 0x00 and then reads a value from addresses 0x08, 0x10, and 0x18. These four bytes form the configuration word of the configuration master, which then proceeds to read the bytes that form the configuration word of the first slave device. The master drives the whole configuration word on D[0–31] and toggles its A0 address line. Each configuration slave uses its $\overline{\text{RSTCONF}}$ input as a strobe for latching the configuration word during $\overline{\text{HRESET}}$ assertion time. Thus, the first slave whose $\overline{\text{RSTCONF}}$ input connects to the master A0 output latches the word driven on D[0–31] as its configuration word. Then, the master continues to configure all MSC8102 devices in the system. The configuration master always reads eight configuration words, regardless of the number of MSC8102 devices in the system.

Figure 1 shows a multi-device configuration. In this system, the configuration master initially reads its own configuration word. It then reads other configuration words and drives them to the configuration slaves by asserting $\overline{\text{RSTCONF}}$. As **Figure 1** shows, this complex configuration is done without additional glue logic. The configuration master controls the whole process by asserting the EPROM control signals and the system address signals as needed. Connecting all the $\overline{\text{HRESET}}$ signals of the configuration master and all the configuration slaves ensures that all MSC8102 devices exit reset together.

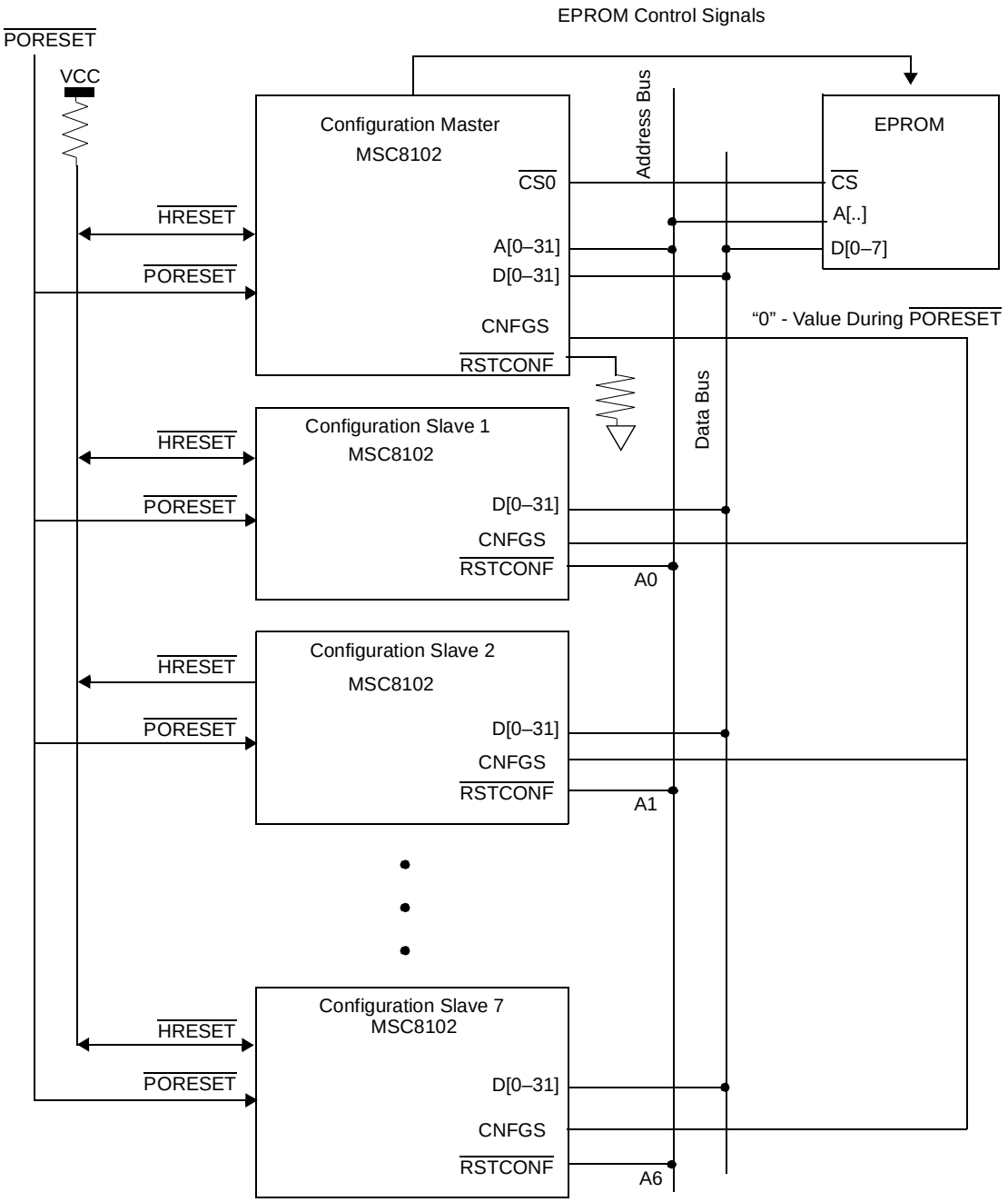

Figure 1. Configuring Multiple MSC8102 Devices

3 Connecting Two MSC8102 Devices

The 60x-compatible bus can be configured as a 64-bit data bus or as a 32-bit data bus. The system configured can use either bus width. The following examples show two MSC8102 devices connected via the 60x-compatible system bus with a 64-bit data bus width and with a 32-bit data bus width.

3.1 Hard Reset Configuration Word, 64-Bit System Bus Width

Hard Reset Configuration Word of Configuration Master

	Bit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	EARB	EXMC	INT OUT	EBM	BPS		SCDIS	ISPS	IRPC	—	DPPC		NMI OUT	ISBSEL		
Value	0	0	1	1	0	0	0	0	1	0	1	1	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	—	BBD	MMR	—	TTPC	CS5 PC	TCPC		LTLEND	PPCLE	—	DLLDIS	MODCK_H			—
Value	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0

HRCW for the configuration master is: 0x30B00A00.

Hard Reset Configuration Word of Configuration Slave

	Bit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	EARB	EXMC	INT OUT	EBM	BPS		SCDIS	ISPS	IRPC	—	DPPC		NMI OUT	ISBSEL		
Value	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	—	BBD	MMR	—	TTPC	CS5 PC	TCPC		LTLEND	PPCLE	—	DLLDIS	MODCK_H			—
Value	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0

HRCW for the configuration slave is: 0xF0010A00.

3.2 Hard Reset Configuration Word, 32-Bit System Bus Width

Hard Reset Configuration Word of Configuration Master

	Bit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	EARB	EXMC	INT OUT	EBM	BPS		SCDIS	ISPS	IRPC	—	DPPC		NMI OUT	ISBSEL		
Value	0	0	1	1	1	1	0	1	1	0	1	1	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	—	BBD	MMR	—	TTPC	CS5 PC	TCPC		LTLEND	PPCLE	—	DLLDIS	MODCK_H			—
Value	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0

HRCW for the configuration master is: 0x3DB00A00.

Hard Reset Configuration Word of Configuration Slave

	Bit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	EARB	EXMC	INT OUT	EBM	BPS		SCDIS	ISPS	IRPC	—	DPPC		NMI OUT	ISBSEL		
Value	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	1

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	—	BBD	MMR	—	TTPC	CS5 PC	TCPC		LTLEND	PPCLE	—	DLLDIS	MODCK_H			—
Value	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0

HRCW for the configuration slave is: 0xFD010A00.

3.3 System Configurations

The following configurations apply to both examples presented in this section:

- The EPROM connects to the $\overline{\text{CS0}}$ signal of the configuration master.
- The CLKOUT of the configuration master connects to the DLLIN of the configuration master and the configuration slave.
- A0 of the configuration master connects to $\overline{\text{RSTCONF}}$ of the configuration slave.
- TT1 connects between the two MSC8102 devices.
- SDRAM connects to $\overline{\text{CS5}}$ of the configuration master. The configuration slave can also access the SDRAM. Configure BR5 and OR5 of the configuration slave the same way as for the configuration master, except with the external memory controller set to on.
- HRCW[IRPC] = 1. Configure $\overline{\text{IRQ}}$/BADDR as BADDR, which is needed for the connection to the SDRAM.

- HRCW[TCPC] = 1. For the Transfer Code pin, configure TC/BNKSEL as BNKSEL, which is needed for the connection to the SDRAM.
- The Arbiter signals ($\overline{\text{BG}}$, $\overline{\text{BR}}$, and $\overline{\text{DBG}}$ are as follows (HRCW[DPPC] = 11):
  - $\overline{\text{IRQ1}}$/DP2/$\overline{\text{DACK2}}$/$\overline{\text{EXT\_BG2}}$ is configured as $\overline{\text{BG}}$,
  - DP0/DREQ1/$\overline{\text{EXT\_BR2}}$ is configured as $\overline{\text{BR}}$,
  - $\overline{\text{IRQ2}}$/DP2/$\overline{\text{DACK2}}$/$\overline{\text{EXT\_DBG2}}$ is configured as $\overline{\text{DBG}}$.

  They are connected to the configuration master.
- HRCW[EARB] = 1. External arbitration is assumed for the configuration slave.
- HRCW[EXMC] = 1. External memory controller is assumed for the configuration slave.
- HRCW[EBM] = 1. 60x-compatible bus mode.
- HRCW[INT OUT] = 1. The $\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$ pin is configured as $\overline{\text{INT\_OUT}}$.
- For a 64-bit data bus size, the following values apply:
  - HRCW[BPS] = 00. 64-bit port size.
  - HRCW[ISPS] = 0. The MSC8102 device acts as a 64-bit slave to give external masters access to its internal space.
- For a 32-bit data bus size, the following values apply:
  - HRCW[BPS] = 11. 32-bit port size
  - HRCW[ISPS] =1. The MSC8102 device acts as a 32-bit slave to give external masters access to its internal space.

NOTES:

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