Application Note

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Connecting an MSC8102 TDM to an MSC8101 Device

by Yael Kahil

CONTENTS

The MSC8102 time-division multiplex (TDM) interface allows many devices to communicate over a single bus by using channels that have individual time slots shared in a larger transmit frame. One device drives the bus (transmit) for each channel time slot. Each active device drives its active transmit channels and samples its active receive channels. It is the system designer's responsibility to ensure that there is no conflict in transmit channel allocation.

The TDM interface consists of four identical and independent TDM modules, each supporting 256 channels running at up to 50 Mbps with 2, 4, 8, and 16-bit word sizes. The TDM bus connects gluelessly to most T1/E1 frames as well as to common buses such as the H.110, SCAS, and MVIP.

This document presents an example in which one MSC8102 TDM is connected to the multi-channel controllers (MCCs) of an MSC8101 device. The application note first describes the physical interface between the MSC8102 and MSC8101 devices and then explains how to configure one MSC8102 TDM module and the MSC8101 MCCs.

1 MSC8102 TDM to MSC8101 Interface

A general TDM interface is implemented with four 8-bit channels. The MSC8102 TDM clocks are always driven from an external source. In our example, the MSC8101 baud-rate generator 1 output (BRG1O) supplies the clock to the MSC8102 and MSC8101 devices. The MSC8102 TDM0 generates the frame sync signal. **Figure 1** shows the connection between the MSC8102 and MSC8101 devices.

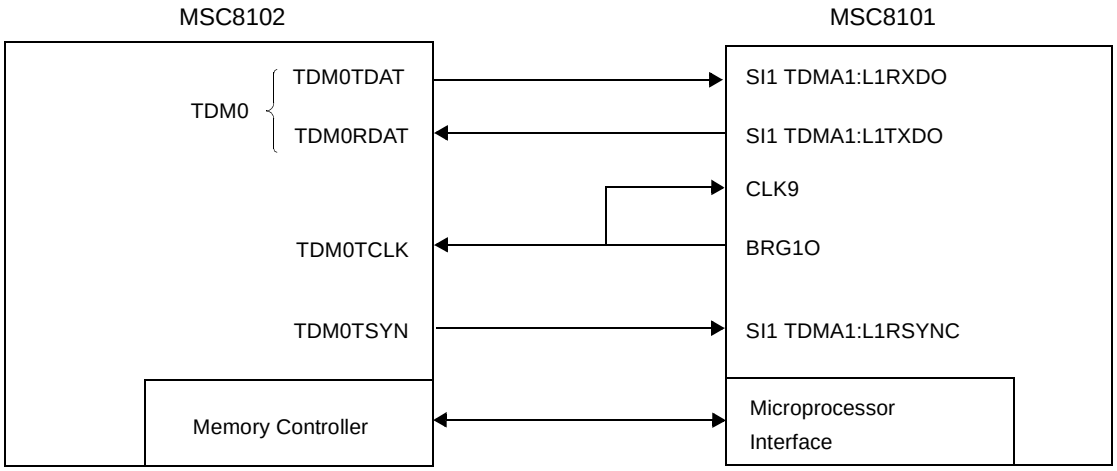
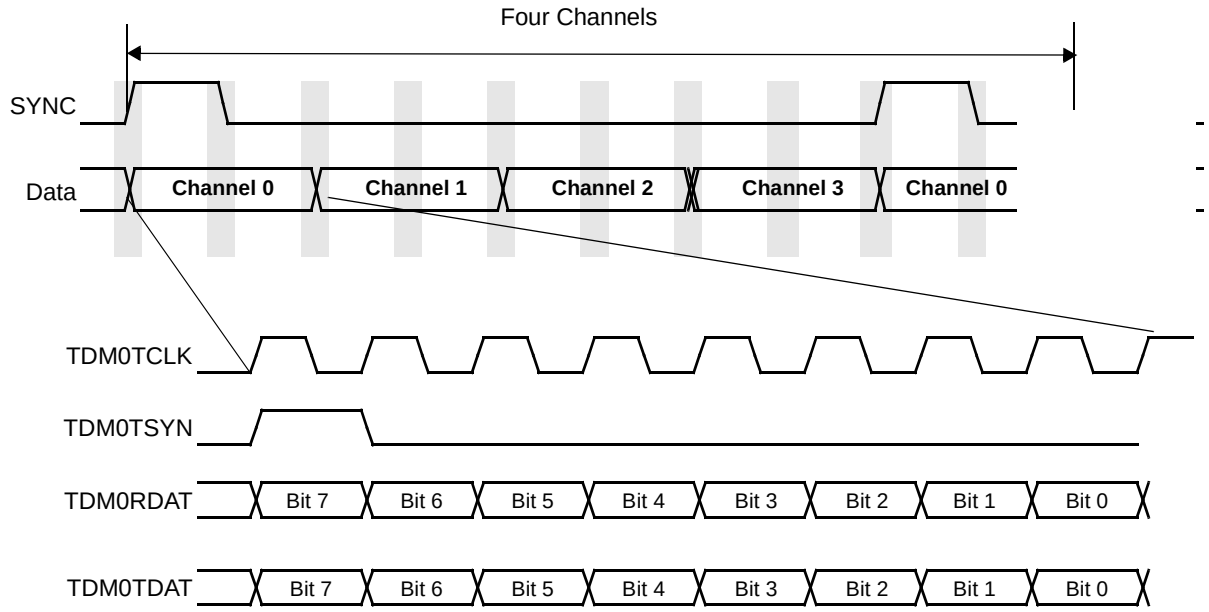


Figure 1. MSC8102 to MSC8101 Connections

Figure 2 shows a timing diagram for the interface between the MSC8102 and MSC8101. The TDM frame supports four 8-bit channels.



Note: The TDM0TDATA and TDM0RDAT ports function as data links.

Figure 2. MSC8102 to MSC8101 Interface

2 Configuring the MSC8102 TDMs

The overall steps in initializing an MSC8102 TDM are as follows:

1. Initialize the configuration registers to define the basic interface between the external device and the MSC8102 TDM.
2. Initialize the channel parameter registers to determine the channel type (A-law, µ–law, or transparent) and the buffer location of each channel.

   The channel parameter register values can change during TDM operation.
3. Initialize the control registers.
4. Clear the event registers (TDMxRER, TDMxTER).
5. Configure the external interface:

   a. Set up the parallel I/O pins.

   b. Enable the TDM.

This section defines the register settings used to complete these steps. For the example presented here, the MSC8102 TDM transfers data to MSC8101 via the TDM0TDAT port, and it receives data via TDM0RDAT. The receiver and transmitter of TDM0 share sync and clock signals, and the sync signal is generated by TDM0 of the MSC8102 device. The receive and transmit buffers of MSC8102 TDM0 are located in the L1 memory of the SC140 core 0 (CORE0), and the buffer size is 128 bytes. All the data buffers are contiguous in memory

Table 1. TDM0 Interface Register Settings

Bit Setting	Description
TDM0GIR[28–31]:RTSAL] = 0x4	The receive and transmit have a common clock and sync. The TDM receives one data link (TDM0RDAT) and transmits one data link (TDM0TDAT).
TDM0GIR[27]:CTS = 0x0	TDM0 does not share signals with the other TDM modules
TDM0RIR[26–27]:RFSD = 0x0	There is no clock delay between the first bit of the receive frame and the synchronization signal.
TDM0RIR[28]:RSL = 0x0	TDM0TSYN is an active high signal (TDM0SYN is common for receive and transmit).
TDM0RIR[29]:RDE = 0x0	The receive data signal (TDM0RDAT) samples at the falling edge of TDM0TCLK.
TDM0RIR[30]:RFSE = 0x0	The TDM0TSYN signal is sampled at the rising edge of TDM0TCLK.
TDM0RIR[31]:RRDO = 0x0	The MSB bit is received first.
TDMTTIR[26–27]:TFSD = 0x1	There is no clock delay between the first bit of the transmit frame and the synchronization signal.
TDM0TIR[28]:TSL = 0x0	TDM0TSYN is an active high signal (TDM0SYN is common for receive and transmit).
TDM0TIR[29]:TDE = 0x0	The transmit data signal (TDM0TDAT) drives out on the rising edge of TDM0TCLK.
TDM0TIR[30]:TFSE = 0x0	The TDM0TSYN signal is sampled on the rising edge of TDM0TCLK.
TDM0TIR[31]:TRDO = 0x0	The MSB bit is transmitted first.
TDM0TIR[18]:TSO = 0x0	TDM0TSYN is an output
TDM0TIR[21]:SOE = 0x1	TDM0TSYN is driven out on the falling edge of the transmit clock.
TDM0TIR[20]:SOL = 0x0	The TDM0TSYN signal is active during one bit transmission.
TDM0TIR[19]:TAO = 0x1	Data is always transmitted out.
Register Setting Summary	TDM0GIR = 0x00000004, TDM0RIR = 32x00010004, TDM0TIR = 32x00012410

Table 2. TDM0 Frame Parameter Register (TDM0RFP/TDM0TFP) Settings

Bit Setting	Description
TDM0RFP[8–15]:RNCF = 0x03	Four receive channels (four channels per data link).
TDM0RFP[21–23]:RCDBL = 0x1	Receive data buffer latency is 128 bits.
TDM0RFP[26–29]:RCS = 0x7	Receive channel size is 8 bits.
TDM0RFP[30]:RT1 = 0x0	The receive frame is not a T1 frame but an E1 frame.
TDM0RFP[31]:RUBM = 0x0	The receiver operates in regular mode.
Register Setting Summary:	TDM0RFP = 32x0007011c,TDM0TFP = 32x0007011c Note: TDM0RFP is identical to TDM0TFP because the receive and transmitter operate in shared mode.

The data buffers of a TDM channel can be located in the L1 memory of the SC140 cores and in M2 memory. The location of each data buffer is independent and is indicated in the Receive/Transmit Channel Parameter Registers (RCPR_X). The data buffer size is identical for all receive channels belonging to a TDM module and is indicated by the TDMx[8–31]:RDBS field. The transmit buffer size is also identical for all the transmit channels belonging to a TDM module and is indicated by the TDMxTDBS[8–31]:TDBS field. The receive data buffer base address is a function of the following:

- Receive Global Base Address. TDMxRGBA[16–31]:RGBA field.

- Receive Channel Data Base Address. TDMxRCPRn[8–31]:RCDBA field.

  Receive data buffer n =RGBA >> 16 + RCDBA

The transmit data buffer base address is a function of the following:

- Transmit Global Base Address. TDMxTGBA[16–31]:TGBA field.
- Transmit Channel Data Base Address. TDMxTCPRn[8–31]:TCDBA field.

  Transmit data buffer n =TGBA >> 16 + TCDBA

Note: The data buffer base address is in the local bus address space.

For example, if the transmit data buffer of channel *n* is located at the first byte of M2 (address at the local bus space = 0x2000000), then the following is true:

- Transmit Global Base Address. TDMxTGBA[16–31]:TGBA = 0x200.
- Transmit Channel Data Base Address. TDMxTCPRn[8–31] = 0x0.

Table 3. TDM0 Data Buffer Register Settings

Bit Setting	Description
TDM0RDBS[8–31]:RDBS = 0x00007F	The receive data buffer size is 128 bytes.
TDM0TDBS[8–31]:TDBS = 0x00007F	The transmit data buffer size is 128 bytes.
TDM0RGBA[16–31]:RGBA = 0x0208	The receive global base address points to the first byte of the L1 memory, SC140 core 0.
TDM0TGBA[16–31]:TGBA = 0x0208	The transmit global base address points to the first byte of the L1 memory, SC140 core 0.
Register Setting Summary:	TDM0RDBS = 0x0000007F, TDM0TDBS = 0x0000007F, TDM0RGBA = 0x00000208,TDM0TGBA = 0x00000208

Table 4. Receive/Transmit Channel Parameter Register Settings

Bit Setting	Description
TDM0RCPR0 = 0x80000000	The receive data buffer of channel 0 is located at an offset of 0 bytes (refer to the TDMx Receive Global Base Address Register, TDMxRGBA[16–31]:RGBA field). The data buffer address is 0x2080000 (local memory address space).
TDM0RCPR1 = 0x80000080	The receive data buffer of channel 1 is located at an offset of 128 bytes (refer to the TDMxRGBA[16–31]:RGBA field). The data buffer address is 0x2080080 (local memory address space).
TDM0RCPR2 = 0x80000100	The receive data buffer of channel 2 is located at an offset of 256 bytes (refer to the TDMxRGBA[16–31]:RGBA field). the data buffer address is 0x2080100 (local memory address space).
TDM0RCPR3 = 0x80000180	The receive data buffer of channel 3locate at an offset of 384 bytes (refer to the TDMxRGBA[16–31]:RGBA field). The data buffer address is 0x2080180 (local memory address space).
TDM0TCPR0 = 0x80000200	The transmit data buffer of channel 0 is located at an offset of 512 bytes (refer to the TDMxTGBA[16–31]:TGBA field). The address of transmit channel 0 is 0x2080200 (local memory address space).
TDM0TCPR1 = 0x80000280	The transmit data buffer of channel 1 is located at an offset of 640 bytes (refer to the TDMxTGBA[16–31]:TGBA field). The address of transmit channel 1 is 0x2080280 (local memory address space).

Table 4. Receive/Transmit Channel Parameter Register Settings (Continued)

Bit Setting	Description
TDM0TCPR2 = 0x80000300	The transmit data buffer of channel 2 is located at an offset of 768 bytes (refer to the TDMxTGBA[16–31]:TGBA field). The address of transmit channel 2 is 0x2080300 (local memory address space).
TDM0TCPR3 = 0x80000380	The transmit data buffer of channel 3 is located at an offset of 896 bytes (refer to the TDMxTGBA[16–31]:TGBA field). The address of transmit channel 3 is 0x2080380 (local memory address space).
Note: All the receive and transmit channels are active and transparent.	

Table 5. Threshold Register Settings

Bit Setting	Description
TDM0TDBFT[8–31]:TDBFT = 0x000038	The transmit first threshold interrupt is generated when the first half of the data buffer is empty.
TDM0TDBFT[8–31]:TDBFT = 0x000078	The transmit second threshold interrupt is generated when the second half of the data buffers is empty.
TDM0RDBFT[8–31]:RDBFT = 0x000038	The receive first threshold interrupt is generated when the first half of the data buffer is full.
TDM0RDBFT[8–31]:RDBFT] = 0x000078	The receive second threshold interrupt is generated when the second half of the data buffer is full.
Register Setting Summary:	TDM0RDBFT = 0x00000038,TDM0RDBST = 0x00000078, TDM0TDBFT = 0x00000038,TDM0TDBST = 0x00000078

Table 6. Parallel I/O Port Registers

Register Setting	Description
PSOR = 32 × 07B00000	The TDM0TSYN, TDM0TDAT, TDM0TDAT, TDM0RDAT, and TDM0RSYN ports are dedicated peripheral ports (option 2).
PODR = 32 × 0	All the I/O ports are actively driven as outputs.
PDIR = 32 × 0	All the I/O ports counteract as inputs (the TDM determines the direction of the port).
PAR = 32 × 07F00000	The TDM0TSYN, TDM0TDAT, TDM0TDAT, TDM0RDAT, TDM0RSYN, and TDM0TCLK ports are dedicated peripheral ports.

Before activating the TDM, you must enable the TDM0 interrupts by setting the TDM0RIER and TDM0TIER registers to a value of 0xF. Also, you must clear the event registers TDM0RER and TDM0TER by writing a value of 0xF to these registers.

Table 7. TDM0 Activation Register Settings

Register Setting	Description
TDM0RCR = 0x00000001	Enable the TDM0 receiver
TDM0TCR = 0x00000001	Enable the TDM0 transmitter

3 Configuring the MSC8101 MCCs

The MSC8101 CPM contains two MCC blocks, each providing up to 128 full-duplex serial data channels routed through the programmable time-slot assigner (TSA) in the serial interfaces, SI1 and SI2. Target applications of the MCC are mainly TDM interfaces. MCC channels are individually configured to handle either transparent or HDLC protocols. For each channel, the serial interface and its associated RAM (SIRAM) control the routing of TDM data through each of the four TDM interfaces to an external network. The overall steps in initializing the MCC are as follows:

1. Configure the channels:
   a. Initialize the buffer descriptors (BDs)
   b. Set up the global parameters.
   c. Set up the MCC control registers
   d. Set up the channel-specific parameters.
   e. Initialize the interrupt queues.
2. Select the TSA channel route to the TDM time slot:
   a. Program the serial interface RAM (SIRAM)
   b. Set up the baud-rate generation.
3. Configure the external interface:
   a. Set up the parallel I/O pins.
   b. Enable the TDM.

The subsections that follow discuss each of these steps.

3.1 Buffer Description Tables

The buffer description tables define the Tx and Rx data buffer locations and maintain status information on receive and transmit frames. In our example, the buffer description tables reside in L1 memory at address 0x10000. Each channel has two 64 byte buffers. All channel BDs are contiguous in memory. **Table 8** and **Table 10** describe the receive and transmit buffer description tables. Note that RXDBPTR is a 4 byte field in local bus address space.

Table 8. Receive Buffer Description Table

Address (Two-Byte Field)		DL (Two-Byte Field)	RXDBPTR	Description
0x10000	0x9000	0x0	0x2012000	First buffer description of channel 0. The buffer resides at address 0x12000 in L1 memory.
0x10008	0xB000	0x0	0x2012040	Second buffer description of channel 0. The buffer resides at address 0x12040 in L1 memory.
0x10010	0x9000	0x0	0x2012080	First buffer description of channel 1. The buffer resides at address 0x12080 in L1 memory.
0x10018	0xB000	0x0	0x20120C0	Second buffer description of channel 01. The buffer resides at address 0x120C0 in L1 memory.
0x10020	0x9000	0x0	0x2012100	First buffer description of channel 2. The buffer resides at address 0x12100 in L1 memory.
0x10028	0xB000	0x0	0x2012140	Second buffer description of channel 3. The buffer resides at address 0x12140 in L1 memory.

Table 8. Receive Buffer Description Table (Continued)

Address (Two-Byte Field)		DL (Two-Byte Field)	RXDBPTR	Description
0x10030	0x9000	0x0	0x2012180	First buffer description of channel 3. The buffer resides at address 0x12180 in L1 memory.
0x10038	0xb000	0x0	0x20121C0	Second buffer description of channel 3. The buffer resides at address 0x121C0 in L1 memory.

Table 9. Transmit Buffer Description Table

Address (2 Byte Field)		DL (2 Byte Field)	RXDBPTR	Description
0x11000	0x9000	0x40	0x201A000	First buffer description of channel 0. The buffer resides at address 0x1A000 in L1 memory.
0x11008	0xB000	0x40	0x201A040	Second buffer description of channel 0. The buffer resides at address 0x1A040 in L1 memory.
0x11010	0x9000	0x40	0x201A080	First buffer description of channel 1. The buffer resides at address 0x1A080 in L1 memory.
0x11018	0xB000	0x40	0x201A0c0	Second buffer description of channel 01. The buffer resides at address 0x1A0C0 in L1 memory.
0x11020	0x9000	0x40	0x201A100	First buffer description of channel 2. The buffer resides at address 0x1A100 in L1 memory.
0x11028	0xB000	0x40	0x201A140	Second buffer description of channel 3. The buffer resides at address 0x1A140 in L1 memory.
0x11030	0x9000	0x40	0x201A180	First buffer description of channel 3. The buffer resides at address 0x1A180 in L1 memory.
0x11038	0xB000	0x40	0x201A1C0	Second buffer description of channel 3. The buffer resides at address 0x1A1C0 in L1 memory.

3.2 Global Parameters

Each MCC has a set of global parameters in the DPRAM that are common to all channels within that MCC. The global parameters define a base for the transmit and receive circular BD tables, the maximum buffer size, and interrupt queue adresses.The global parameters provide the common functionality for all active channels on each MCC. The MCC1 global parameter resides in the DPRAM at address 0x8700. **Table 10** describe the global channel parameters of MCC1.

Table 10. Global Parameter of MCC1

Address	Name	Width	Field Value	Field Description
0x14708700	MCCBASE	Word	0x02000000	Points to the starting address of the BD (local bus address space).
0x14708704	MCCSTATE	Hword	0x0	
0x14708706	MRBLR	Hword	0x40	The maximum receive buffer length is 64 bytes.
0x14708708	GRFTHR	Hword	0x0	
0x1470870A	GRFCNT	Hword	0x0	
0x1470870C	RINTTMP	Word	0x0	
0x14708710	DATA0	Word	0x0	

Table 10. Global Parameter of MCC1

Address	Name	Width	Field Value	Field Description
0x14708714	DATA1	Word	0x0	
0x14708718	TINTBASE	Word	0x2000900	The transmit interrupt queue base address is located in L1 memory at address 0x900 (0x2000900 is the local bus address space).
0x1470871C	TINTPTR	Word	0x2000900	Transmit interrupt queue base address.
0x14708720	TINTTMP	Word	0x0	
0x14708724	SCTPBASE	Hword	0x0	
0x1470872C	XTRABASE	Word	0xB000	The extra base parameter information resides in the DPRAM at address 0xB000.
0x1470872E	C_MASK16	Hword	0x0	
0x14708730	RINTTMP0	Word	0x0	
0x14708734	RINTTMP1	Word	0x0	
0x14708738	RINTTMP2	Word	0x0	
0x1470873C	RINTTMP3	Word	0x0	
0x14708740	RINTBASE0	Word	0x2000500	The receive interrupt queue base address is located in L1 memory at address 0x500 (0x2000500 is the local bus address space).
0x14708744	RINTPTR0	Word	0x0	Receive interrupt queue base address.
0x14708748	RINTBASE1	Word	0x0	
0x1470874c	RINTPTR1	Word	0x0	
0x14708750	RINTBASE2	Word	0x0	
0x14708754	RINTPTR2	Word	0x0	
0x14708758	RINTBASE3	Word	0x0	
0x1470875C	RINTPTR3	Word	0x0	
0x14708760	TS_TMP	Word	0x0	

3.3 MCC Control Registers

Part of the global set-up is to initialize the three main MCC control registers:

- *MCCF1*. Defines the mapping of an MCC channel block to a TDM pin interface. In example discussed here, the four channels route to the TDMA port, so the MCCF1 register value is 0x0.
- *MCCM1*. The interrupt mask register filter interrupt event request to the SC140 core. We set MCCM1 to a value of 0xFFFF to enable all the interrupts.
- *MCCE1*. The interrupt Event Register report receive and transmit event. This register is cleared by writing all ones (MCCE1 = 0xFFFF) at initialization.

3.4 Channel-Specific Parameters

The main channel-specific parameters include maximum receive frame size, allowable SC140 core interrupts, start-up parameters for channels, and selection of transparent or HDLC protocol for an individual channel. The channel-specific parameters are located in DPRAM at offset 64 (channel number). For example, channel 2 is located at address 0x14700080. **Table 11** describes the channel-specific parameters for channel 0, but these parameters are identical for all channels.

Table 11. Channel-Specific Parameters of Channel 0

Address	Name	Field value	Field Description
0x14700000	TSTATE	0x1B800000	
0x14700004	ZISTATE	0x10000207	
0x14700008	ZIDATA0	0xFFFFFFFF	
0x1470000C	ZIDATA0	0xFFFFFFFF	
0x14700010	TBDflags	0x0	
0x14700012	TBDCNT	0x0	
0x14700014	TBDPTR	0x0	
0x14700018	INTMASK	0x0303	Channel interrupt mask flag. UN=1,TXB=1,RBSY=1,RXB=1
0x1470001A	CHAMR	0x7400	Transparent channel.
0x14700020	RSTATE	0x1B800000	
0x14700024	ZDSTATE	0x50FFFE0	No sync channel and regular channel.
0x14700028	ZDDATA0	0xFFFFFFFF	
0x1470002c	ZDDATA1	0xFFFFFFFF	
0x14700030	RBDflags	0x0	
0x14700032	RBDCNT	0x0	
0x14700034	RBDPTR	0x0	
0x14700038	TMRBLR	0x40	Transparent maximum receive buffer length.
0x1470003A	RCVSYNC	0x0	

3.5 Channel Extra Parameters

Each MCC channel has an 8 byte allocation for parameters defining the actual address of the Tx and Rx BD. The extra parameters are located at an offset from the base address of the DPRAM, defined by XTRBASE, in the global base parameters. The TBASE/RBASE parameters define the base address of Tx and Rx BDs for a particular channel. All BDs are contiguous in memory. **Table 12** describes the channel extra parameters. In our example, XTRBASE is set to a value of 0xB000, so the channel extra parameters are located in the DPRAM at address 0x1470B000.

Table 12. Channel Extra Parameters in the DPRAM

Address	TBASE	TBPTR	RBASE	RBPTR	Description
0x1470B000	0x2200	0x2200	0x2000	0x2200	Channel 0 extra parameters
0x1470B008	0x2202	0x2202	0x2002	0x2202	Channel 1extra parameters
0x1470B010	0x2204	0x2204	0x2004	0x2204	Channel 2 extra parameters
0x1470B018	0x2206	0x2206	0x2006	0x2206	Channel 2 extra parameters

3.6 Circular Interrupt Queues

Each unmasked channel interrupt generated during the transmission and reception of data creates an entry in an interrupt queue.The receive and transmit entries are held in separate tables. In this example, RINT0 and TINT are used for the receive and transmit interrupts, respectively, as set up in the global parameters. The interrupt queues are located in L1 memory at addresses 0x500 and 0x900. All entries in the interrupt tables must be user-initialized with a value of 0x0, except for the last word, which must be initialized with a value of 0x40000000 (W=1, thus defining the end of the table).

3.7 Serial Interface RAM

The SIRAM is a block of memory internal to the CPM that routes data from the TDM pins to the MCC. The SIRAM consists of a series of entries, one set for Tx and one for the Rx flow. **Table 13** and **Table 14** show the receive and transmit SIRAM configuration.

Table 13. Receive SI1 RAM

Address	Entry Value	MCC	LOOP	MCSEL	CNT	BYTE	LST	Description
0x14712000	0x	0x1	0x0	0x0	0x0	0x1	0x0	Channel 0 Rx entry
0x14712002	0x	0x1	0x0	0x1	0x0	0x1	0x0	Channel 1 Rx entry
0x14712004	0x	0x1	0x0	0x2	0x0	0x1	0x0	Channel 2 Rx entry
0x14712006	0x	0x1	0x0	0x3	0x0	0x1	0x1	Channel 3 Rx entry

Table 14. Transmit SI1 RAM

Address	Entry Value	MCC	LOOP	MCSEL	CNT	BYTE	LST	Description
0x14712400	0x	0x1	0x0	0x0	0x0	0x1	0x0	Channel 0 Tx entry
0x14712402	0x	0x1	0x0	0x1	0x0	0x1	0x0	Channel 1 Tx entry
0x14712404	0x	0x1	0x0	0x2	0x0	0x1	0x0	Channel 2 Tx entry
0x14712406	0x	0x1	0x0	0x3	0x0	0x1	0x1	Channel 3 Tx entry

3.8 Clocks and Baud-Rate Generation

The TDMA clocks (L1RCLKA and L1TCLKA) are always driven from an external source. In our example, the receive and transmit clocks are common and they are configured to be driven from the CLK9 pin. The CMXSI1 clock route register is set to a value of 0x88.The reference clock is from BRG0. The BRG0 output is a fraction of the CPM BRGCLK clock and is determined by the division factor programed in the BRG configuration register (BRGC1). To give a a clock rate of ~0.5MHz, BRGC10 is set to a value of 0x00010048.

Note: The BRG10 pin must be externally connected to the CLK9 pin.

3.9 Parallel I/O Pins

The CPM interface is essentially a set of I/O pins that can be configured for either a peripheral or general-purpose function. The multiplexed peripheral pins for TDMA are configured through the parallel I/O port registers, PPAR, PSOR, and PDIR (see **Table 15**).

Table 15. General I/O pins registers

Register	Register Value	Description
PPARA	0x03C00000	PA9, PA8, PA7, and PA6 are dedicated pins.
PSORA	0x03C00000	PA9, PA8, PA7, and PA6 are dedicated option 2 pins.
PDIRA	0x00000000	PA9 direction is output.
PPARB	0x0	
PSORB	0x0	
PDIRB	0x0	
PPARC	0x00000101	PC31, BRG1O, and PC23 (CLK9) are dedicated pins.
PSORC	0x00000000	All the ports are dedicated option 1.
PDIRC	0x00000001	PC31 direction is output (BRG10 port).
PPARD	0x0	
PSORD	0x0	
PDIRD	0x0	

3.10 TDMA

To enable the TDM, the serial interface registers must be configured. The SI Global Mode Register (SI1GMR) is the last register to be set up in the driver before the driver is started. Because TDMA is used, this register is set to a value of 0x01.

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