# AN1906

# MC92600 WarpLink Quad Configuring Unused Channels to Minimize Power

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## INTRODUCTION

This application note details how to configure an unused WarpLink Channel to minimize power consumption of this device.
**Warning: WarpLink is designed to allow word synchronization (32 bit alignment) for all 4 channels. If a channel is not used then word synchronization is not supported for the remaining channels.**

### 1.1 Configuration Requirements

When configuring unused channels for minimizing power consumption, all outputs associated with an unused channel should be left unconnected. All inputs (other than Receiver Link Inputs) should be tied to ground. The Receiver Link Inputs (RLINK_n_N and RLINK_n_P) should be terminated as shown in Figure 1.

Lower values of $R_1$ and $R_2$ improve noise margin (AC power) at the expense of DC power. Higher values of $R_1$ and $R_2$ reduce noise margin but save DC power. R1 and R2 must be selected such that $V_{inp} - V_{inm} \geq 35mV$. This is the minimum voltage difference necessary to maintain adequate noise margins. The best values for $R_1$ and $R_2$ are: $R_1 = R_2 = 2.2k$ ohms. This achieves $V_{inp} - V_{inm} = 38mV$.

Other values will work with slightly more power being drawn as long as the following relationships are met:

$$\frac{V_{dd}}{2} \leq V_{cm} \leq \frac{2 \cdot V_{dd}}{3}$$

$$\frac{R_2}{2} \leq R_1 \leq R_2$$

$$R_1 + R_2 \leq 4.4k$$

It does not matter which signal is pulled down. The important point is that the other should be pulled up. RLINK_n_P may be pulled down and RLINK_n_N pulled up. RLINK_n_N may be pulled down and RLINK_n_P pulled up.

Multiple links may share the same $R_1$ and $R_2$ (in parallel) by adjusting $R_1$ and $R_2$ according to:

$$R_{1new} = \frac{R_1}{x} \qquad R_{2new} = \frac{R_2}{x}$$

where “x” is the number of links sharing $R_1$ and $R_2$.

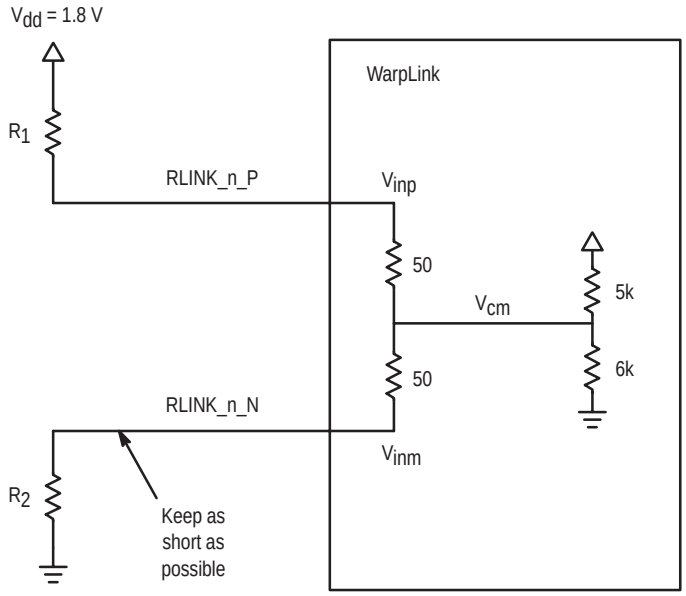


**Figure 1. Unused RLINK Termination**

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Table 1 lists the connections for the inputs and outputs of each unused channel to minimize power. All unused channels must be connected as shown.

**Table 1: WarpLink Pinout and Termination**

| WarpLink Pinout * | Input/Output | Disposition |
|---|---|---|
| XMIT_n_0 | I | GND |
| XMIT_n_1 | I | GND |
| XMIT_n_2 | I | GND |
| XMIT_n_3 | I | GND |
| XMIT_n_4 | I | GND |
| XMIT_n_5 | I | GND |
| XMIT_n_6 | I | GND |
| XMIT_n_7 | I | GND |
| XMIT_n_K | I | GND |
| XMIT_n_IDLE_B | I | GND |
| XLINK_n_P | O (link) | N/C |
| XLINK_n_N | O (link) | N/C |
| RECV_n_0 | O | N/C |
| RECV_n_1 | O | N/C |
| RECV_n_2 | O | N/C |
| RECV_n_3 | O | N/C |
| RECV_n_4 | O | N/C |
| RECV_n_5 | O | N/C |
| RECV_n_6 | O | N/C |
| RECV_n_7 | O | N/C |
| RECV_n_K | O | N/C |
| RECV_n_9 | O | N/C |
| RECV_n_IDLE | O | N/C |
| RECV_n_ERR | O | N/C |
| RECV_n_RCLK | O | N/C |
| RLINK_n_P | I (link) | See Figure 1 |
| RLINK_n_N | I (link) | See Figure 1 |

* “n” is a placeholder for the channel identifier “A” through “D”.

### 1.2 Power Consumption Estimates

Tables 2 and 3 contain estimated power consumption for various WarpLink configurations assuming the guidelines defined in Section 1.1 of this document are followed.

**Table 2: Power Estimates (mW) for 8b10b Mode**

| Supply | Condition* | 1 active channel | 2 active channels | 3 active channels | 4 active channels |
|---|---|---|---|---|---|
| 3.3V | Typical | 41 | 82 | 123 | 164 |
| 1.8V | Typical | 391 | 519 | 648 | 777 |
| Total | Typical | 432 | 601 | 771 | 941 |
| | | | | | |
| 3.3V | Worst Case | 49 | 98 | 147 | 196 |
| 1.8V | Worst Case | 453 | 603 | 753 | 902 |
| Total | Worst Case | 502 | 701 | 900 | 1098 |

**Table 3: Power Estimates (mW) for 10 bit Mode**

| Supply | Condition* | 1 active channel | 2 active channels | 3 active channels | 4 active channels |
|---|---|---|---|---|---|
| 3.3V | Typical | 48 | 96 | 144 | 192 |
| 1.8V | Typical | 391 | 519 | 648 | 777 |
| Total | Typical | 439 | 615 | 792 | 969 |
| | | | | | |
| 3.3V | Worst Case | 57 | 114 | 171 | 228 |
| 1.8V | Worst Case | 453 | 603 | 753 | 902 |
| Total | Worst Case | 510 | 737 | 924 | 1130 |

* Typical power conditions for 3.3V logic is 3.3V, 40°C, and typical process
Typical power conditions for 1.8V logic is 1.8V, 40°C, and typical process
Worst Case power conditions for 3.3V logic is 3.6V, 105°C, and best case process
Worst Case power conditions for 1.8V logic is 1.95V, 105°C, and best case process

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