AN1747

Migrating from the MC68HC705K1 to the MC68HC805K3

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Introduction

Freescale provides two different parts to easily migrate your current MC68HC705K1 (K1) application. Depending on your design, system enhancements, and cost, the MC68HC805K3 (K3) and the MC68HC705KJ1 (KJ1) provide two different migration paths.

The major differences between the K3 and the KJ1 are:

- Price
- Pinout compatibility

The K3 is pin for pin the same as the K1 but is roughly 90% the cost of the K1. Although the KJ1 is not pin for pin the same as the K1, it is roughly 70% the cost of the K1.

This application note illustrates the differences between the K1 and the K3. Note that additional features of the K3 and how they can be used in your system are discussed to further enhance your system design. Consult the K1 and K3 data books for detailed design reference.

For information on migrating your design to the KJ1, consult the application note *Migrating from the MC68HC705K1 to the MC68HC705KJ1*, Freescale document order number AN1746/D.

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MC68HC805K3 Features

- 928 bytes of user EEPROM (electrically erasable programmable read-only memory)
- 64 bytes of low-power user RAM (read-access memory)
- 128 bits of personality EEPROM (PEEPROM), not memory mapped, programmed using user software or during user EEPROM programming
- 2-MHz internal bus frequency at 5 volts
- On-chip charge pump for in-circuit programming of the PEEPROM at 3.0 to 5.5 volts
- 8-bit free-running timer with real-time interrupt
- COP (computer operating properly) watchdog timer
- 10 bidirectional input/output (I/O) pins, including:
  - 8-mA sink capability on four I/O pins
  - Software programmable pulldowns on all I/O pins
  - Keyboard scan with selectable interrupt on four I/O pins
- Selectable sensitivity on external interrupt (edge- and level-sensitive or edge-sensitive only)
- On-chip oscillator with options for:
  - Crystal or ceramic resonator with internal 2-MΩ resistor
  - 2-pin or 3-pin resistor-capacitor (RC) oscillator
  - External clock
- External interrupt mask bit and acknowledge bit
- EEPROM security bit[1] to aid in locking out access to programmable EEPROM array
- Selectable STOP conversion to HALT and option for fast restart and power-on reset
- Internal steering diode and pullup device on $\overline{\text{RESET}}$ pin to V_{DD}

1. No security feature is absolutely secure. However, Motorola's strategy is to make reading or copying the EPROM/OTPROM difficult for unauthorized users.

Migrating to the MC68HC805K3

Pinouts and Package Types

The K3 has the exact pinout as the K1. See **Figure 1** for the pinout diagram.

Both parts are available in either plastic DIP or SOIC packages.

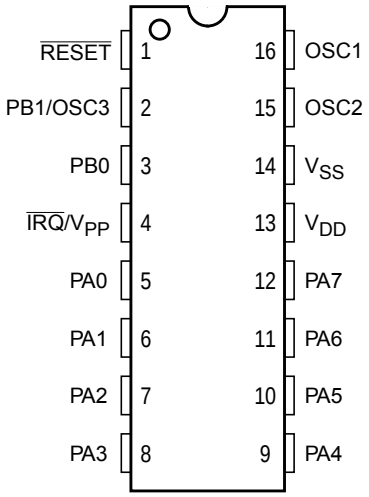

Figure 1. MC68HC705K1 and MC68HC805K3 Pinout

Block Diagrams

Throughout this application note, refer to the block diagram for the K1 in **Figure 2** and for the K3 in **Figure 3**.

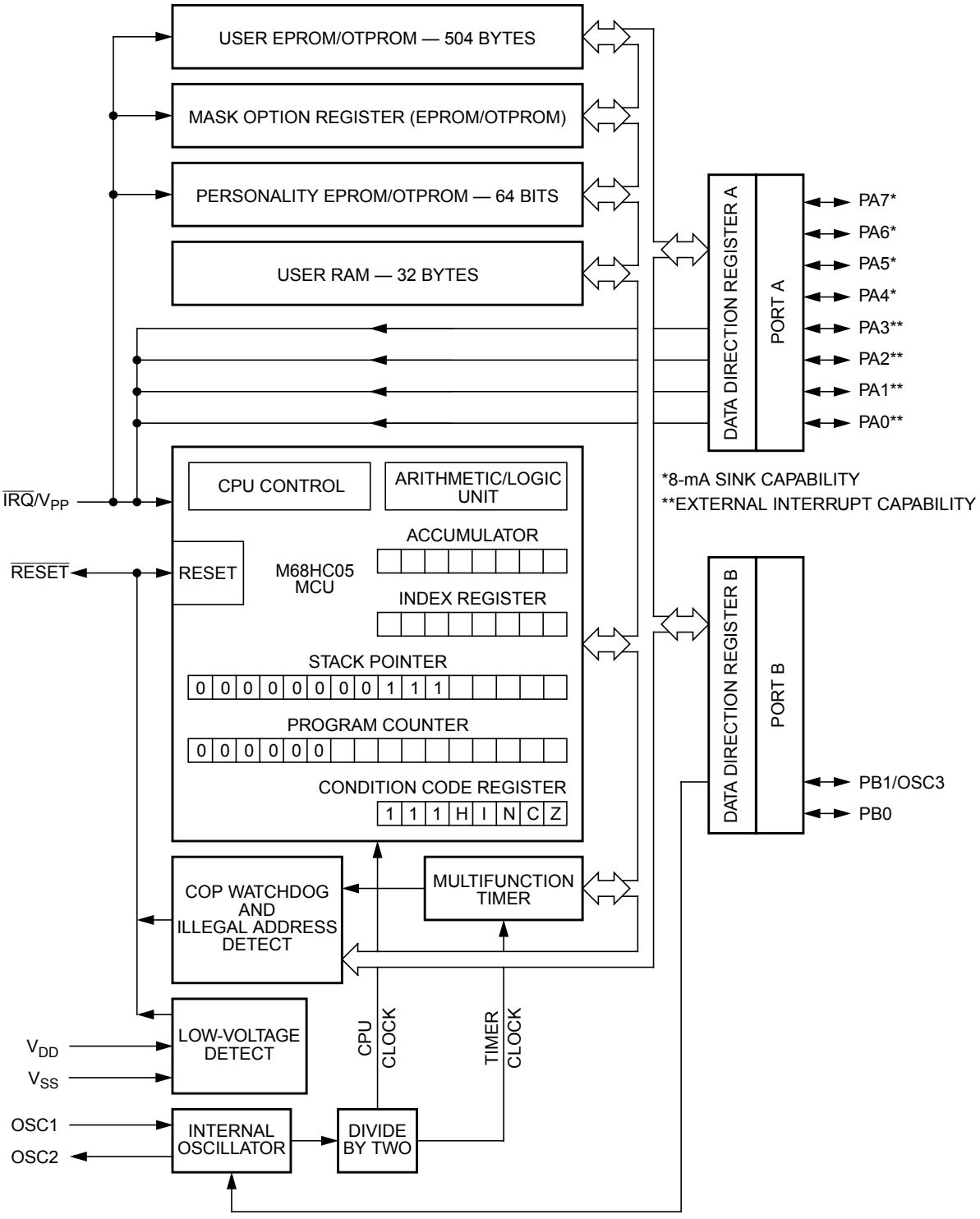

Figure 2. MC68HC705K1 Block Diagram

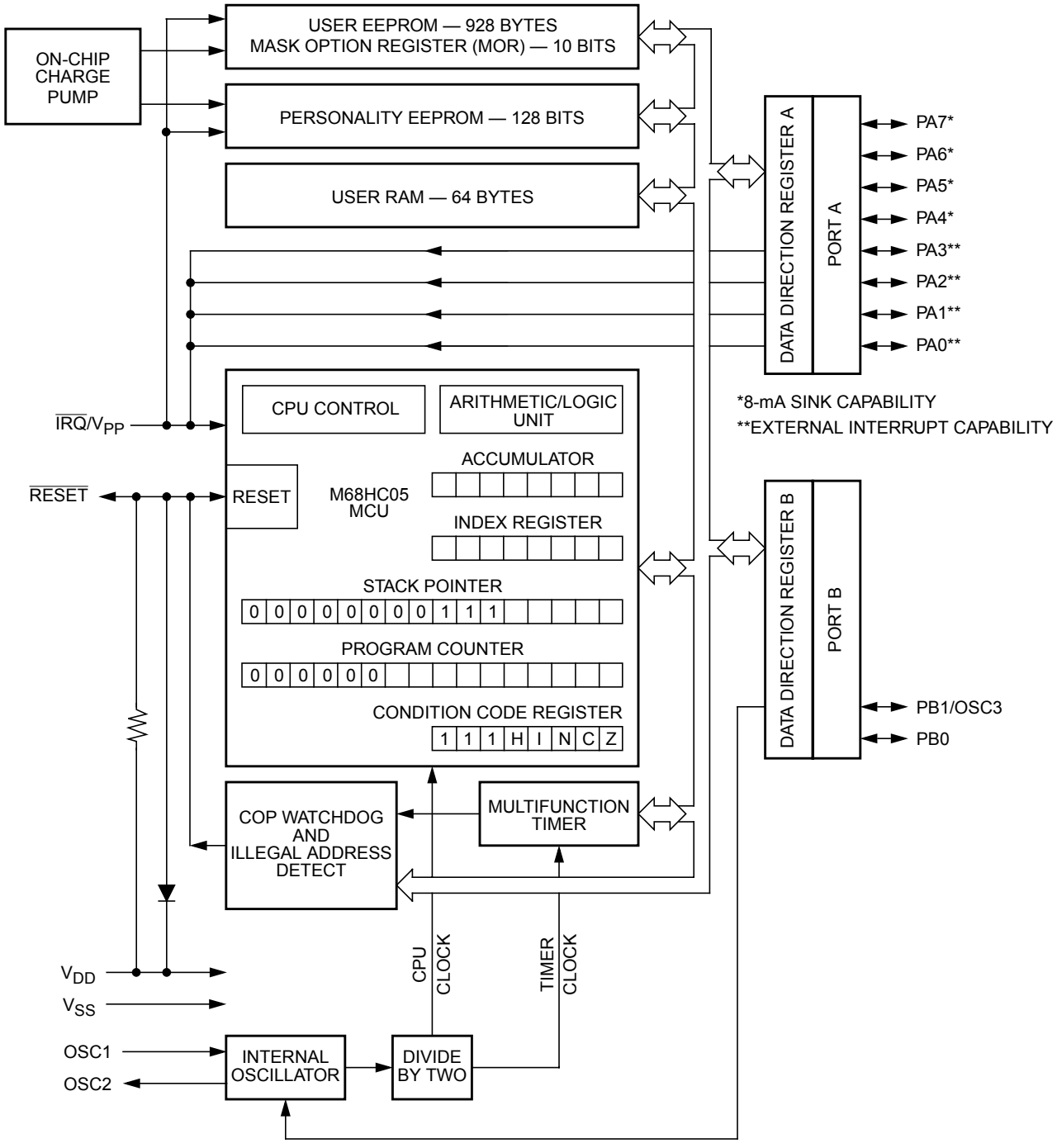

Figure 3. MC68HC805K3 Block Diagram

Memory Maps and Registers

Figure 4 and Figure 5 show the memory maps and registers of the K1 and K3.

Modify your code to reflect these points:

- To utilize the expanded RAM of the K3, move the start of RAM to $C0 from $E0.
- The EEPROM on the K3 is split into two different areas. Originate EEPROM memory to start at $100. The start of the other EEPROM array is at $20.
- The K3 has two registers for the MOR. These are located at $12 and $13.

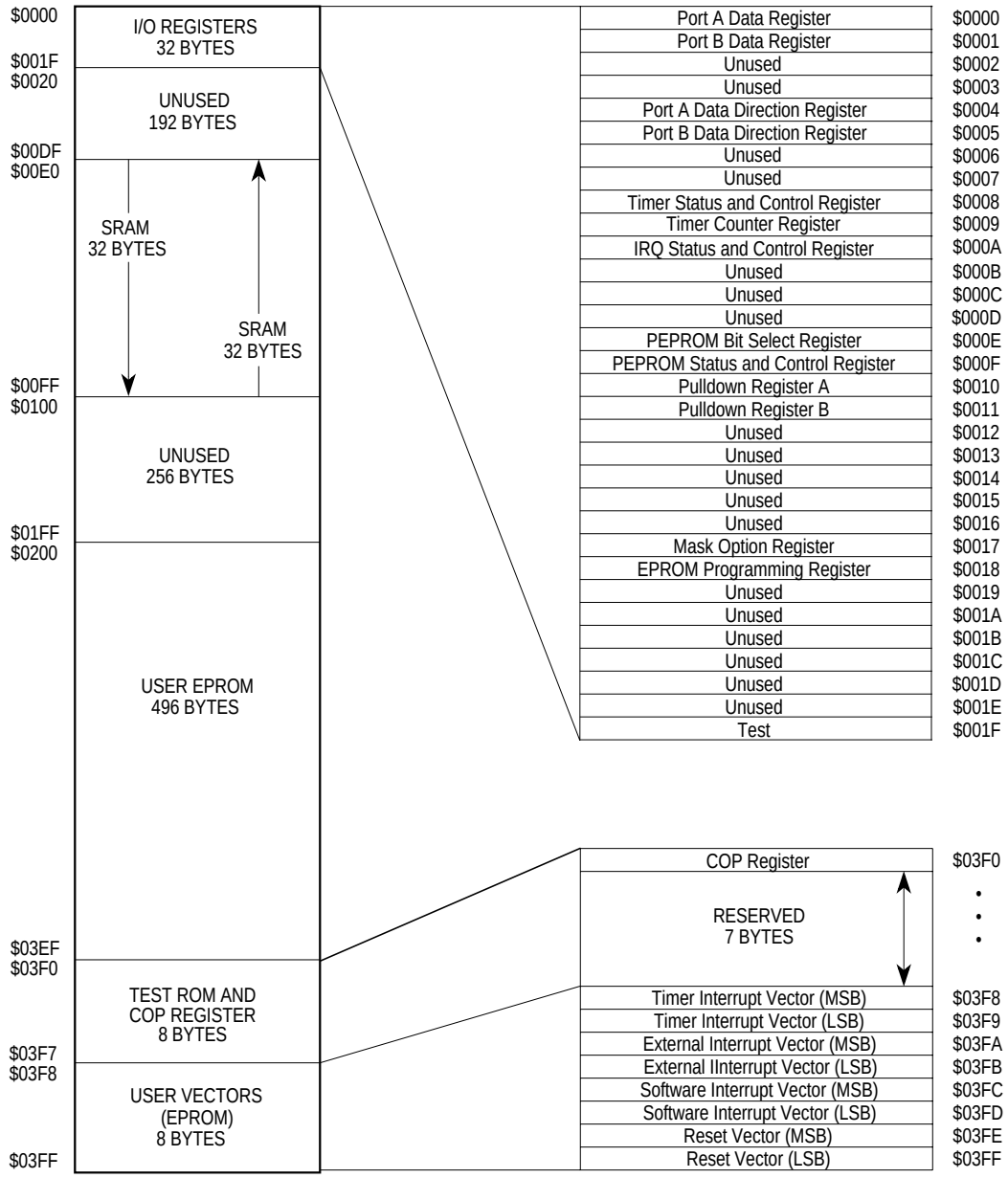

Figure 4. MC68HC705K1 Memory and Register Map

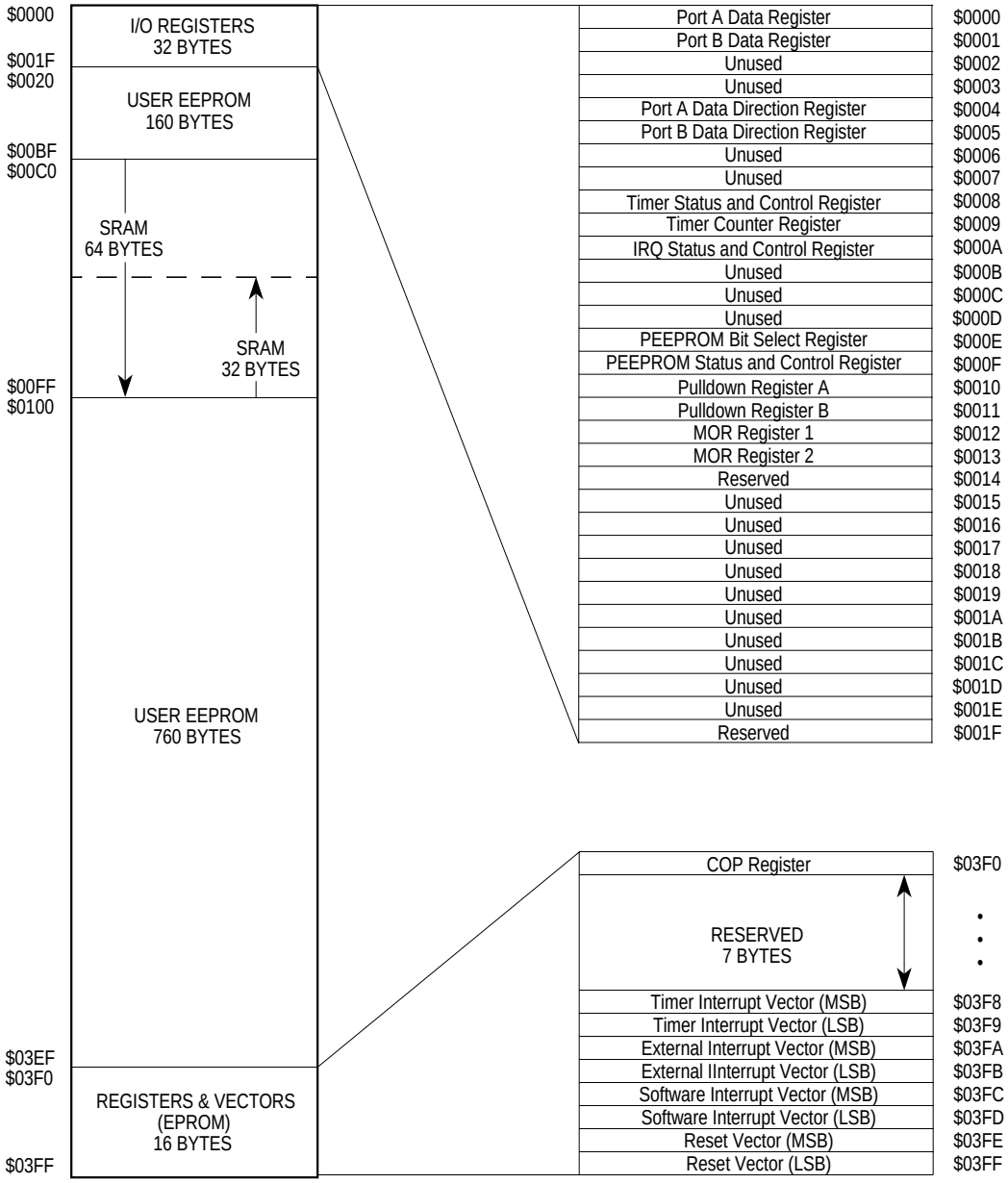

Figure 5. MC68HC805K3 Memory and Register Map

Port A No changes are needed on port A. Like the K1, the K3 can sink 8 mA of current on pins PA7–PA4.

Port B No changes are needed on port B.

Clock

The internal clock circuitry of the K3 is identical to that of the K1. Configuring the oscillator depends on the settings of the PIN3 and RC bits in the MOR (mask option register). These bits can be programmed at bit 6 and bit 5 at location $12.

Reset and LVR Circuitry

The reset function on the K3 has some additional features. These are:

- The $\overline{\text{RESET}}$ pin contains a steering diode to discharge any voltage on the pin to V_{DD} when the power is removed.
- The $\overline{\text{RESET}}$ pin contains an internal pullup resistor to V_{DD} to allow the $\overline{\text{RESET}}$ pin to be left unconnected for low-power applications.

The K3 has all of the K1 reset sources except a low-voltage reset (LVR). These are:

- Power-on reset
- Logic 0 on the $\overline{\text{RESET}}$ pin
- Computer operating properly (COP)
- Illegal address

The K3 does not have an internal LVR. External LVR circuitry should be added to ensure system integrity.

Interrupts

Like the K1, the K3 has the same interrupt sources and functionality. These are:

- Software interrupt
- Logic 0 applied to the $\overline{\text{IRQ}}/V_{PP}$ pin
- Logic 1 applied to one of the PA3–PA0 pins
- Timer overflow interrupt
- Real-time interrupt

The interrupt status and control register on the K3 is identical to that register on the K1.

Two bits in the K3 MOR, location $12, define interrupt functionality. They are the PIRQ bit and the LEVIRQ bit. They function like the PIRQ and LEVEL bits of the K1.

Timer

The timers on the K3 and K1 are identical. Consequently, no changes are needed in software or hardware.

COP

The COP on the K1 is enabled by programming the COPEN bit (bit 0) of the MOR at location $17 to a 1. On the K3, program the COPEN bit (bit 0) of the MOR at location $12 to a 1.

The K1 COP timer is cleared by writing a 0 to bit 0 of the COPR (computer operating properly register) at location $3F0. This does not change on the K3.

Just like the K1, the K3 COP timeout is set by RT1 and RT0 bits of the timer status and control register. No code changes are needed.

Personality EEPROM

Like the K1, the K3 provides memory to store variables, constants, and system information. Instead of EPROM, the K3 uses 128 bits of personality EEPROM (PEEPROM). These 128 bits are provided as a simple EEPROM array and control logic that requires serial reading of the data. The PEEPROM may be accessed via software programmed into the user ROM through two registers that directly interface with the PEEPROM array. The actual implementation of the software varies, depending on customer requirements.

The PEEPROM array is arranged as 16 bytes (rows) with a separate column select for each bit (column) in a byte. The column select connects the bit to a single sense amplifier as shown in the block diagram of the PEEPROM module in **Figure 6**.

An on-chip charge pump is provided to allow programming and erasure of the personality EEPROM if the supply voltage to the V_{DD} pin is at least 3.0 Vdc.

NOTE: *Programming and erasure of the PEEPROM may be performed only if V_{DD} > 3.0 Vdc.*

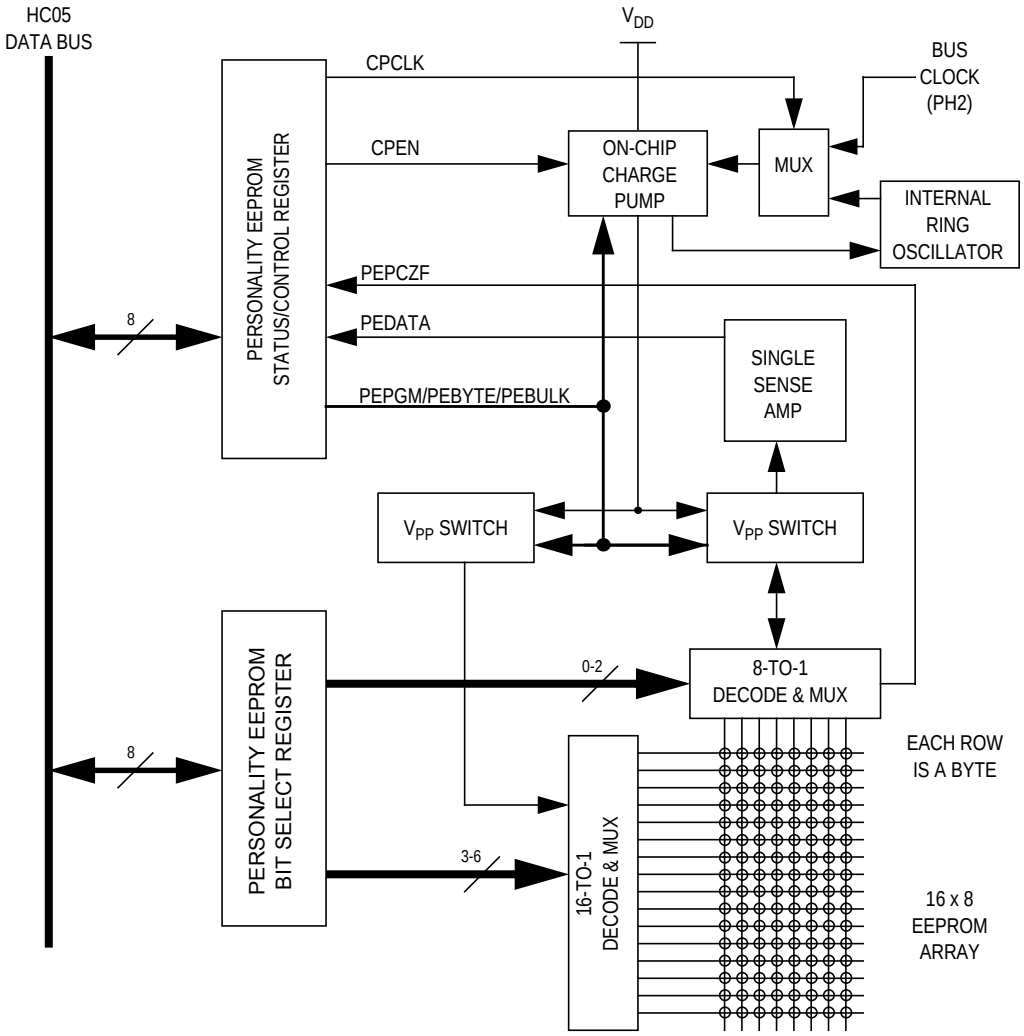

Figure 6. Block Diagram of the K3 PEEPROM

Consult the K3 manual for a detailed description of the PEEPROM and its configuration registers, PEBSR and PESCR.

For programming routines, consult the Freescale application note *Programming the 68HC(8)05K3's Personality EEPROM on the MMDS and MMEVS*, Freescale document order number AN1288/D.

MOR

The K3 gives users additional options in the MOR. **Table 1** compares the MORs of the two parts.

Table 1. MOR Comparison

Part	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
K1	$17	SWPDI	PIN3	RC	SWAIT	LVRE	PIRQ	LEVEL	COPEN
K3	$12	RCSTD	PIN3	RC	HALT	SWPDI	PIRQ	LEVIRQ	COPEN
K3	$13							SBIT1	SBIT0

SWPDI The software pulldown inhibit bit has the same functionality on both parts but is found at bit 3 of the K3 MOR location $12.

PIN3 The PIN3 bit has the same functionality on both parts.

RC The RC bit has the same functionality on both parts.

SWAIT The STOP conversion-to-wait bit has the same functionality on the K3 but the bit is named HALT. It is found at bit 4 location $12.

LVRE The K3 does not have a low-voltage reset function. This option is not found in the K1 MOR registers.

PIRQ The port A IRQ enable bit has the same functionality on both parts.

LEVEL The external interrupt sensitivity bit has the same functionality on the K3 but the bit is named LEVIRQ. It is found at bit 2 location $12.

COPEN The COP enable bit has the same functionality on both parts.

RCSTD The RC oscillator startup delay bit controls the oscillator stabilization counter. The normal stabilization delay following reset or exit from stop mode is 4064 bus cycles. Setting the RCSTD enables a 16-bus cycle stabilization. If your oscillator design has a quick startup time, the

RCSTD bit will allow quicker recovery from oscillator startup. Setting the bit to a 1 enables the shorter oscillator delay.

EPMSEC The K3 provides the added functionality of securing the EEPROM array. The SBIT1 and SBIT0 bits at location $13 define the security options on the K3.

Table 2. Setting EEPROM Security

SBIT1	SBIT0	EEPROM and Personality EEPROM Security
0	0	Enabled
0	1	Enabled
1	0	Enabled
1	1	Disabled

Ordering Information

Table 3 shows the MC order numbers for the K3.

Table 3. Ordering Information for the MC68HC805K3

Package Type	Temperature	Order Number
Plastic DIP	0 to 70 °C	MC68HC805K3P
SOIC	–40 to 85 °C	MC68HC805K3CP
Plastic DIP	0 to 70 °C	MC68HC805K3DW
SOIC	–40 to 85 °C	MC68HC805K3CDW

References/Additional Reading

MC68HC805K3 General Release Specification, document order number HC805K3GRS/D, Freescale

MC68HC705K1 Technical Data Book, document order number MC68HC705K1/D, Freescale

M68HC05 Applications Guide, document order number M68HC05AG/AD, Freescale.

Application Note

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