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GSM900/DCS1800 Dual-Band 3.6 V Power Amplifier Solution with Open Loop Control Scheme

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INTRODUCTION

Dual band GSM900 and DCS1800 (or DCS1900) phone design puts a real challenge on Power Amplifier function which needs to operate in two frequencies while providing appropriate isolation and control for each frequency.

This application note describes the dual band demoboard that we have developed based on two single band Power Amplifier ICs: MRFIC0919 and MRFIC1819, plus a dedicated control IC: MC33170 (product of ON Semiconductor).

DUAL–BAND DEMOBOARD

New IPA Generation

– Our previous range of 3.6 V GaAs IPAs (MRFIC0917 for GSM900 and MRFIC1817 for DCS1800/PCS1900) was requiring external negative voltage to operate which was derived from a dedicated Power Management IC MC33169. The way to control the Power Amplifiers with this IC is detailed in Application Note AN1599 and a dual band application using MRFIC0917, MRFIC1817 and MC33169 (product of ON Semiconductor) is described in Application Note AN1602.

The MRFIC0919 and MRFIC1819 are the follow–up of the MRFIC0917 and MRFIC1817 with three major improvements:

– Absolutely Spur free Voltage Generators are included in the IPA (based on synchronous rectification of the RF carrier). A negative voltage is used for biasing the line–up and a positive step–up voltage for depleting the NMOS drain switch FET.
– Better performances in terms of output power. This is particularly of interest for dual band application where the recombination of the GSM900 and the DCS1800/PCS1900 lines before the antenna induces additional insertion losses.
– Smaller packaging: both devices are housed in a TSSOP–16EP package which has an attractive size (5x6.5mm, maximum height of 1.2 mm) and an exposed backside pad allowing excellent thermal and electrical performances.

In addition, gain has been increased on MRFIC0919 compared to MRFIC0917 allowing operation with input power down to 3.0 dBm. Both MRFIC0919 and MRFIC1819 are featuring three stages RF line–up.

Negative/Positive Voltage Generator

On both MRFIC0919 and MRFIC1819, RF rectification is used to build the dc bias voltage supply on chip (patent pending). The DC Voltage Generator (basically schottky diodes and capacitor network) is connected at the output of a dedicated buffer that samples and amplifies the RF input signal.

The key advantage of this built–in dc voltage generation is to remove the need of an external switching supply generator which would require particular attention when laying out the board due to possible spurious beside the RF carrier as modulation sidebands.

– The negative voltage is high enough (–5.0 V) to simultaneously bias the activated RF line up while disabling the other one through their gates.
– The positive voltage is used to drive an NMOS FET switch that performs the Output Power Control according to the Drain Control method.

All those voltages are shared and used by the MC33170 that in addition performs the band selection job by either setting correct biasing point to a path or turning it off.

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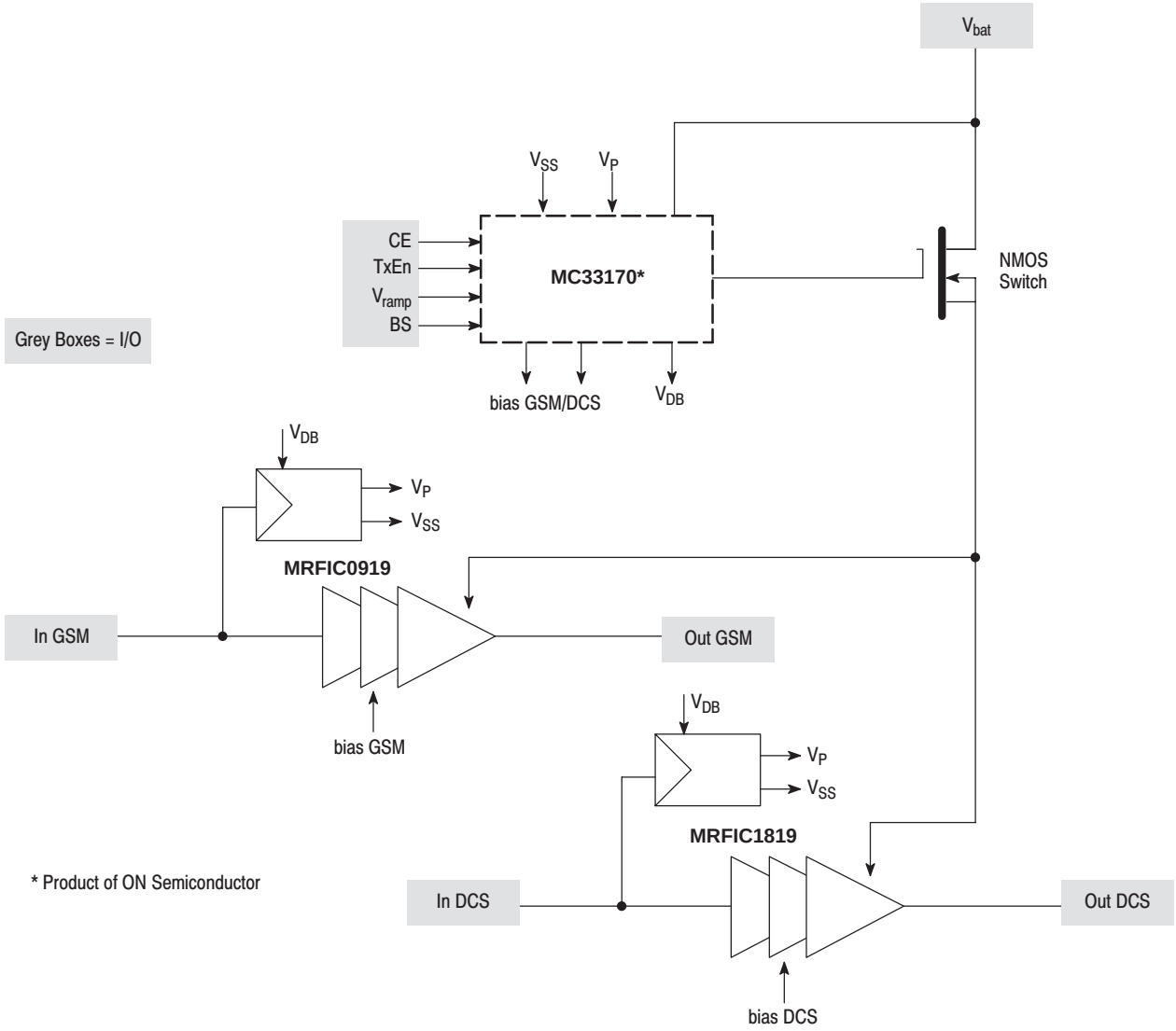
Figure 1. Block Diagram



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Dual Band Demoboard Description

The dual band demoboard implements the MRFIC0919 and MRFIC1819 in the RF section composed of separated GSM900 and DCS1800 paths. This simple arrangement is the best solution for reducing crosstalk between the two bands; especially regarding the second harmonic of GSM leaking through the DCS paths.

A common control section (composed by MC33170+MTSF3N02HD, products of ON Semiconductor) is located at the top of the demoboard. Those ICs interface properly the RF section with the main supply voltage thanks to control signals. First the TXEN signal is used to activate the Negative Voltage Generator and then the V_{RAMP} signal performs the burst shaping. Also a very simple selection circuitry enables the Power Amplifier according to BS (band selection) signal.

Figure 2. GSM/DCS Dual–Band Application Board

DC Connector Detail

1. **V_{ramp} (0 to 2.0 V)**
2. VDI (0 to V_{BAT})
3. V_p (8.0 V)
4. V_{D2} (0 to V_{BAT})
5. V_{SS} (–5.0 V)
6. V_{DB} (0/V_{BAT})
7. **CE (0/2.0 V)**
8. **BS (0/2.o V)**
9. **Gnd**
10. V_{D3} (0 to V_{BAT})
11. **V_{BAT} (3.6 V)**
12. **TxEn (0/2.0 V)**

NOTE: Only Pins 1, 7, 8, 9, 11 and 12 are required to operate the board.

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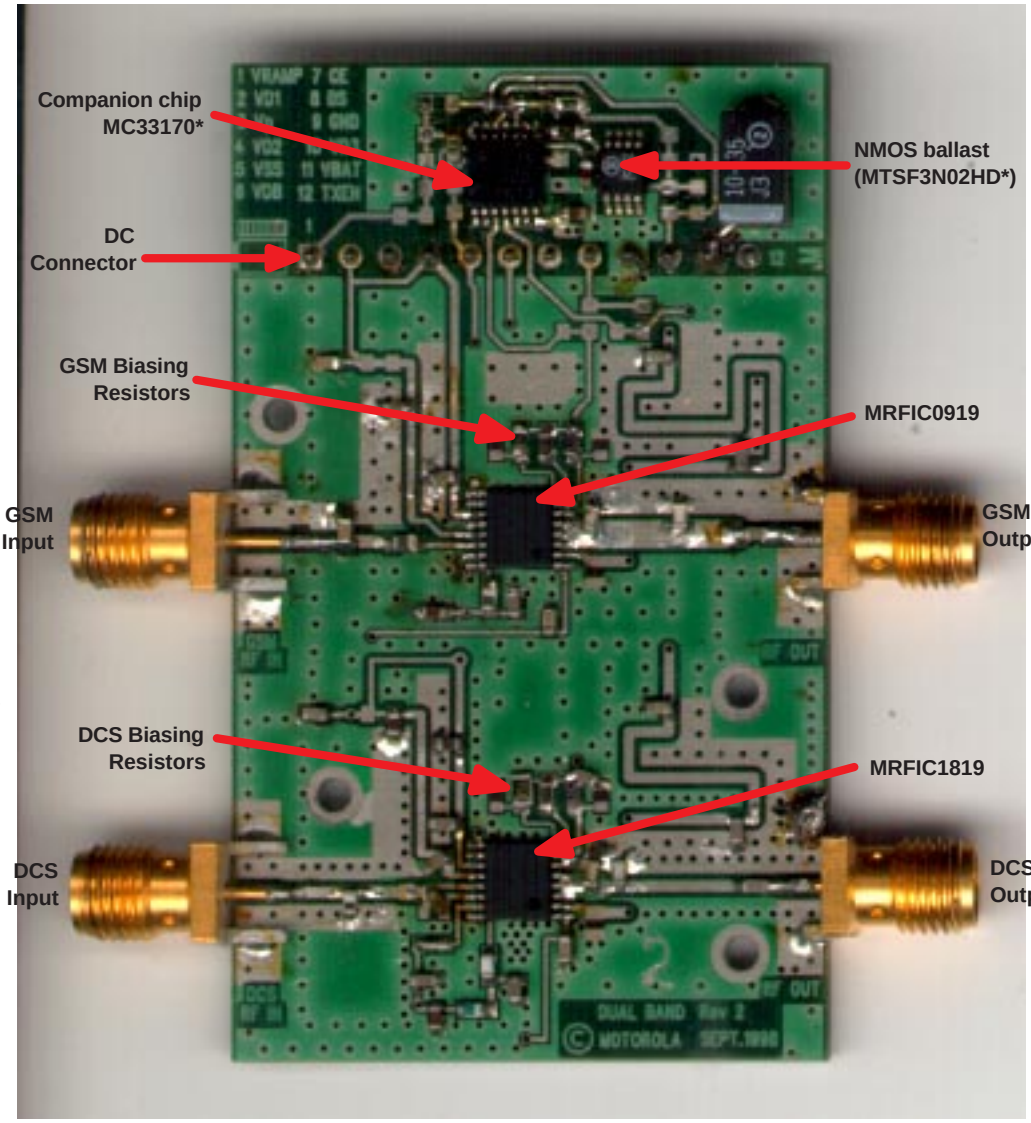

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Application Schematic

The electrical schematic given hereafter is the reference circuitry for the complete application. In particular it has been used to populate the above PCB and on this demoboard have been performed all the measurements that will follow.

Figure 3. Application Schematic

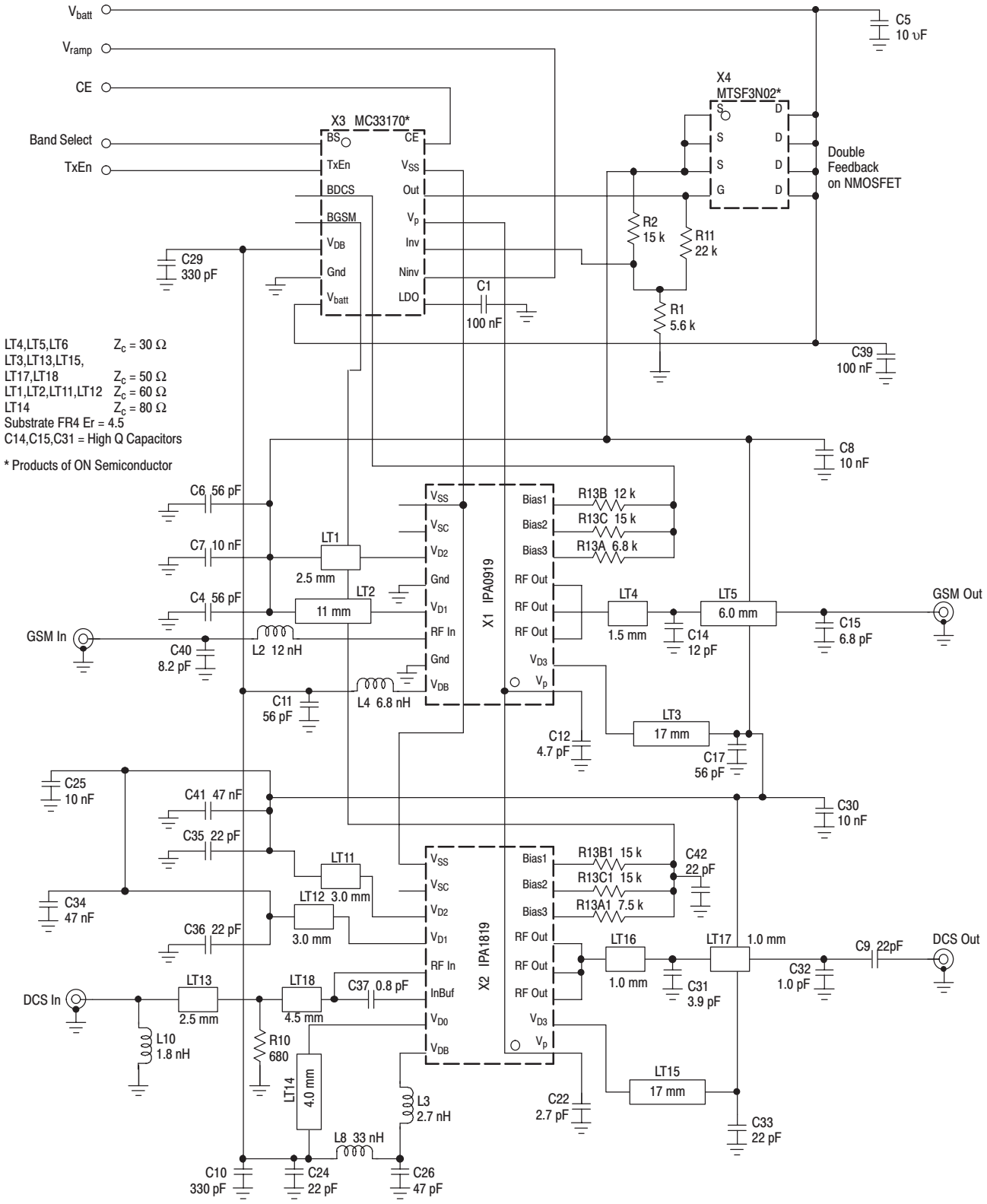

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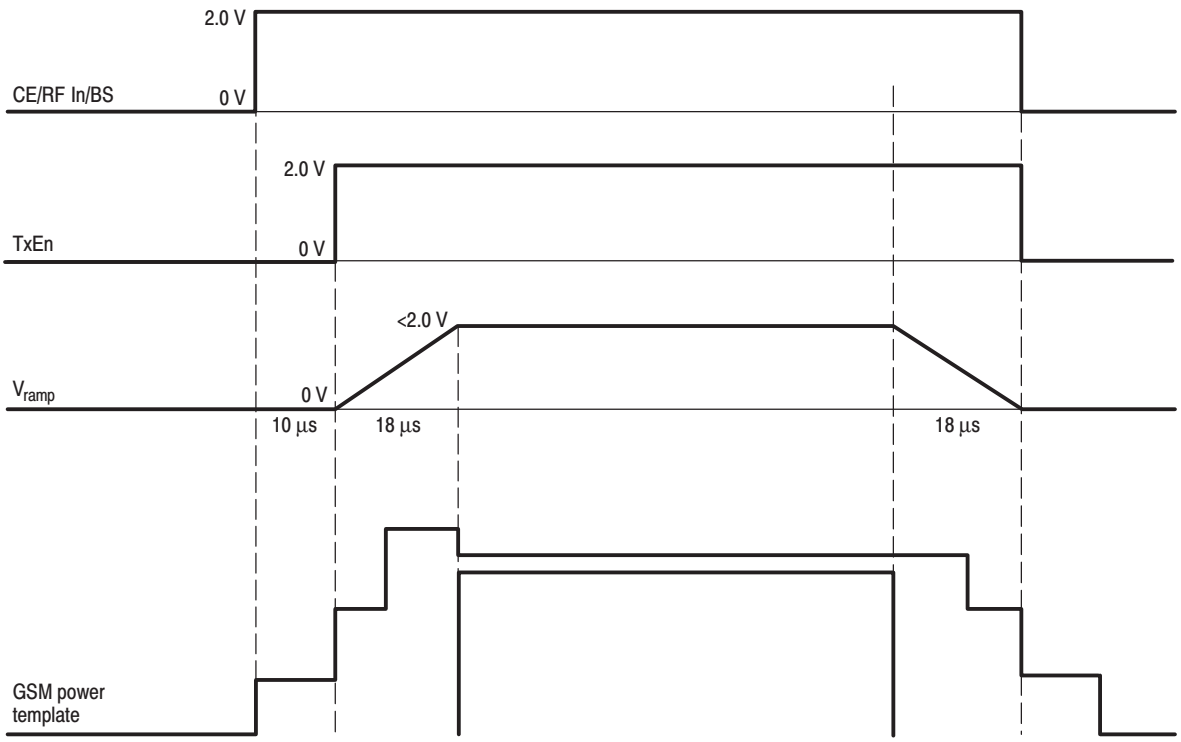
Figure 4. Control Signals Timing for Burst Mode



Burst Shaping

The association of both IPAs with the companion chip gives a unique solution suitable for fast burst operation that can wake–up from complete stand by mode (Current <10 µA) to full output power within the GSM power template. In order to perform burst mode measurements, the following timing can be used as a guide line.

Explanation:

– CE is activated at the very beginning of the burst (28 µs before the nominal part of the burst), this is also the right time to apply input power to the selected line up (Set Band Select appropriately).
– TxEn is activated 10 µs later to activate the buffer and generate Negative and Positive Voltage. The settling time of negative and positive voltages is so short (<1.0 µs) that burst ramping can be initiated also.
– V_{ramp} can start almost immediately after TxEn and is smoothly shaped in order to limit the switching transient (a simple linear ramp is good enough as shown on the next plots).
– The falling down is performed the same way (but in the reverse order), and last even shorter (18us is enough).

Next plot shows the output power versus time for four different PCL (power control level) within the top 30 dB range. The exact same timing is kept for all PCL; only the nominal voltage of Vramp is changed to set the nominal output power (within the useful part of the burst).

The four traces correspond to V_{ramp} = 0.41, 0.52, 0.8 and 1.9 V respectively. Also there is a gap in the time sweep (after 50 µs) that removes the constant power section of the burst.

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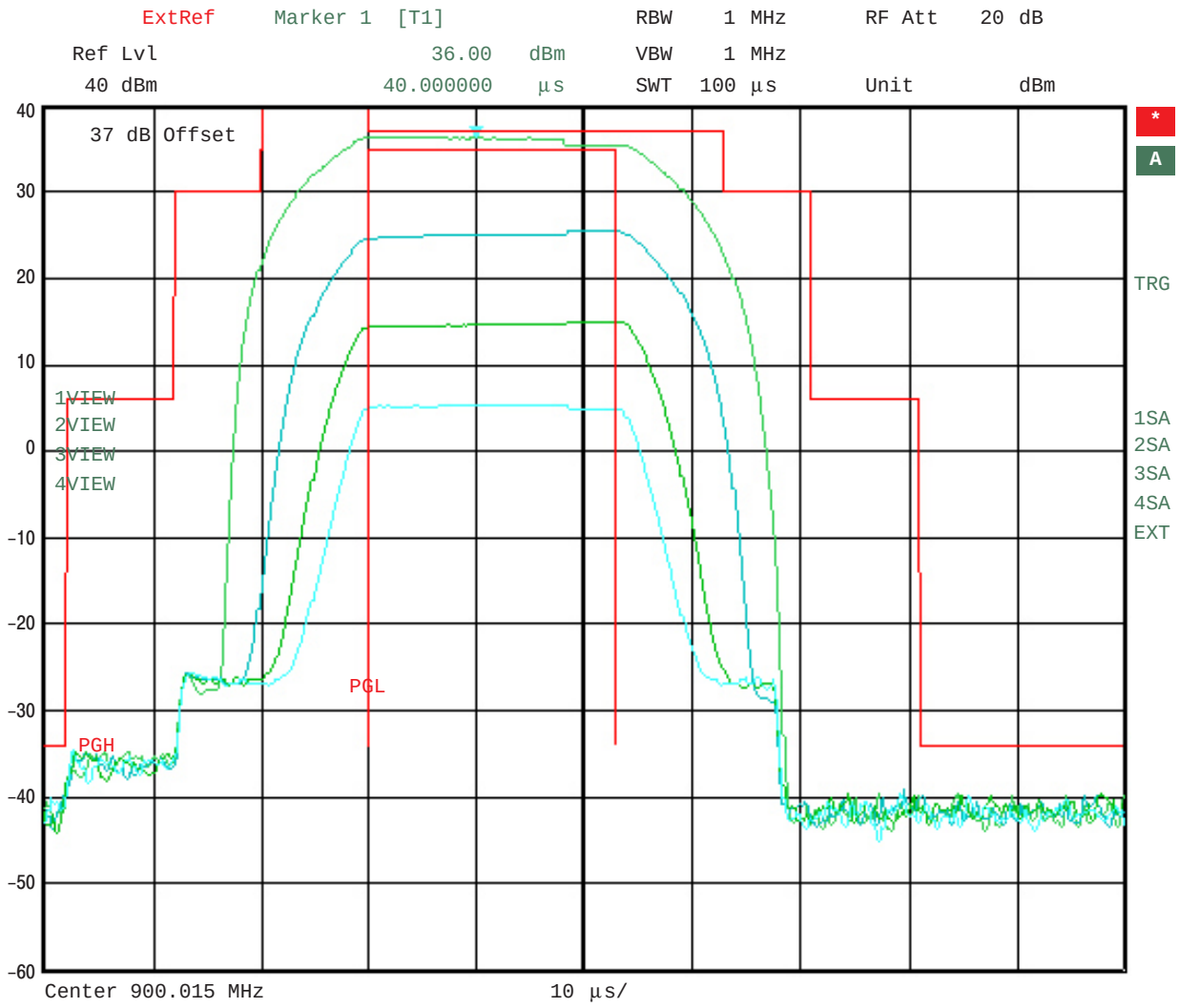
Figure 5. Power versus Time



Switching Spectrum

The second (but most severe) condition that any transmitted GSM burst has to fulfill is the spectral mask or output spectrum due to switching transient. A max hold measurement is used to check the possible spectral degradation a few channels apart from the carrier.

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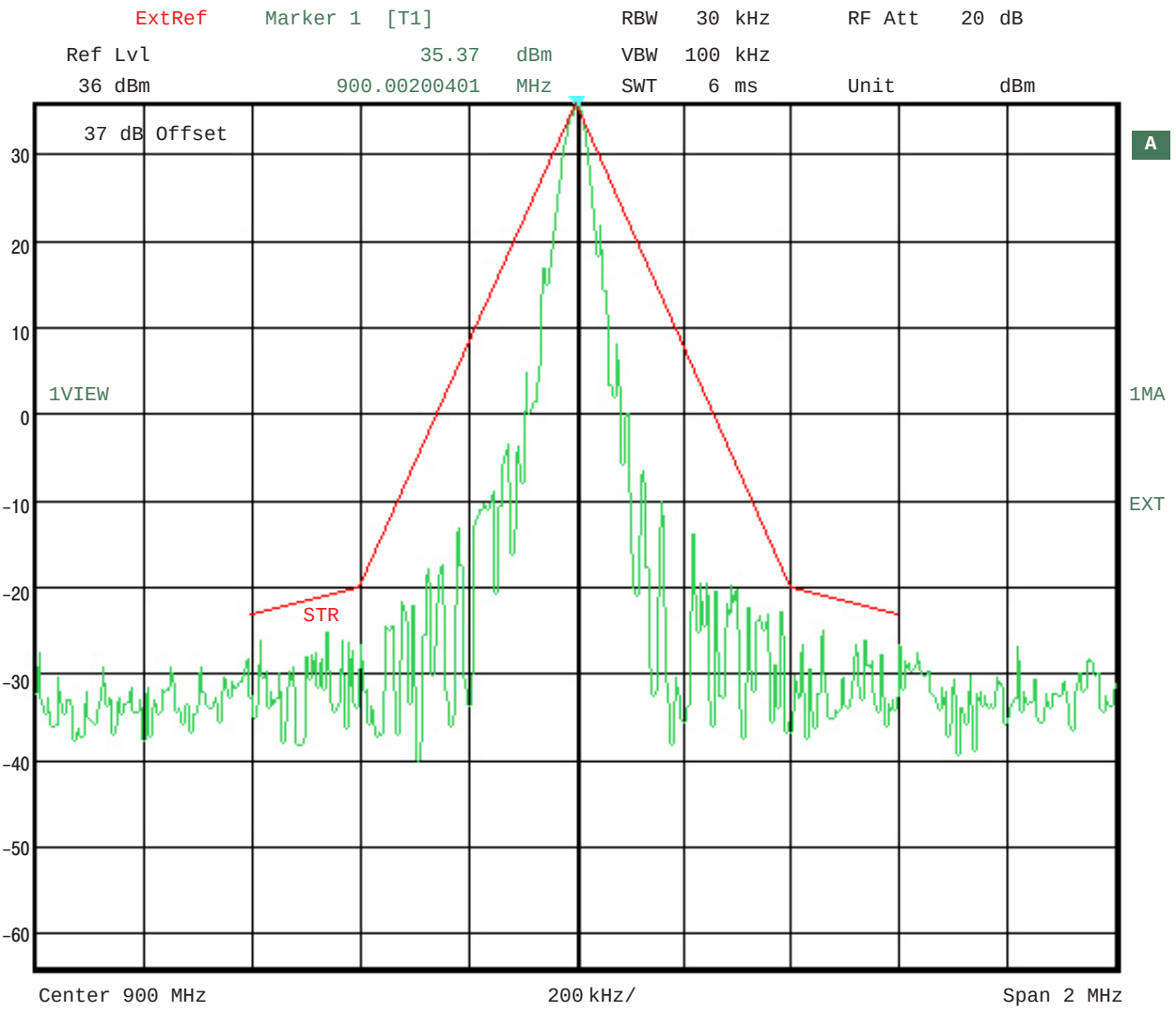
Figure 6. Output Spectrum (Max Hold)



Open Loop versus Temperature

The Drain Control principle is stable and predictive enough to be used in an open loop mode: this simply means that you don't need to sense the output power but simply trust the IPA drain supply voltage. The following 2 measurements clearly highlight the good stability of the drain control versus either frequency or temperature.

This control method will be thoroughly depicted in the second part of this application note.

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Figure 7. Output Power versus Temperature

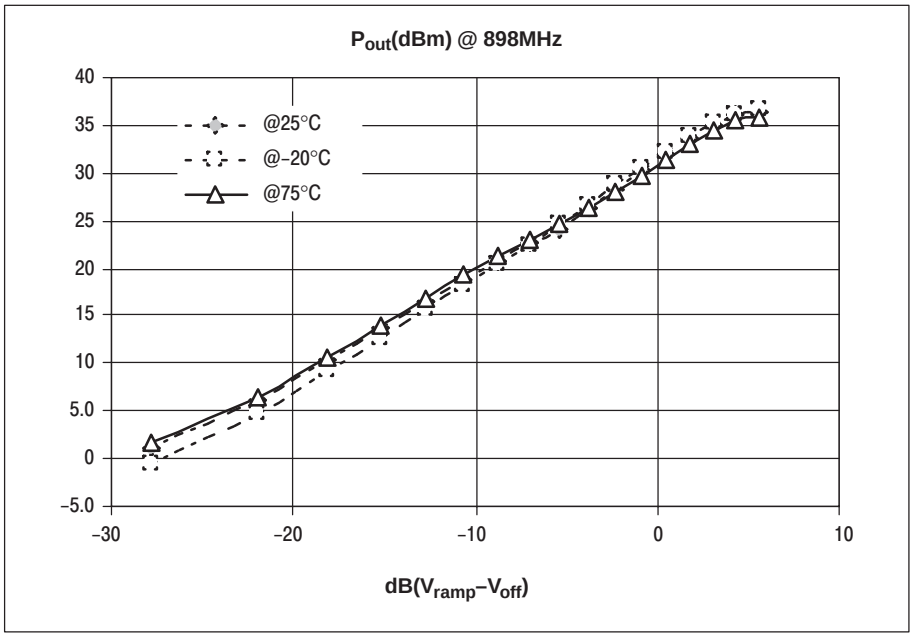
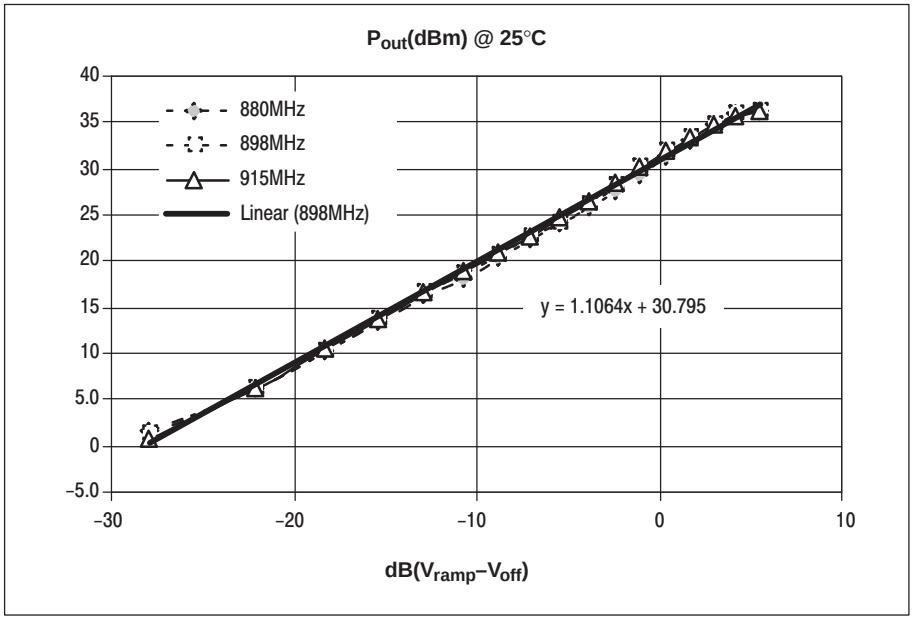


Figure 8. Output Power versus Frequency



Another tremendous advantage of the drain control technique is the very low ripple across the Tx band in all the useful dynamic range (top 30 dB).

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CONTROL PHILOSOPHY

MRFIC0919 and MRFIC1819 application uses the drain control technique developed for our previous range of GaAs IPAs (refer to AN1599).

A NMOS FET is used to switch the IPA drain and vary the drain supply voltage from 0 to battery voltage. As the NMOS FET requires higher voltage than Vbat to fully saturate it, a positive step–up voltage is generated inside the IPA for that purpose. An fast Operational Amplifier is included in the MC33170 and can be customized to provide proper transfer function between control signal V_{ramp} and IPA supply voltage. This OpAmp is connected using in a dual feedback configuration: both the NMOS gate and source voltages are injected back to the inverting input in order to maintain good linearity of control and avoid any saturation at the output of the OpAmp.

Indeed, the control has the benefit of providing linear transfer function while also being repeatable versus control voltage and temperature variations. Therefore it appears as a good candidate for open loop configuration (the coupler and the temperature compensation diode from the traditional control loop can be removed).

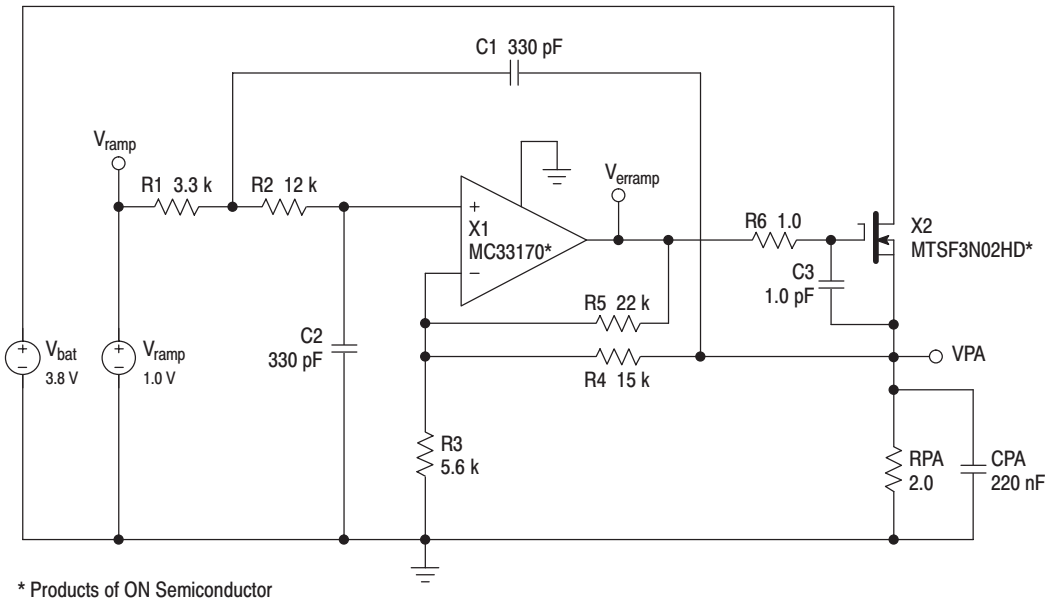
Double Feedback

In previous open loop application with MC33169 (see AN1599), the control signal V_{ramp} was multiplied by a fixed gain amplifier and applied to the NMOS gate. Now that MC33170 gives complete access to all pins of its internal OpAmp, one could imagine embedding the NMOS inside the feedback loop to compensate for its threshold voltage variation. This way a true linear law would be guaranteed between control voltage and IPA drain voltage hence RF voltage. Although this concept is quite satisfactory for steady state condition, it shows some penalty for the transient response. As a matter of fact, the OpAmp output can go high and saturate into its supply rail (when control voltage is too high or battery voltage too low) and exhibit a small delay to recover during the falling down of the burst. The immediate consequence is to deteriorate the switching transient spectrum.

Double feedback is the good compromise to get the best of both solutions: it provides some compensation of Vth while avoiding OpAmp saturation.

The following schematic will be used as the baseline to discuss this concept and simulate its behavior. Note that some capacitors are included inside the circuitry to provide in addition a Low–Pass filter characteristic. The IPA is simply modeled by RPA and CPA.

Figure 9. Control Circuitry Schematic



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Sweep on V_{ramp}

The following plot represents the gate voltage and source voltage of the NMOS versus Vramp.

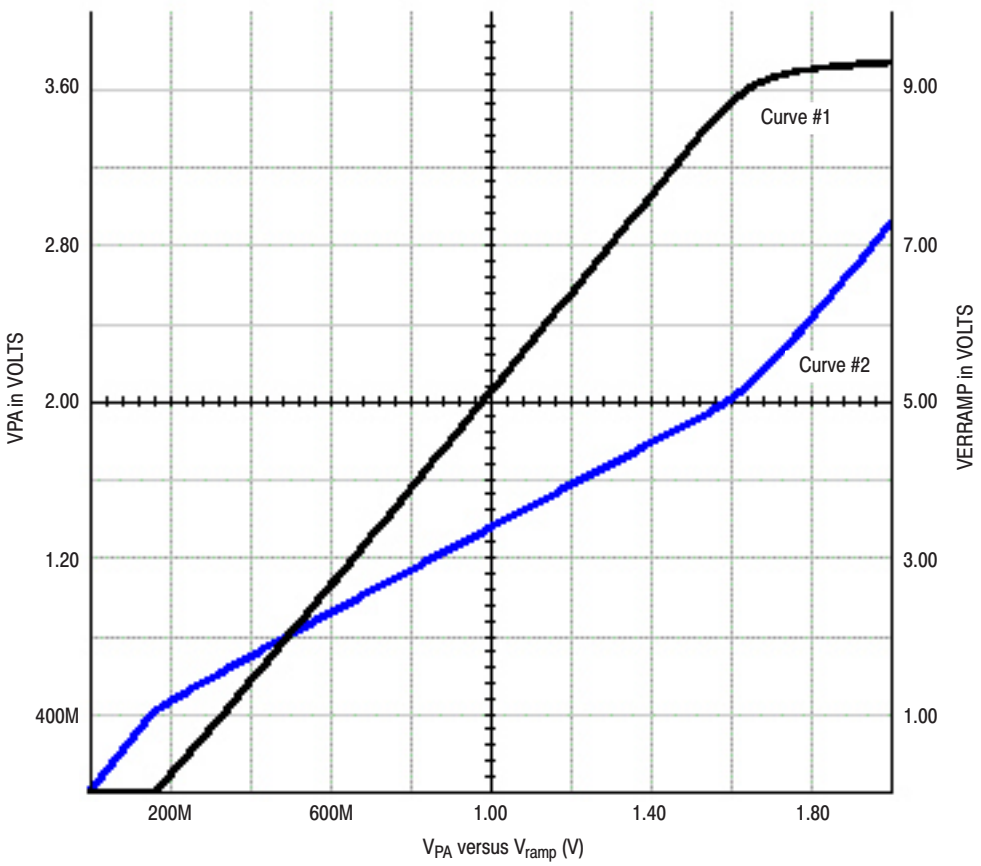
V_{ramp} is swept from 0 to 2.0 V. Curve #1 is the IPA supply voltage and curve #2 is the output voltage of the OpAmp. The later shows 3 different portions:

– The first one (slope = divider ratio between R5 and R3//R4, i.e. G1=(R5+R3//R4)/(R3//R4)) occurs when the NMOS is off (no feedback via the VPA voltage). This higher slope contributes to reduce the dead zone before reaching VGSth (approximately 1.1 V for this NMOS fet).

– The smaller one (divider ratio between R5//R4 and R3) occurs when the NMOS is in its ohmic region as a voltage follower. This is the useful portion covered for linear Pout control.

– The third one (slope = divider ratio between R5 and R3//R4) occurs when the NMOS is saturated (no more feedback via the VPA voltage that is limited by Vbat). This higher slope is useful to still increase the NMOS gate voltage while avoiding OpAmp saturation.

Figure 10. DC Transfer Function



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Bessel Type LPF

The most appropriate transfer function to realize the burst shaping is a Bessel type since its pulse response exhibit smooth transition with no overshoot. The switching transients are also minimized after the shaping.

A 2 pole Bessel filter is embedded in the OpAmp external circuitry as a Salen–Key topology. The gain used to compute component value is the smaller one of second portion (divider ratio between R5//R4 and R3: G2 = (R3 + R4//R5)/R3 = 2.7).

Note that R3, R4 and R5 are used to set the gain value then only R1, R2, C1 and C2 determine the filter characteristic. The theoretical values of those components for a cut–off frequency of 60 kHz are:

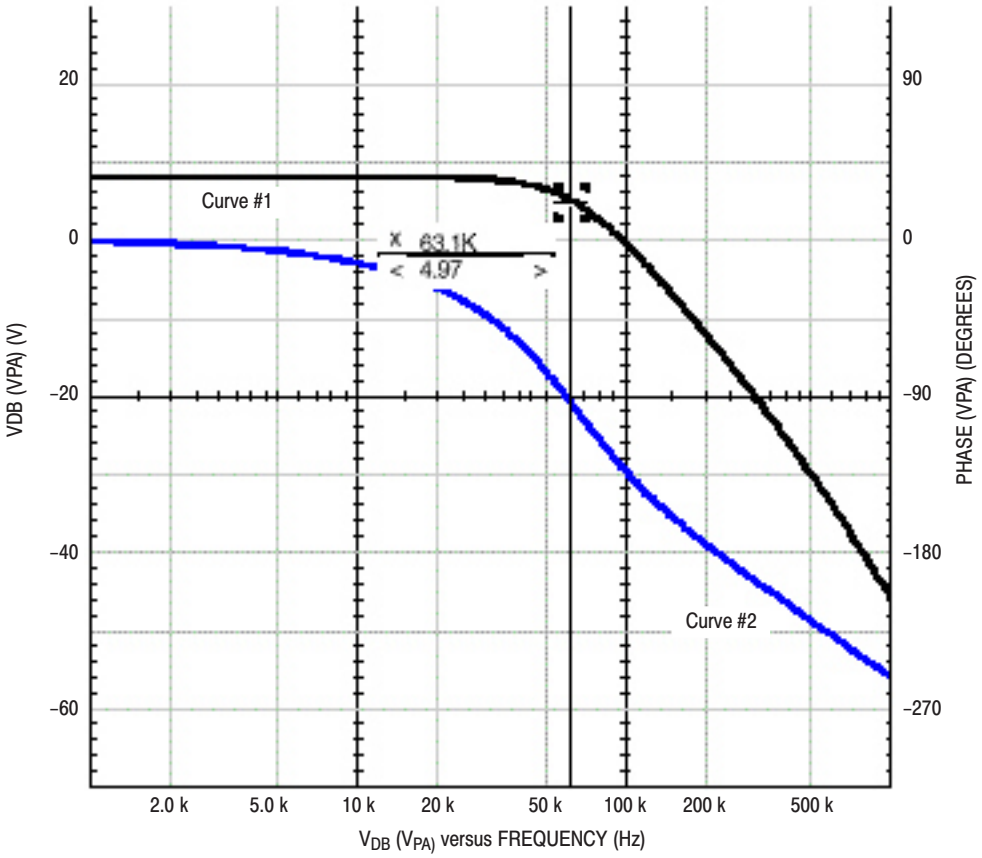
R1 = 3.0 k, R2 = 13 k, C1 = 330 pF, C2 = 330 pF.

Closest normalized value were chosen instead and used for the simulation without significant difference.

Transfer Function (Bode Plot)

Cut–off frequency is around 63 kHz, with dc gain about 8.0 dB.

Figure 11. Simulated Frequency Response



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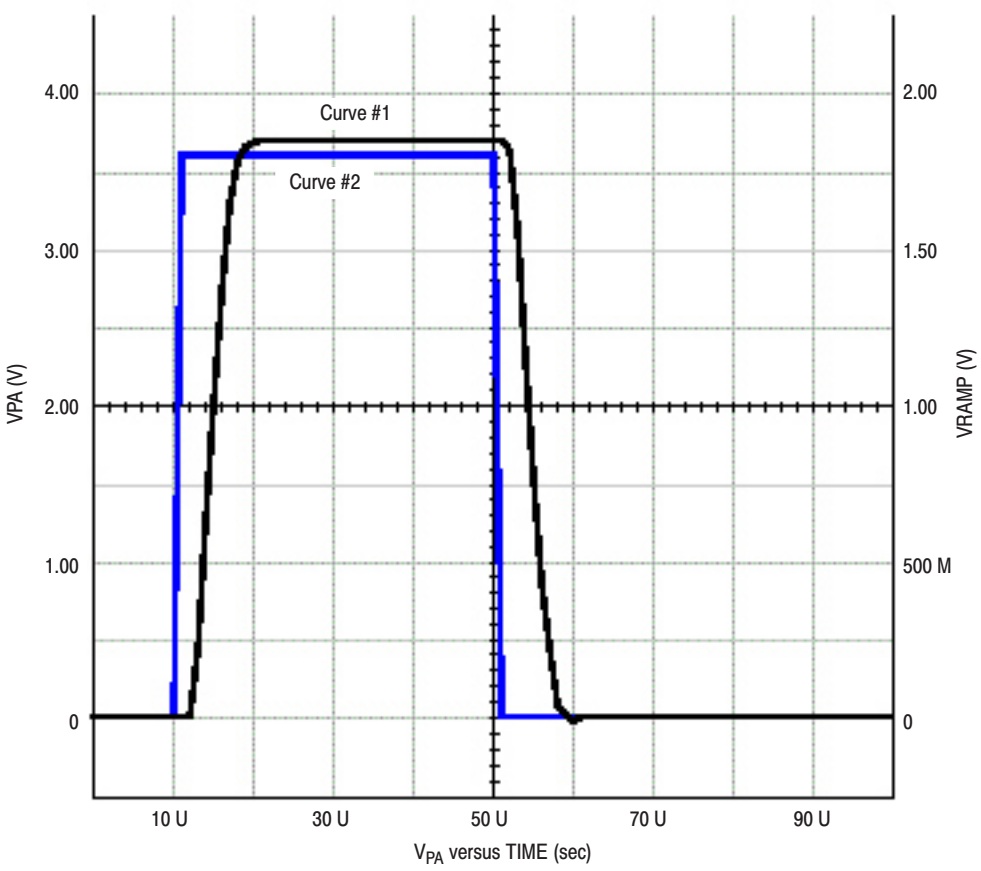
Pulse Response

At last the time domain response to a rectangular pulse is shows hereafter. The settling time is about 7us without overshoot as expected.

It is clear that in real application the control voltage Vramp can be much more sophisticated because it is generated by a dedicated DAC using look–up tables for ramp up and down. Indeed, this signal looks like a staircase that can approximate optimum rising/falling edges with minimal spectral content. Anyway, the same low pass filter characteristic is still required to smooth this staircase.

Figure 12. Simulated Time Transient



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CONCLUSION

The dual band Power Amplifiers demo board described in this application note is a stand alone system solution for dual band transmitters. Using off–the–shelf mono band IPAs plus a dedicated controller, one can easily meet the GSM ETSI recommendations with a rugged, simple but innovative architecture.

The “open loop” concept for controlling Pout is demonstrated as a viable solution with key advantages:

- Suppression of the coupler leads to minimize the insertion losses after the PA.
- Suppression of the detector diodes and their possible compensation circuitry.
- At last but not least, it eases the calibration of the transmitter (thanks to its superior predictability, linearity and reproducibility) and shortens the production time for that phase.

REFERENCES

1. MRFIC0919 Data Sheet: 3.6 V GSM 900 MHz GaAs Integrated Power Amplifier.
2. MRFIC1819 Data Sheet: 3.6 V DCS 1800 MHz GaAs Integrated Power Amplifier.
3. MC33170 Data Sheet: High Performance Integrated Driver for Dual–Band RF Power Amplifiers. (Product of ON Semiconductor)
4. AN1599 Application Note: Power Control with the MRFIC0913 GaAs Integrated Power Amplifier and MC33169 Support IC.
5. AN1602 Application Note: 3.6 V and 4.8 V GSM/DCS1800 Dual Band PA Application with DECT Capability Using Standard Motorola RFIC’s.

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