AN15223

Migration guide among MCX A series

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Document information

Information	Content
Keywords	MCX A series, device migration, porting guide, pin multiplexing, motor control, memory constraints.
Abstract	This application note provides a porting and design guide for migrating applications among devices in the MCX A series, with a focus on moving from the higher-end MCX A346/345 to the cost-optimized MCX A344/343 variants. It covers device selection, core and clocking differences, pinout and peripheral mapping considerations (LPUART, I2C, pin multiplexing), analog subsystem resources (ADC, OPAMP, comparators) and their impact on three-shunt motor control designs, Flash/SRAM memory constraints and alternative memory organization, and code optimization practices. The guidance is intended to help hardware and firmware engineers minimize redesign effort and avoid common pitfalls when porting designs across the MCX A series.

1 Introduction

This application note provides a concise porting and design guide for migrating devices among the MCX A series.

During early stages of product development, it is common practice to select a microcontroller with larger memory resources and broader feature availability to simplify development and provide maximum flexibility. In later production phases, cost optimization often leads to selecting a lower-tier device within the same family, such as transitioning from MCX A346/345 to MCX A344/343.

Devices with smaller memory capacities might not meet new requirements. In such cases, migrate to a device with a larger memory capacity, for example, from MCX A343 to MCX A346 or from MCX A153 to MCX A156.

Although these devices belong to the same product family, hardware and software portability is not always seamless. In particular, pin compatibility and peripheral availability may differ, which can introduce necessary modifications to the hardware design. Some peripherals present on the higher-end device may be reduced, relocated, or unavailable on the cost-optimized variants.

Another critical topic is the memory constraints discussed in the chapters below.

This document highlights the key differences and provides guidance to ensure a smooth transition, with a focus on minimizing redesign effort and avoiding common pitfalls. To help you understand the guidance, this document uses an example of migration between MCX A346/345 and MCX A344/343.

2 MCX A series products

Table 1. MCX A series products overview

Series	Part number	Main Clock	Features	Packages
MCX A1 Essential	MCX A13	96	1x ADC, I3C	H-PQFN32, LQFP48
	MCX A14	48	1x/2x ADC, I3C, USB, Opt. CAN	H-PQFN32, LQFP48, LQFP64, LQFP100, LFBGA64, VFBGA112
	MCX A15	96	1x/2x ADC, Opt. OPAMP, I3C, USB, Opt. CAN	H-PQFN32, LQFP48, LQFP64, LQFP100, LFBGA64, VFBGA112
	MCX A17	180	2x ADC, OPAMP, Opt. I3C, USB, CAN	H-PQFN32, LQFP48, LQFP64, LQFP100, LQFP144, WFBGA169
	MCX A18	240	2x ADC, OPAMP, I3C, USB, 2x CAN, seg-LCD	LQFP64, LQFP100, LQFP144, VBGA169
MCX A2 Enhanced	MCX A25	180	2x ADC, OPAMP, I3C, USB, CAN, Advanced security	LQFP64, LQFP100, LQFP144, WFBGA169
	MCX A26	240	2x ADC, OPAMP, I3C, USB, 2x CAN, seg-LCD, Advanced security	LQFP64, LQFP100, LQFP144, WFBGA169
MCX A3 Mixed-Signals	MCX A34	180	2x/4x ADC, 3x/4x OPAMP, CAN	H-PQFN32, LQFP48, LQFP64, LQFP100, LQFP144, WFBGA169
	MCX A35	240	4x ADC, 4x OPAMP, CAN	LQFP64, LQFP100, LQFP144, VBGA169
	MCX A36	240	4x ADC, 4x OPAMP, I3C, USB, CAN, seg-LCD, Advanced security	LQFP64, LQFP100, LQFP144, VBGA169

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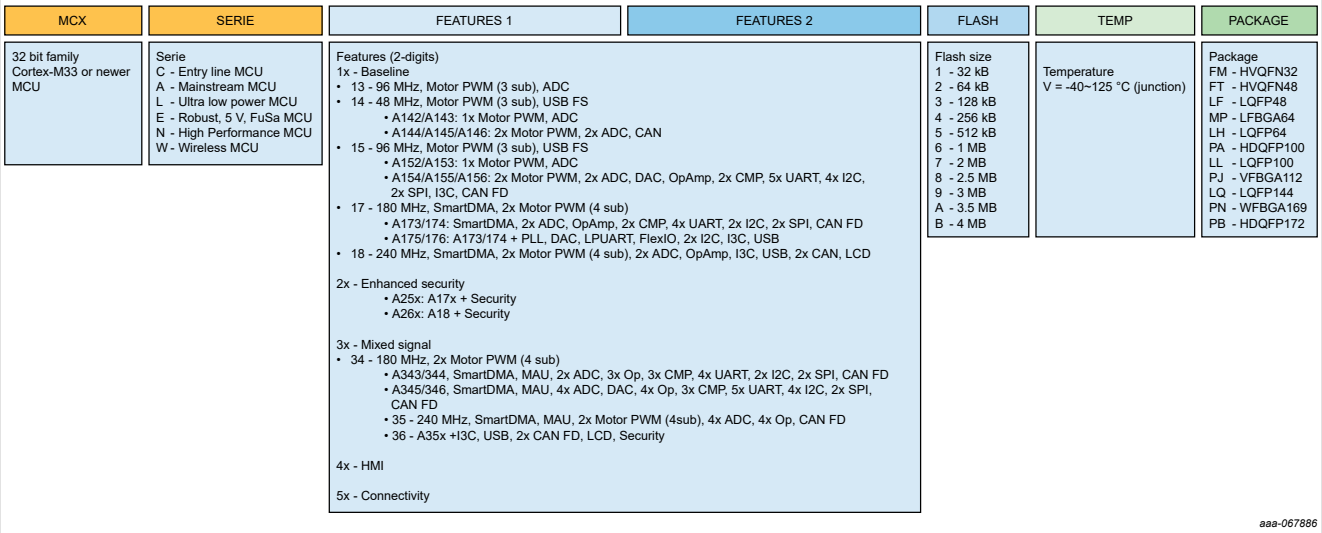


Figure 1. Part numbering

3 MCX A product selection

Table 2. MCX A13x/14x/15x product selection

Part number	Embedded memory		Core Cortex-M33 (MHz)	GPIO	Package	
	Flash (kB)	SRAM (kB)			Pin count	Type
MCX A133VFT	128	32	96	44	48	QFN
MCX A133VFM	128	32	96	29	32	QFN
MCX A133VLF	128	32	96	41	48	LQFP
MCX A132VFT	64	16	96	44	48	QFN
MCX A132VFM	64	16	96	29	32	QFN
MCX A132VLF	64	16	96	41	48	LQFP
MCX A143VLH	128	32	48	52	64	LQFP
MCX A143VFT	128	32	48	41	48	QFN
MCX A143VFM	128	32	48	26	32	QFN
MCX A142VLH	64	16	48	52	64	LQFP
MCX A142VFT	64	16	48	41	48	QFN
MCX A142VFM	64	16	48	26	32	QFN
MCX A153VLH	128	32	96	52	64	LQFP
MCX A153VFT	128	32	96	41	48	QFN
MCX A153VFM	128	32	96	26	32	QFN
MCX A152VLH	64	16	96	52	64	LQFP
MCX A152VFT	64	16	96	41	48	QFN
MCX A152VFM	64	16	96	26	32	QFN

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Table 3. MCX A175/176/185/186/255/256/265/266 product selection

Part number	Embedded memory		Core Cortex-M33 (MHz)	GPIO	Package	
	Flash (kB)	SRAM (kB)			Pin count	Type
MCX A175VPN	512	128	180	114	169	WFBGA
MCX A175VLQ	512	128	180	114	144	LQFP
MCX A175VLL	512	128	180	83	100	LQFP
MCX A175VLH	512	128	180	52	64	LQFP
MCX A176VPN	1024	256	180	114	169	WFBGA
MCX A176VLQ	1024	256	180	114	144	LQFP
MCX A176VLL	1024	256	180	83	100	LQFP
MCX A176VLH	1024	256	180	52	64	LQFP
MCX A185VPN	512	128	240	114	169	WFBGA
MCX A185VLQ	512	128	240	114	144	LQFP
MCX A185VLL	512	128	240	83	100	LQFP
MCX A185VLH	512	128	240	52	64	LQFP
MCX A186VPN	1024	256	240	114	169	WFBGA
MCX A186VLQ	1024	256	240	114	144	LQFP
MCX A186VLL	1024	256	240	83	100	LQFP
MCX A186VLH	1024	256	240	52	64	LQFP
MCX A255VPN	512	128	180	114	169	WFBGA
MCX A255VLQ	512	128	180	114	144	LQFP
MCX A255VLL	512	128	180	83	100	LQFP
MCX A255VLH	512	128	180	52	64	LQFP
MCX A256VPN	1024	256	180	114	169	WFBGA
MCX A256VLQ	1024	256	180	114	144	LQFP
MCX A256VLL	1024	256	180	83	100	LQFP
MCX A256VLH	1024	256	180	52	64	LQFP
MCX A265VPN	512	128	240	114	169	WFBGA
MCX A265VLQ	512	128	240	114	144	LQFP
MCX A265VLL	512	128	240	83	100	LQFP
MCX A265VLH	512	128	240	52	64	LQFP
MCX A266VPN	1024	256	240	114	169	WFBGA
MCX A266VLQ	1024	256	240	114	144	LQFP
MCX A266VLL	1024	256	240	83	100	LQFP
MCX A266VLH	1024	256	240	52	64	LQFP

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Table 4. MCX A343/344 product selection

Part number	Embedded memory		Core Cortex-M33 (MHz)	GPIO	Package	
	Flash (kB)	SRAM (kB)			Pin count	Type
MCX A344VLL	256	64	180	86	100	LQFP
MCX A344VLH	256	64	180	55	64	LQFP
MCX A344VLF	256	64	180	41	48	LQFP
MCX A344VFM	256	64	180	29	32	H-PQFN
MCX A343VLL	128	32	180	86	100	LQFP
MCX A343VLH	128	32	180	55	64	LQFP
MCX A343VLF	128	32	180	41	48	LQFP
MCX A343VFM	128	32	180	29	32	H-PQFN

Table 5. MCX A345/346/355/356/365/366 product selection

Part number	Embedded memory		Core Cortex-M33 (MHz)	GPIO	Package	
	Flash (kB)	SRAM (kB)			Pin count	Type
MCX A345VPN	512	128	180	114	169	WFBGA
MCX A345VLQ	512	128	180	114	144	LQFP
MCX A345VLL	512	128	180	86	100	LQFP
MCX A345VLH	512	128	180	55	64	LQFP
MCX A346VPN	1024	256	180	114	169	WFBGA
MCX A346VLQ	1024	256	180	114	144	LQFP
MCX A346VLL	1024	256	180	86	100	LQFP
MCX A346VLH	1024	256	180	55	64	LQFP
MCX A355VPN	512	128	240	114	169	WFBGA
MCX A355VLQ	512	128	240	114	144	LQFP
MCX A355VLL	512	128	240	86	100	LQFP
MCX A355VLH	512	128	240	55	64	LQFP
MCX A356VPN	1024	256	240	114	169	WFBGA
MCX A356VLQ	1024	256	240	114	144	LQFP
MCX A356VLL	1024	256	240	86	100	LQFP
MCX A356VLH	1024	256	240	55	64	LQFP
MCX A365VPN	512	128	240	114	169	WFBGA
MCX A365VLQ	512	128	240	114	144	LQFP
MCX A365VLL	512	128	240	86	100	LQFP
MCX A365VLH	512	128	240	55	64	LQFP
MCX A366VPN	1024	256	240	114	169	WFBGA
MCX A366VLQ	1024	256	240	114	144	LQFP
MCX A366VLL	1024	256	240	86	100	LQFP

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Table 5. MCX A345/346/355/356/365/366 product selection...*continued*

Part number	Embedded memory		Core Cortex-M33 (MHz)	GPIO	Package	
	Flash (kB)	SRAM (kB)			Pin count	Type
MCX A366VLH	1024	256	240	55	64	LQFP

4 MCX A series core specifications

Table 6. MCX A series core specifications

Part number	Main clock	CPU
MCX A153/152/133/132	96	Arm 32-bit Cortex-M33 CPU, no FPU, no DSP extension instruction set, no TrustZone, no MPU
MCX A143/142	48	
MCX A156/155/154	48	Arm 32-bit Cortex-M33 CPU, with FPU and DSP extension instruction set, no TrustZone, no MPU
MCX A146/145/144	96	
MCX A173/174	180	Arm 32-bit Cortex-M33 CPU, with FPU and DSP extension instruction set and MPU, no TrustZone
MCX A185/186/265/266	240	
MCX A175/176/255/256	180	
MCX A343/344/345/346/355/356/365/366	180	

5 MCX A system clocking

In the MCX A series, the low/mid-range MCX A13x/A14x/A15x parts share one common SCG-Lite clock architecture, while the higher-performance MCX A17x/18x/25x/26x parts mainly differ by adding higher clock capability and PLL support rather than a fundamentally different system clock concept.

Table 7. MCX A series system clocking architecture

MCX A group	System clock module / architecture	Main internal sources	External oscillator	PLL
MCX A13x/14x / 15x	SCG-Lite with one SCG instance (SCG0)	FRO192M FRO12M FRO16K	8–50 MHz	No
MCX A175/176 / 255/256	SCG0 with FRO180M and PLL	FRO180M FRO12M FRO16K	8–50 MHz	Yes
MCX A185/186 / 265/266	SCG0 with FRO180M configurable to 240 MHz and PLL	FRO180M FRO12M FRO16K	8–50 MHz	Yes

6 Pinout decisions example

When migrating a design from MCX A346/345 to MCX A344/343, pin assignment choices made early in the development of the original design directly affect how much hardware rework is needed later. This section illustrates how to evaluate pinout decisions so that the resulting layout remains portable across the MCX A34x family.

As a rule, signals should be assigned to the lowest available instance of each peripheral (for example LPUART0/1 instead of LPUART4/5, or ADC0/1 instead of ADC2/3) whenever functionally possible. Lower-index

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instances are present on all MCX A34x variants, while higher-index instances are only available on the higher-end devices and are typically not rerouted to lower-index peripherals on the cost-optimized parts.

Designers should also check, for the specific package being targeted, which pins expose the required peripheral signals and whether alternative pin-mux options (for example INPUTMUX-based routing) can be used to recover functionality that is not directly available through standard multiplexing. Reviewing these aspects during the initial pinout definition reduces the risk of layout changes being required after migrating to a reduced-pin-count device.

7 LPUART and I2C porting considerations

When migrating, for example, from MCX A346/345 to MCX A344/343, special attention must be paid to the reduced number of peripherals and their mapping flexibility.

Note: *Use peripherals with lower instance indexes when designing firmware and hardware mappings. This approach simplifies migration, as lower-index instances are more likely to be preserved across device variants.*

7.1 LPUART reduction (6 → 4)

The MCX A346 provides six LPUART instances, whereas the MCX A344 and MCX A343 provide only four. This is one of the most significant functional differences between these devices. If the original MCX A346 or MCX A345 design uses higher-index LPUART instances, such as LPUART4 or LPUART5, migration requires changes to the hardware design.

7.2 I2C reduction (4 → 2)

Although I2C is available on all devices, the MCX A344 and MCX A343 provide fewer I2C instances and more limited pin-multiplexing options than the MCX A346 and MCX A345. When redesigning the hardware, verify the availability of the required I2C instances and carefully review the associated pin-multiplexing options.

7.3 Pin multiplexing flexibility

Despite the reduced peripheral count, pin-multiplexing flexibility can partially compensate for missing signals:

Some pins that are not available as, for example, LPUART4 signals on MCX A344/343 may instead support TRIG_IN, TRIG_OUT signals.

Attention: *This option is available only for specific signals, check this availability in the design phase for the dedicated device and package.*

These signals can be internally connected to LPUART or other peripherals via INPUTMUX internal routing mechanisms.

This enables:

- Additional flexibility in dense designs
- Possibility to maintain functionality even with limited pin availability
- Better utilization of available pins in cost-optimized packages

7.4 LPUART example

In the Pins tool, assign `TRIG_IN` to the Rx signal and `TRIG_OUT` to the Tx signal of the unavailable UART instance. Then, in the INPUTMUX peripheral, connect `TRIG_OUT` to an available UART instance.

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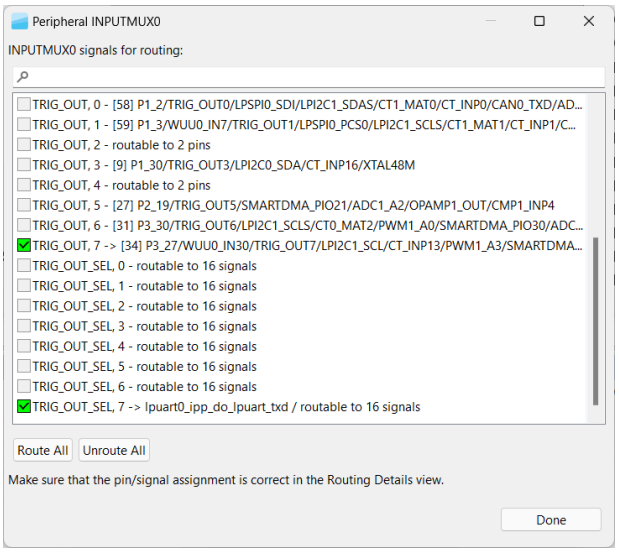


Figure 2. Pins tool trigger setup

In the dedicated LPUART, select the trigger signal.

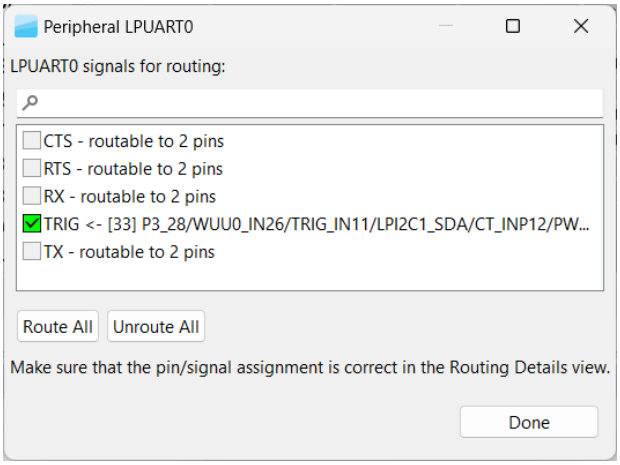


Figure 3. Pins tool LPUART trigger setup

In LPUART initialization, add the following line of code:

Note about the source code in the document

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```
LPUART0->PINCFG = LPUART_PINCFG_TRGSEL(0b01);
```

8 Analog subsystem

Migration from MCX A346/345 to MCX A344/343 introduces notable reductions in analog peripheral resources, particularly in ADC and OPAMP availability.

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An overview of the ADC and OPAMP resources is provided below:

Table 8. ADC and OPAMP peripheral comparison (MCX A346 vs MCX A343/344)

Peripheral	MCX A346	MCX A343/344
LPADC	4	2
OPAMP	4	3 (package-dependent)
CMP	3	3

ADC (LPADC)

- MCX A346/345 integrates four ADC modules
- MCX A344/343 devices provide two ADC modules

Operational Amplifiers (OPAMP)

- MCX A346/345 provides four OPAMPs
- MCX A344/343 provides three OPAMPs (smaller packages, for example, QFN32 may expose only 1 OPAMP)

CMP (analog comparators)

- Overcurrent protection is fully supported by all MCX A34x on all three phases, all OPAMP outputs.

9 Impact on three-shunt motor control (optimized use case)

In applications such as three-shunt motor control, the reduced analog resources of MCX A344/343 can still be sufficient when the system is designed accordingly.

Adjusted design assumptions:

- Three internal OPAMPs are used exclusively for phase current sensing
- Partially sequential ADC sampling is acceptable for the target drive performance

Under these conditions, the migration impact is significantly reduced.

10 OPAMP utilization

MCX A344/343 provide three OPAMPs, which can be directly assigned to:

- Phase A current
- Phase B current
- Phase C current

This enables a fully internal three-shunt current sensing solution without external amplifiers.

11 ADC sampling strategy

MCX A346/345 provide up to 4x ADC modules, while MCX A344/343 provide 2x ADC modules.

By default, for MCX A344/343 partially sequential sampling of phase currents is required.

When properly designed, sequential sampling does not limit control performance for many motor control applications. Alternatively, if an op-amp does not support internal routing for full parallel sampling, route its output externally to an ADC input pin.

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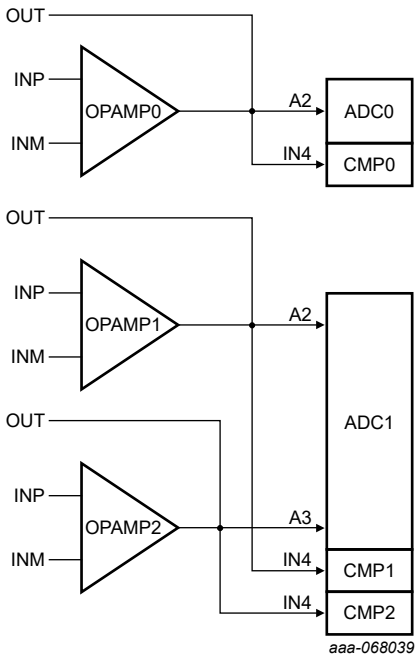


Figure 4. MCX A344/343 internal OPAMPs

Figure 4 shows the internal routing of OPAMPs and ADCs on MCX A343 and MCX A344. True parallel sampling is possible when the design connects one OPAMP (1 or 2) output to a free ADC0 channel on an MCU pin.

12 Important design rule – ADC instance selection

When designing a product intended to be initially evaluated on MCX A346/345 or later ported to MCX A344/343, it is recommended to use lower-index ADC instances (ADC0, ADC1). The reason is that higher-index ADC instances (ADC2, ADC3) available on MCX A346/345 do not exist on MCX A344/343. Their input pins are typically not rerouted or internally connected to lower-index ADCs.

As a result, the signals connected to higher-index ADC inputs on MCX A346 cannot be easily remapped in hardware and may require PCB redesign.

Using higher ADC instances during development can lead to:

- Loss of analog input channels after migration
- Unavailable pin mappings on cost-optimized devices

13 Memory constraints example

One of the primary differences between MCX A346/345 and MCX A344/343 devices is the available on-chip memory, which directly impacts firmware portability.

Table 9. Flash and SRAM memory comparison (MCX A343/344/345/346)

Memory type	MCX A346	MCX A345	MCX A344	MCX A343
Flash	1 MB	512 KB	256 KB	128 KB
Total SRAM	256 KB	128 KB	64 KB	32 KB

The 8 KB CMPA region at the end of the flash memory reduces the space available for user code. For example, MCX A343 provides 120 KB for user code.

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Table 10. MCX A34x memory map (code bus and system bus address ranges)

Memory			MCX A345 MCX A355	MCX A365	MCX A346 MCX A356	MCX A366
Code bus memory [1]						
Flash	User Flash	Start	0x00000000	0x00000000	0x00000000	0x00000000
		End	0x0007DFFF	0x0006FFFF	0x000FDFFF	0x000EFFFF
	Secure Installer	Start	—	0x00070000	—	0x000F0000
		End	—	0x0007DFFF	—	0x000FDFFF
	CMPA [2]	Start	0x0007E000	0x0007E000	0x000FE000	0x000FE000
		End	0x0007FFFF	0x0007FFFF	0x000FFFFF	0x000FFFFF
SRAM	SRAM X0	Start	0x04000000	0x04000000	0x04000000	0x04000000
		End	0x04001FFF	0x04001FFF	0x04001FFF	0x04001FFF
	SRAM X1	Start	0x04002000	0x04002000	0x04002000	0x04002000
		End	0x04003FFF	0x04003FFF	0x04003FFF	0x04003FFF
System bus RAM						
SRAM	SRAM A0	Start	0x20000000	0x20000000	0x20000000	0x20000000
		End	0x20001FFF	0x20001FFF	0x20001FFF	0x20001FFF
	SRAM A1	Start	0x20002000	0x20002000	0x20002000	0x20002000
		End	0x20002FFF	0x20002FFF	0x20002FFF	0x20002FFF
	SRAM A2	Start	0x20003000	0x20003000	0x20003000	0x20003000
		End	0x20003FFF	0x20003FFF	0x20003FFF	0x20003FFF
	SRAM A3	Start	0x20004000	0x20004000	0x20004000	0x20004000
		End	0x20007FFF	0x20007FFF	0x20007FFF	0x20007FFF
	SRAM A4	Start	0x20008000	0x20008000	0x20008000	0x20008000
		End	0x2000FFFF	0x2000FFFF	0x2000FFFF	0x2000FFFF
	SRAM B0	Start	0x20010000	0x20010000	0x20010000	0x20010000
		End	0x20017FFF	0x20017FFF	0x20017FFF	0x20017FFF
	SRAM B1	Start	0x20018000	0x20018000	0x20018000	0x20018000
		End	0x2001DFFF	0x2001DFFF	0x2001FFFF	0x2001FFFF
	SRAM C0	Start	—	—	0x20020000	0x20020000
		End	—	—	0x20027FFF	0x20027FFF
	SRAM C1	Start	—	—	0x20028000	0x20028000
		End	—	—	0x2002FFFF	0x2002FFFF
	SRAM C2	Start	—	—	0x20030000	0x20030000
		End	—	—	0x20037FFF	0x20037FFF
	SRAM C3	Start	—	—	0x20038000	0x20038000
		End	—	—	0x2003BFFF	0x2003BFFF
	SRAM X0 Alias [3]	Start	0x2001E000	0x2001E000	0x2003C000	0x2003C000

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Table 10. MCX A34x memory map (code bus and system bus address ranges)*...continued*

Memory			MCX A345 MCX A355	MCX A365	MCX A346 MCX A356	MCX A366
		End	0x2001FFFF	0x2001FFFF	0x2003DFFF	0x2003DFFF

[1] Users are recommended to place code in the code bus memory range to improve code execution performance.

[2] Customer Manufacturing/Factory Configuration Area (CMPA).

[3] SRAM X0 is enabled in Alias mode by default.

14 SRAM architecture and constraints

In addition to the reduction in total RAM size, MCX A series devices implement a split SRAM architecture, where memory is divided into regions connected to different internal buses but the SRAM memory addresses are designed in a contiguous way so that SRAM blocks can be fully usable.

The SRAM organization is shown below.

MCX A devices partition SRAM into:

- SRAM (system SRAM) – connected to the core system/data bus
- SRAMX (code SRAM) – connected to the code (instruction) bus

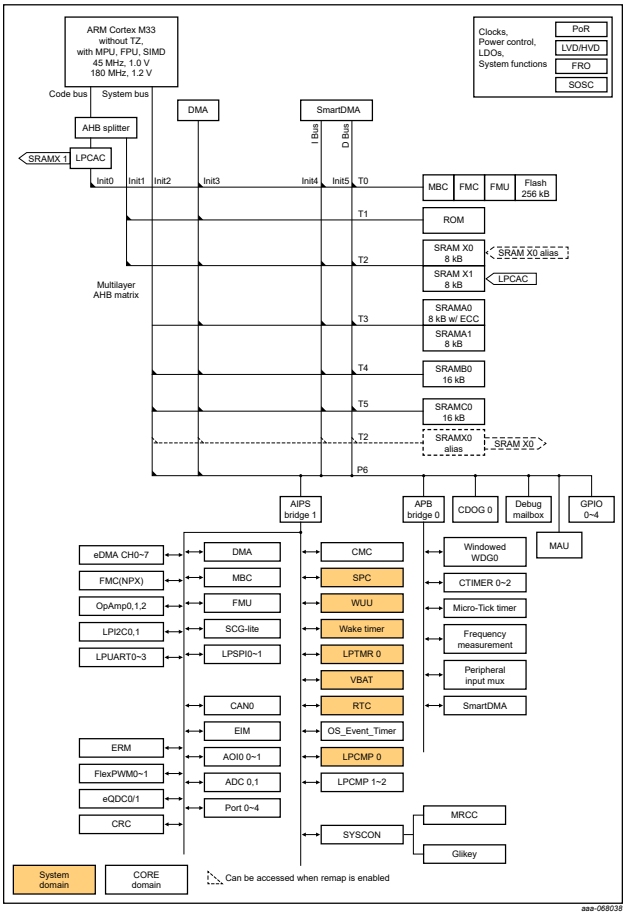


Figure 5. Memory diagram of MCX A344/343

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Key Fact

- SRAMX size is always 16 KB SRAM (X0: 8 KB, SRAM X1: 8 KB) across MCX A34x devices

Example MCX A344

- The 64 KB total SRAM is split as:
  - 48 KB SRAM
  - 16 KB SRAMX

Example MCX A343

- The 32 KB total SRAM is split as:
  - 16 KB SRAM
  - 16 KB SRAMX

14.1 Alternative memory organization (alias mode)

SRAMX can be partially remapped to system SRAM. SRAMX0 alias is visible in the diagram.

Example for MCX A343:

- Default memory layout: 16 KB SRAM / 16 KB SRAMX
- Alternative memory layout: 24 KB SRAM / 8 KB SRAMX

Requirements

- Linker modification
- Startup code update

Benefit

- Increased usable data memory
- Reduced code execution space

For details, see *Continuous SRAM Address Usage on MCX A15x* (document AN14377).

15 Code optimization considerations

When migrating, for example, from MCX A346/345 to MCX A344/343, the significant reduction in Flash memory requires more aggressive compiler optimization, which can introduce additional challenges beyond simple code size reduction. Use the target MCU SDK project framework for the final application project, then add the related code into the project. This helps reduce manual modification of the linker files for memory allocation, startup file (including vector table), and clock configuration.

The code may require:

- Additional volatile qualifiers
- Refactoring of polling loops
- Replacement of delay loops with timer-based delays
- Cleanup of undefined or nondeterministic behavior
- Disabling optimization for parts of code

Best practices

- Use optimization early
- Enable size optimization already during MCX A346/345 development
- Avoid “debug-only” builds that hide problems

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16 Conclusion

The MCX A series offers a broad range of features tailored to diverse embedded applications. Device selection is primarily driven by application-specific requirements, including the necessary peripherals, feature set, and memory capacity. While a fully universal migration path across all MCX A devices is not feasible, the family provides consistent architectural elements and shared peripheral groups, with variations mainly in the number of available instances.

Porting designs from higher-end devices such as MCX A346/345 to cost-optimized variants like MCX A344/343 can be achieved with minimal effort, provided that resource constraints are considered early in the design phase. Although these lower-cost devices feature reduced memory and fewer peripherals, they remain well-suited for a wide range of applications—including motor control—when efficient design practices and resource optimization are applied.

17 Acronyms and abbreviations

The following table lists the acronyms and abbreviations used in this document.

Acronym or abbreviation	Definition
ADC	Analog-to-digital converter
AHB	Advanced High-performance Bus
AIPS	Advanced peripheral bus interface
AOI	AND/OR/Invert
APB	Advanced Peripheral Bus
CAN	Controller Area Network
CMP	Comparator
CMPA	Customer Manufacturing/Factory Configuration Area
CPU	Central processing unit
CRC	Cyclic redundancy check
DAC	Digital-to-analog converter
DMA	Direct memory access
DSP	Digital signal processing
ECC	Error-correcting code
EIM	Error injection module
ERM	Error Reporting Module
FMC	Flash memory controller
FMU	Flash management unit
FPU	Floating-point unit
FRO	Free-running oscillator
GPIO	General-purpose input/output
HMI	Human-machine interface
HVD	High-voltage detector
I2C	Inter-Integrated Circuit

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Acronym or abbreviation	Definition
I3C	Improved Inter-Integrated Circuit
INPUTMUX	Input multiplexer
LCD	Liquid-crystal display
LDO	Low-dropout regulator
LPADC	Low-power analog-to-digital converter
LPCAC	Low-power code bus access controller
LPCMP	Low-power comparator
LPI2C	Low-power Inter-Integrated Circuit
LPSPI	Low-power serial peripheral interface
LPTMR	Low-power timer
LPUART	Low-power universal asynchronous receiver/transmitter
LVD	Low-voltage detector
MAU	Math acceleration unit
MBC	Memory block checker
MCU	Microcontroller unit
MPU	Memory protection unit
MRCC	Module reset and clock control
OPAMP	Operational amplifier
PCB	Printed circuit board
PLL	Phase-locked loop
PWM	Pulse-width modulation
RAM	Random-access memory
ROM	Read-only memory
RTC	Real-time clock
SCG	System clock generator
SDK	Software development kit
SIMD	Single instruction, multiple data
SOSC	System oscillator
SPC	System power controller
SPI	Serial peripheral interface
SRAM	Static random-access memory
SRAMX	Code-bus static random-access memory
SYSCON	System controller
UART	Universal asynchronous receiver/transmitter
VBAT	Battery-supply domain
WDG	Watchdog timer
WUU	Wake-up unit

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18 Revision history

Table 11. Revision history

Document ID	Release date	Description
AN15223 v.1.0	18 November 2026	Initial version

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