AN15145

Peripheral Enablement in Low-Power Modes in MCX L255

Rev. 1.0 — 27 August 2026 Application note

Document information

Information	Content
Keywords	AN15145, MCX L255, peripheral enablement, AON, RTC, Main domain, power modes, Low-power mode, functional domains
Abstract	This application note describes the requirements for enabling peripherals across different Low-power modes.

1 Introduction

The MCX L255 device provides a flexible low-power architecture that allows applications to balance power consumption and peripheral functionality. Depending on the selected power mode, peripherals located in the Main domain or the Always-On (AON) domain can continue operating, require other configuration, or become unavailable.

This application note describes the requirements for enabling peripherals across different Low-power modes. This application note explains the register configurations needed to maintain peripheral operation when transitioning from Active mode into low-power states.

For more details on Low-power modes and available wake-up sources, see the *Implementing MCX L25 Low-Power Mode* (AN14949).

2 MCX L255 Low-power modes overview

To support power-sensitive applications, the MCX L255 provides the following nine power modes:

- Active (All On)
- Sleep
- Deep-Sleep (DS)
- Power-Down 1 (PD1)
- Power-Down 2 (PD2)
- Deep-Power-Down 1 (DPD1)
- Deep-Power-Down 2 (DPD2)
- Deep-Power-Down 3 (DPD3)
- Shutdown

The availability of peripherals depends on the domain in which they reside.

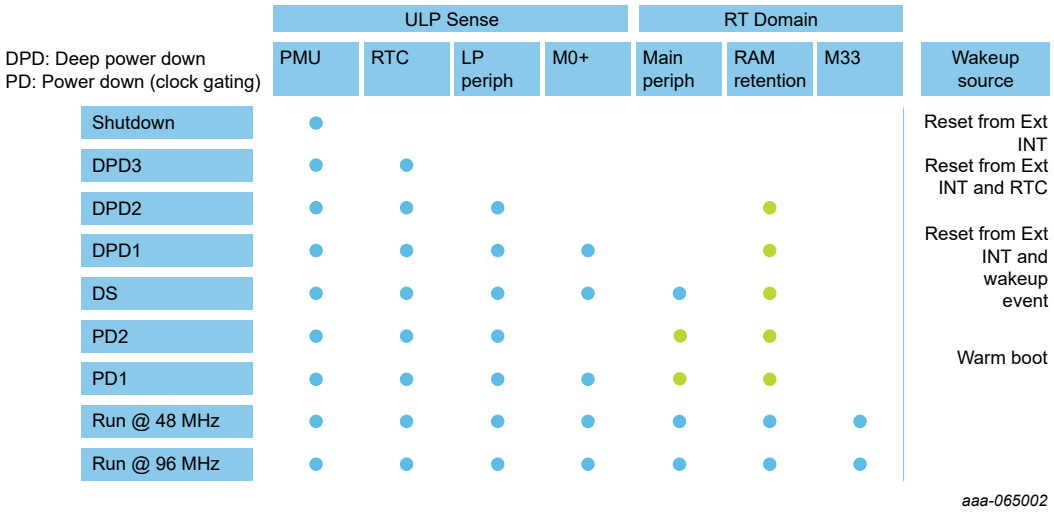

Figure 1. Domain states in Low-power mode

3 Main domain peripheral enablement

The Main domain is the area where most of the computational capabilities of the device are situated. Therefore, it is also known as the Compute domain. This domain is used in scenarios where the computational capabilities of the CM33 core or the security accelerators are required. The domain also instantiates the long-term storage

components such as the internal flash memory of the device and more feature-packed ADC (though more power consuming), and analog comparator modules.

3.1 Active mode

In Active mode, all clocks are available and peripherals operate normally.

3.1.1 Required configuration

The following is the required configuration:

- Select a peripheral functional clock.
- Enable a peripheral clock.
- Release peripheral from reset.

For example, to enable CTimer0 in Active mode:

```
/* Enable clock */
SYSCON->AHBCLKCTRLSET[0] = SYSCON_AHBCLKCTRL0_CTIMER0_MASK;
/* Release reset */
SYSCON->PRESETCTRLCLR[0] = SYSCON_PRESETCTRL0_CTIMER0_RST_MASK;
```

3.2 Sleep mode

In Sleep mode, Main-domain peripheral clocks remain active while the CM33 enters WFI state.

3.2.1 Required configuration

No additional settings are required compared to Active mode.

3.3 DS mode

In DS mode:

- Main-domain peripherals are automatically clock gated.
- FIRC is disabled by default.
- Peripheral functionality can be maintained through SIRC, ROSC, or FRO16K.

3.3.1 Required configuration

The following is the required configuration:

1. Switch peripheral clock source: Use any of the following to attach SIRC to the peripheral.

```
CLOCK_SetupFRO12MClocking();              /* Setup FRO12M clock */
CLOCK_AttachClk(kFRO12M_to_CTIMERg0);
```

```
/* Initialize Rosc if not already initialized */
    if (!CLOCK_IsRoscInitialized())
    {
        AON__CGU->CLK_CONFIG |= CGU_CLK_CONFIG_XTAL32_OUT_EN_MASK;
        /* Get default Rosc initialization configuration */
        CLOCK_GetDefaultInitRoscConfig(&roscInitConfig);
        /* Configure Rosc initialization for FRDM-MCXL255 for faster init*/
        roscInitConfig.detectionDelay = 50U;
```

```
        roscInitConfig.detectionTimeout = 0U;
        roscInitConfig.detectionDelaySwitchedMode = 50U;
        roscInitConfig.detectionTimeoutSwitchedMode = 50U;
        CLOCK_InitRosc(&roscInitConfig);
    }
CLOCK_AttachClk(kCLK_16K_LS_to_CTIMERg0);
```

2. Enable SIRC in the DS: Enable SIRC standby operation:

```
SCG0->SIRCCSR |= SCG_SIRCCSR_SIRCSTEN_MASK;
```

Table 1. Register field

Register	Bit	Description
SIRCCSR	SIRCSTEN	It keeps SIRC running in DS

3. Disable automatic clock gating: Automatic clock gating must be disabled for peripherals required during DS. Example:

```
GLB->ACCCTL0 |= GLB_ACCCTL0_FLEXCOMM0_MASK;
```

Table 2. Register field

Register	Description
GLB_ACCx	Controls peripheral clock gating behavior during low-power entry

4. Enable peripheral clock:

```
SYSCON->AHBCLKCTRLSET[0] =
    SYSCON_AHBCLKCTRL0_FLEXCOMM0_MASK;
```

5. Release peripheral reset:

```
SYSCON->PRESETCTRLCLR[0] =
    SYSCON_PRESETCTRL0_FLEXCOMM0_RST_MASK;
```

Summary: Main-domain peripherals can operate in DS, if:

- Clock source is changed to SIRC, ROSC, and FRO16K.
- SIRC, ROSC, and FRO16K remain enabled in low power.
- Automatic clock gating is disabled.
- Peripheral clocks remain enabled.

3.4 PD1 mode

In PD1 mode, main domain power is removed. Therefore, main domain peripherals cannot operate in PD1 mode.

3.5 PD2 mode

In PD2 mode, main domain power is removed. Therefore, main domain peripherals cannot operate in PD2 mode.

3.6 DPD1 mode

In DPD1 mode, main domain power is removed. Therefore, main domain peripherals cannot operate in DPD1 mode.

3.7 DPD2 mode

In DPD2 mode, main domain power is removed. Therefore, main domain peripherals cannot operate in DPD2 mode.

3.8 DPD3 mode

In DPD3 mode, main domain power is removed. Therefore, main domain peripherals cannot operate in DPD3 mode.

3.9 Shutdown mode

In the Shutdown mode, main domain power is removed. Therefore, main domain peripherals cannot operate in the Shutdown mode.

4 AON domain peripheral enablement

The AON domain operates under the ADVC, which operates effectively at a maximum frequency of 10 MHz. The user code must enable the ADVC operation. However, it runs independently in the background down to DPD2/PD2 mode. The user can use this domain to perform low power computation using the CM0+ core along with serial peripherals like LPI2C/LPUART/LCSense/LPACMP/LPADC and Timers that can count external events or generate output triggers.

4.1 Active Mode

In Active mode, enable clocks and release reset.

4.1.1 Required configuration

The following is the required configuration:

- Enable a peripheral clock.
- Release peripheral from reset.
- Select a peripheral functional clock.

For example, to enable LPTimer0 in Active mode:

```
/* Select clock */
CLOCK_AttachClk(kFROdiv4_to_AON_TMR);
CLOCK_AttachClk(AON_TMR_to_AON_LPTMR);
/* Enable clock */
CLOCK_EnableClock(kCLOCK_LPTMR0);
/* Release reset */
RESET_ClearPeripheralReset(kLPTMR0_RST_SHIFT_RSTn);
```

4.2 Sleep mode

No additional settings are required compared to Active mode.

4.3 DS mode

No additional settings are required compared to Active mode.

4.4 PD1 mode

No additional settings are required compared to Active mode.

4.5 PD2 mode

No additional settings are required compared to Active mode.

4.6 DPD1 mode

No additional settings are required compared to Active mode.

4.7 DPD2 mode

In DPD2 mode, if PWDN_CONFIG[AON_DPD_CLK_SEL] = 0, then the LPIRC and ULPIRC clocks are turned off and the core clock switches to 32 kHz clock. The peripherals clocked using LPIRC or ULPIRC stop working on entering DPD2 mode. To keep the peripherals running in DPD2 mode, set the AON_DPD_CLK_SEL bit to 1 or switch peripherals to 32 kHz or FRO 16 kHz clock before entering DPD2 mode.

For example, to switch the LPTimer0 clock to 32 kHz or 16 kHz in DPD2 mode:

```
/* Select clock */
/* XTAL 32KHz clock */
CLOCK_EnableClock(kCLOCK_GateAonAPB);
BOARD_BootClockFRO10M_InitClockModule(kClockModule_ROSC);
CLOCK_AttachClk(kROOT_AUX_to_AON_TMR);
CLOCK_AttachClk(AON_TMR_to_AON_LPTMR);
Or
/* FRO 16KHz clock */
CLOCK_EnableClock(kCLOCK_GateAonAPB);
BOARD_BootClockFRO10M_InitClockModule(kClockModule_FRO16K);
CLOCK_AttachClk(kFRO16K_to_AON_LPTMR);
```

4.8 DPD3 mode

AON peripherals are not operational in DPD3 mode.

4.9 Shutdown mode

AON peripherals are not operational in Shutdown mode.

5 RTC domain peripheral enablement

The RTC domain comprises of only the RTC logic. Due to the inherent low power operation of RTC, it is designed to run at approximately 0.5 V (sub-Threshold) while operating at a clock frequency of 32.768 kHz and sourcing from an external oscillator (ROSC) to support accurate timekeeping.

6 Acronyms

Table 3 lists the acronyms used in this document.

Table 3. Acronyms

Acronym	Description
AON	Always-On
DPD	Deep-Power-Down
DS	Deep-Sleep
FIRC	Fast Internal Reference Clock
PD	Power-Down
SIRC	Slow Internal Reference Clock
WFI	Wait For Interrupt

7 Revision history

Table 4 summarizes the revisions to this document.

Table 4. Revision history

Document ID	Release date	Description
AN15145 v.1.0	27 August 2026	Initial public release

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