AN15106

PCA8525/PCF8525TK Temperature Compensation Engine

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Document information

Information	Content
Keywords	AN15106, PCA8525, PCF8525TK, RTC, crystal, accuracy, timekeeping, drift, aging, compensation, temperature, real time clock
Abstract	This application note describes the use of the PCA8525/PCA8525TK internal temperature compensation engine to correct frequency drift of a typical crystal (selectable between −0.035 ppm/°C² and −0.04 ppm/°C²), achieving up to 5× improved timekeeping accuracy compared to a standard RTC without an internal temperature compensation engine.

1 Introduction

This application note demonstrates the PCA8525 and PCF8525TK integrated temperature compensation feature to mitigate the crystal frequency drift and improve timekeeping accuracy.

PCA8525/PCF8525TK also includes an on-chip oscillator detection circuit, which indicates the status of oscillations, as well as an on-chip supply voltage detection circuit, which indicates the low status of the supply voltage. When the supply is below VLOW, the Voltage Low Flag (VLF) is set to logic 1. When the oscillator stops, the Oscillator Stop Flag (OSF) is set to logic 1.

A Real-Time Clock (RTC) is an electronic device that keeps track of current time. RTCs are commonly used on computers and servers but find use in many different embedded applications where independent timekeeping is essential. Not all applications require the same level of accuracy, but when higher accuracy is needed, a standard RTC cannot fulfill these requirements.

An essential feature that goes with reliable timekeeping is its accuracy. It is not acceptable to have a timekeeping system that drifts for several minutes per day.

Several factors such as humidity, vibration, and pressure can influence RTC accuracy; as well as the proximity of the quartz crystal to the RTC IC and its layout. However, the primary source of deviation is the inherent variation of quartz crystal characteristics over temperature.

The PCA8525 and PCF8525TK are the first RTC IC (which requires external crystal) to feature a default temperature compensation engine. It compensates for a typical crystal model, which can be selected as either −0.035 ppm/°C² or −0.04 ppm/°C². This compensation improves timekeeping accuracy by up to 5× compared to a conventional RTC IC that does not include an internal temperature-compensation engine.

2 PCA8525 and PCF8525TK Temperature Compensation

The frequency of tuning fork quartz crystals is temperature-dependent. A typical (ideal) crystal response to temperature is shown in Figure 1. This ideal response can be modeled using a temperature coefficient of -0.035 ppm/°C², and assuming the crystal is calibrated to 0 ppm at 25 °C. This means that a tuning fork crystal oscillator resonates close to its target frequency at 25 °C but slows down when the temperature either increases or decreases.

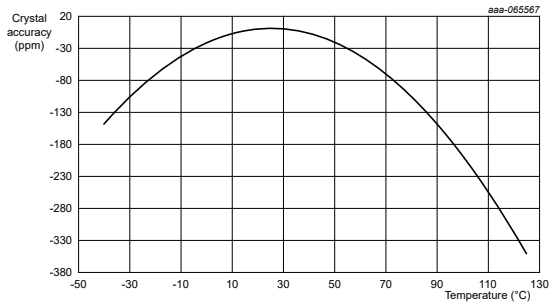

Figure 1. Typical crystal response to temperature

The behavior shown in Figure 1 is described by the following equation:

$$f = f_0 \left[1 + B(T - T_0)^2\right] \quad (1)$$

Here f is the actual frequency, f_0 is the frequency at room temperature, B is the parabolic coefficient, T is the temperature, and T_0 is the turnover temperature.

The coefficient B has a small spread for various crystals of the same type. However, it has the largest effect on the shape of the parabolic curve representing frequency deviation as a function of temperature.

The crystal manufacturer specifies the parabolic coefficient B and the turnover temperature T_0 parameters. The PCA8525/PCF8525TK compensates for a typical 32.768 kHz crystal model with temperature coefficients of -0.035 ppm/°C² or -0.04 ppm/°C² (configurable).

The crystal mounted on the PCF8525-ARD has a typical temperature coefficient of −0.034 ppm/°C²; therefore, the −0.035 ppm/°C² configuration is suitable.

2.1 PCA8525/PCF8525TK temperature measurement

The PCA8525/PCF8525TK has a temperature sensor circuit used to perform temperature compensation of the clock input to the RTC. The temperature is measured after power on and then periodically with a period set by the temperature conversion rate TCR [2:0] in the register CLKOUT_ctl. During the first approximately 60 s after startup, temperature compensation remains inactive. After this period, temperature compensation becomes active.

At every temperature compensation interval, the integrated temperature sensor records the ambient temperature of the IC. The temperature compensation engine estimates the error of the crystal at this temperature (using Figure 1) and applies an equal and opposite compensation to the internal digital clock.

2.2 PCA8525/PCF8525TK Temperature Compensation Register flow

This section describes the PCA8525/PCF8525TK temperature compensation register flow through the flowchart presented in Figure 2. The flowchart provides an overview of the register configuration process, Section 2.3 provides a description of the main registers involved in temperature compensation, their default reset values, and the OSF and VLF status flags. These flags are essential for ensuring correct RTC operation.

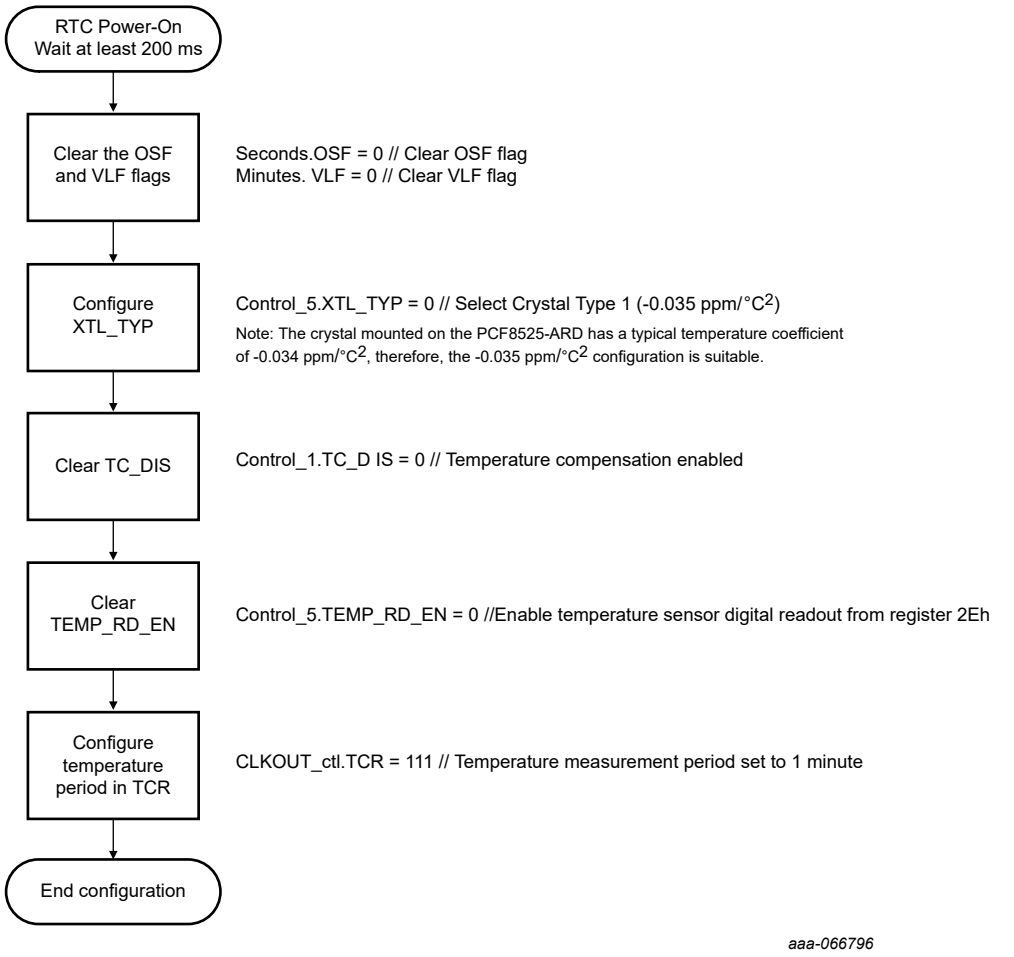

Figure 2. Temperature Compensation Register Flow

The Power-On Reset (POR) is active whenever the oscillator is stopped. The oscillator is considered stopped during the time between power on and stable crystal resonance. This time can be in the range of 200 ms to 2 s depending on temperature and supply voltage.

2.3 PCA8525/PCF8525TK Temperature Compensation Engine Register description

This section provides a brief description of the PCA8525/PCF8525TK registers introduced in the previous section.

Table 1 describes the Seconds register (Register Address 07h) and its reset value.

Table 1. Seconds - seconds and clock integrity register (address 07h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	**OSF**	SECONDS (0 to 59)						
Reset value	**1**	0	0	0	0	0	0	0

Table 2 describes the two possible OSF values and their descriptions.

Table 2. OSF bit value description

Symbol	Value	Description
OSF	0	No oscillator stop occurred. For correct RTC operation, OSF must be cleared manually (Seconds.OSF = 0)
	1	Oscillator stop occurred. The oscillator is not running and the chip is in reset

Table 3 describes the Minutes register (Register Address 08h) and its reset value.

Table 3. Minutes - minutes register (address 08h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	**VLF**	MINUTES (0 to 59)						
Reset value	**1**	0	0	0	0	0	0	0

Table 4 describes the two possible VLF values and their descriptions.

Table 4. VLF bit value description

Symbol	Value	Description
VLF	0	Clock integrity is guaranteed. For correct RTC operation, VLF must be cleared manually (Minutes.VLF = 0)
	1	I2C integrity is not guaranteed; Clock and timing keeping function can still work down to supply voltage = 0.9 V

Table 5 describes the Register Control_5 (Register Address 04h), and its reset value.

Table 5. Control_5 - control and status register 5 (address 04h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TSIE	-	-	-	-	TEMP_RD_EN	R	**XTL_TYP**
Reset value	0	0	0	0	0	0	0	**0**

Table 6 describes the two possible XTL_TYP values and their descriptions.

Table 6. XTL_TYP – XTL_TYP bit value description

Symbol	Value	Description
XTL_TYP	0	Crystal type 1 model (-0.035 ppm/°C^2) used for temperature compensation
	1	Crystal type 2 model (-0.04 ppm/°C^2) used for temperature compensation

Table 7 describes the Register Control_1 (Register Address 00h), and its reset value.

Table 7. Control_1 - control and status register 1 (address 00h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	R	**TC_DIS**	STOP	100^{TH}_S_DIS	R	12_24	MI	SI
Reset value	0	**0**	0	0	1	0	0	0

Table 8 describes the two possible TC_DIS values and their descriptions.

Table 8. TC_DIS bit value description

Symbol	Value	Description
TC_DIS	0	Temperature compensation enabled
	1	Temperature compensation disabled

Table 9 describes the Register Control_5 (Register Address 04h), and its reset value.

Table 9. Control_5 - control and status register 5 (address 04h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TSIE	-	-	-	-	**TEMP_RD_EN**	R	XTL_TYP
Reset value	0	0	0	0	0	**0**	0	0

Table 10 describes the two possible TEMP_RD_EN values and their descriptions.

Table 10. TEMP_RD_EN– TEMP_RD_EN bit value description

Symbol	Value	Description
TEMP_RD_EN	0	Enable temperature sensor digital readout from register 2Eh
	1	Disable temperature sensor digital readout from register 2Eh

Table 11 describes the bit arrangement of the Temperature Register data.

Table 11. Temperature Register

Bit	7	6	5	4	3	2	1	0
Symbol	TEMP [7:0]							
Reset value	0	0	0	0	0	0	0	0

TEMP[7:0] = Digital result of the temperature measurement from the most recent analog-to-digital conversion.

Note: *After power up or reset, TEMP[7:0] = 0 °C.*

Table 12 describes the CLKOUT_ctl - CLKOUT control register (address 15h), and its reset value.

Table 12. CLKOUT_ctl - CLKOUT control register (address 15h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	**TCR[2:0]**			OTPR	CLKOE	COF[2:0]		
Reset value	**0**	**0**	**0**	X	1	0	0	0

Table 13 describes examples of the Temperature Register data and value.

Table 13. Temperature register values

TCR[2:0]	Temperature measurement period
000(default)	32 minutes
001	16 minutes
010	8 minutes

Table 13. Temperature register values...*continued*

TCR[2:0]	Temperature measurement period
011	4 minutes
100	2 minutes
101	1 minute
110	1 minute
111	1 minute

3 How to calculate error in ppm

At the heart of every RTC circuit is a resonator that produces the oscillations required to generate a stable clock. It is usually a 32,768 Hz quartz crystal.

This means that the ideal resonant frequency is 32,768 Hz.

Any deviation from this ideal value is expressed in parts per million (ppm) using the formula below.

$$\text{Error in ppm} = \frac{(\text{Actual frequency} - 32{,}768) \times 10^6}{32{,}768} \tag{2}$$

3.1 Converting frequency error (ppm) to time error

A frequency error expressed in parts per million (ppm) can be converted into accumulated time error using the following equation.

$$\text{Time error}(\text{seconds}) = \text{ppm} \times \frac{\text{Elapsed time}(\text{seconds})}{10^6} \tag{3}$$

The following examples illustrate the relationship between frequency deviation and clock accuracy.

Using Equation 3, a crystal with a frequency deviation of 100 ppm has an accumulated time error per day of:

$$\frac{100 \times (3600 \times 24)}{10^6} = 8.64 \text{ seconds} / \text{day} \tag{4}$$

Since there are 60 seconds in one minute, the accumulated time error in minutes per day is:

$$\text{Time error} = \frac{8.64}{60} = 0.144 \text{ min} / \text{day} \tag{5}$$

Therefore, a crystal with a frequency deviation of 100 ppm accumulates approximately 8.64 seconds (0.144 minutes) error per day.

Table 14 provides the calculated time error associated with a 100 ppm oscillator accuracy specification for several elapsed time periods, from one hour to one year.

Table 14. Time Error for a frequency deviation of 100 ppm

Elapsed time	Elapsed time (seconds)	Time error (seconds)	Time error (minutes)
1 hour	3,600	0.36	0.006
1 day	86,400	8.64	0.144
1 week	604,800	60.48	1.008
1 month (30 days)	2,592,000	259.2	4.32
1 year (365 days)	31,536,000	3,153.6	52.56

4 Evaluation board

4.1 PCF8525-ARD

The PCF8525-ARD is an evaluation board that can be connected through an Arduino port to various Arduino compatible (including original Arduino UNO R3) boards. The board is equipped with a battery holder allowing the user to test the battery switch-over circuit of the RTC. The evaluation board is intended to test and evaluate all characteristics of the silicon. These characteristics include I2C communication, power management, battery backup, timestamps, interrupts, and other internal features of the PCF8525 RTC.

Additionally, the expansion board has software support and a graphical user interface (Windows platform) for the FRDM-MCXN947 MCU EVK Board. This board contains Arduino ports, allowing the user to attach and operate from the PCF8525-ARD expansion board from the GUI. The schematic, board layout, and BOM for the PCF8525-ARD evaluation board are available.

5 Revision history

Table 15 summarizes revisions to this document.

Table 15. Revision history

Document ID	Release date	Description
AN15106 v.1.0	13 August 2026	Initial public release

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