AN15076

Multi-protocol implementation on the i.MX RT1180 MCU

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Document information

Information	Content
Keywords	AN15076, i.MX RT1180 MCU, EtherCAT, NETC, PHY, MII, RGMII
Abstract	This document describes a method for multi-protocol implementation on the i.MX RT1180 MCU that supports 100 Mbit/s (MII) and 1000 Mbit/s (RGMII) with shared hardware. The proposed method uses a single PHY with software-configurable modes, enabling both EtherCAT and NETC. It reduces complexity and lowers the cost.

1 Introduction

The NXP i.MX RT1180 crossover MCU integrates both EtherCAT and NETC Ethernet communication capabilities.

- The EtherCAT interface operates at 100 Mbit/s and typically connects to Fast Ethernet PHYs via an MII interface.
- The NETC interface supports 1000 Mbit/s operation and is commonly connected to gigabit PHYs through an RGMII interface.

Pin multiplexing is implemented between the EtherCAT and NETC interfaces. Therefore, different application scenarios require corresponding configurations of external PHY connections, IOMUX settings, clock sources, and MAC interface modes.

The MIMXRT1180-EVK (also called i.MX RT1180-EVK) board uses two dedicated PHY configurations to support EtherCAT and NETC independently:

- A 100 Mbit/s PHY connected via MII for EtherCAT
- A 1000 Mbit/s PHY connected via RGMII for NETC.

While this architecture simplifies independent functional validation, it increases hardware cost, resource consumption, and overall system complexity when switching between the two modes.

This document describes a more efficient design by using a single Ethernet PHY that supports both MII and RGMII interfaces, as well as 100 Mbit/s and 1000 Mbit/s operation. Through software reconfiguration, the PHY can operate in MII/100 Mbit/s mode for EtherCAT or switch to RGMII/1000 Mbit/s mode for NETC. This unified approach allows both communication protocols to share a single PHY, significantly reducing hardware complexity while enhancing system flexibility. So, this paper presents a system-level solution for implementing both EtherCAT and NETC functionalities using a single Ethernet PHY.

2 EtherCAT application

In the EtherCAT application, the shared Ethernet PHY is configured to operate in MII mode with a link speed of 100 Mbit/s. In this mode, the PHY is connected to the i.MX RT1180 EtherCAT controller through the MII signal group, and the system is optimized for deterministic real-time industrial communication.

This section describes the hardware connection, clock and pin multiplexing requirements, software initialization flow, and basic validation result for running EtherCAT over the shared PHY solution.

2.1 Hardware configuration

For EtherCAT operation, the external PHY is configured as a 100 Mbit/s Fast Ethernet PHY using the MII interface. The MII transmit and receive data signals, management interface signals, reference clock, and reset signal are connected between the i.MX RT1180 EtherCAT MAC and the shared PHY.

The IOMUX configuration must select the EtherCAT MII function for the corresponding pins. Since the pins are multiplexed between EtherCAT and NETC functions, the NETC RGMII pin function must be disabled when the system operates in EtherCAT mode.

The PHY can work with both MII and RGMII. However, the clock configuration for these two modes is completely different. Therefore, the hardware must meet the MII timing requirement. Typically, a 25 MHz reference clock is used for 100 Mbit/s MII operation. Figures Figure 1, Figure 2, and Figure 3 describe the hardware clock configuration.

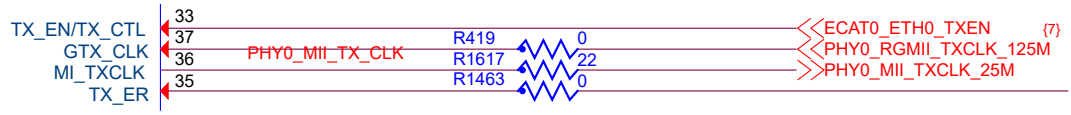

Figure 1. TX_CLK connection

As shown in Figure 1, the MII_TX_CLK works as the output from PHY side and RGMII_TX_CLK_125M works as the input from PHY side. The PHY separates these two signals to two pins.

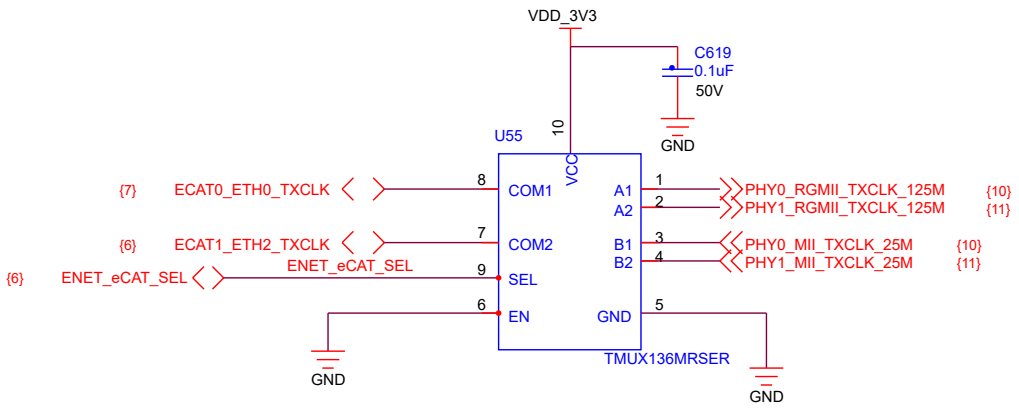

Figure 2. TX_CLK signal selection

From the MCU side, the NETC RGMII TXCLK uses the same pin as the EtherCAT MII TXCLK. Therefore, an analog switch must be used to choose the right TX_CLK signal. As shown in Figure 2, the ENET_eCAT_SEL signal connects to a GPIO of i.MX RT1180 MCU. The software code enables selection of the right signal for different modes.

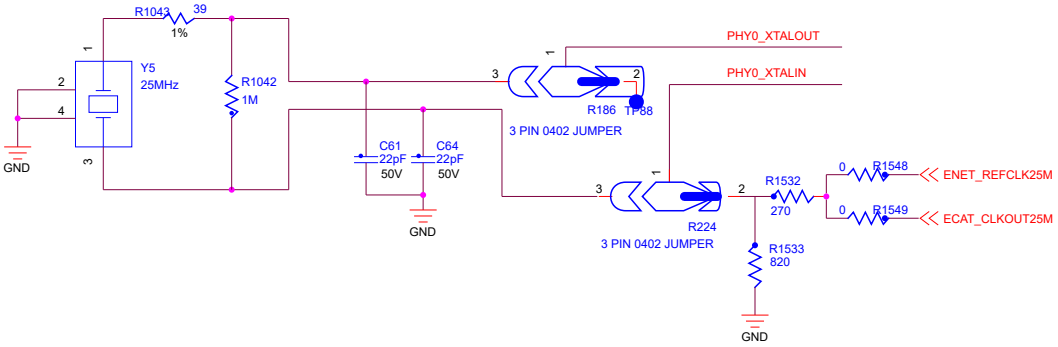

Figure 3. Selecting the reference clock

Additionally, EtherCAT has a stricter requirement for the reference clock. It is recommended to let the EtherCAT controller provide the reference clock to the PHY, so that the hardware can choose the right reference clock. As described in Figure 3, three methods for providing reference clock to the PHY are reserved in the design. Resistors are used to distinguish whether a crystal oscillator or an MCU provides the reference clock. The MCU software configuration is used to select the clock provider from the MCU.

For details of the PHY configuration used on a sample board, refer to the Section 7.

2.2 Software configuration

During EtherCAT initialization, the software first configures the IOMUX pins for the EtherCAT MII interface, I2C interface, and MDIO interface and enables the required clock sources. The PHY reset sequence is then executed to ensure that the PHY starts from a known state.

After reset, the software accesses the PHY through ECAT MDIO to configure the register to set it as MII mode. This step is done because the default pin strapping configuration for this PHY is RGMII mode. The second configuration for the PHY is to configure the LED function. As the ECAT_LINK signal is connected to the LED pin of the PHY, you must configure the LED0 to indicate the link status of the PHY.

For deterministic EtherCAT operation, the final link mode must be confirmed as 100 Mbit/s full-duplex mode.

For the PHY configuration, refer to the code below:

```
/* Set the auto negotiation advertisement mode to 100M*/
ECAT_EscMdioWrite(ECAT, 0x01, 0x04, 0x1e1);
/* Disable the 1000Base-T capability to avoid negotiating to 1000M */
ECAT_EscMdioWrite(ECAT, 0x01, 0x09, 0x00);
/* Restart auto negotiation */
ECAT_EscMdioWrite(ECAT, 0x01, 0x00, 0x1240);
/* Set the LED0 feature as link status indication */
ECAT_EscMdioWrite(ECAT, 0x01, 0x1E, 0x401);
```

Then, initialize the EtherCAT controller with MII as the MAC interface mode. After the PHY link connection is established, the EtherCAT stack can start the SubDevice initialization process and enter the normal EtherCAT state transition flow, including INIT, PRE-OP, SAFE-OP, and OP states.

2.3 Test results

The EtherCAT application was verified by configuring the shared PHY in MII 100 Mbit/s mode and connecting the board to an EtherCAT MainDevice. After initialization, the PHY link was successfully established at 100 Mbit/s, and the EtherCAT detected the SubDevice.

The SubDevice completed the standard EtherCAT state transition and entered OP state successfully. Process data communication was verified between the EtherCAT MainDevice and the i.MX RT1180 EtherCAT SubDevice. Results confirm that the shared PHY solution can support EtherCAT communication in MII 100 Mbit/s mode.

Table 1 shows a typical EtherCAT solution validation result.

Table 1. EtherCAT application validation result

Test item	Expected result	Test result
PHY interface mode	MII	Pass
Link speed and mode	100 Mbit/s full-duplex	Pass
EtherCAT SubDevice detection	SubDevice detected by MainDevice	Pass
EtherCAT state transition	INIT to OP	Pass
Process data exchange	Cyclic data communication normal	Pass

3 NETC application

In the NETC application, the Ethernet PHY is configured to operate in RGMII mode with a link speed of 1000 Mbit/s. In this mode, the PHY is connected to the RT1180 NETC Ethernet controller and provides high-bandwidth Ethernet communication for general network applications and other industrial networking protocols such as ProfNet, TSN, and others.

This section describes the hardware connection, pin multiplexing, clock configuration, software initialization flow, and basic validation result for running Gigabit Ethernet over the shared PHY solution.

3.1 Hardware configuration

For NETC operation, the external PHY is configured as a Gigabit Ethernet PHY using the RGMII interface. The RGMII transmit and receive data signals, control signals, clock signals, MDIO/MDC management interface, reset signal, and interrupt signal are connected between the RT1180 NETC MAC and the shared PHY.

The IOMUX configuration must select the NETC function for the corresponding pins. Since the pins are multiplexed between EtherCAT and NETC functions, the EtherCAT pin function must be disabled when the system operates in NETC mode.

The clock configuration for RGMII is different, because the TX_CLK signal in RGMII mode is output from the MAC side. As shown in the Figure 2, the ENET_eCAT_SEL must be pulled low to let the MAC TX_CLK connect to the GTX_CLK of the PHY.

The RGMII interface also has a timing delay adjustment requirement. Configure the PHY and MAC consistently for RGMII internal delay or external PCB delay. The PHY must be configured to advertise and establish a 1000 Mbit/s full-duplex link.

Because every PHY has a default pin strapping configuration, which can make the PHY work in a specific mode after reset. Figure 4 shows the default pin strapping for the MIMXRT1180-EVK design.

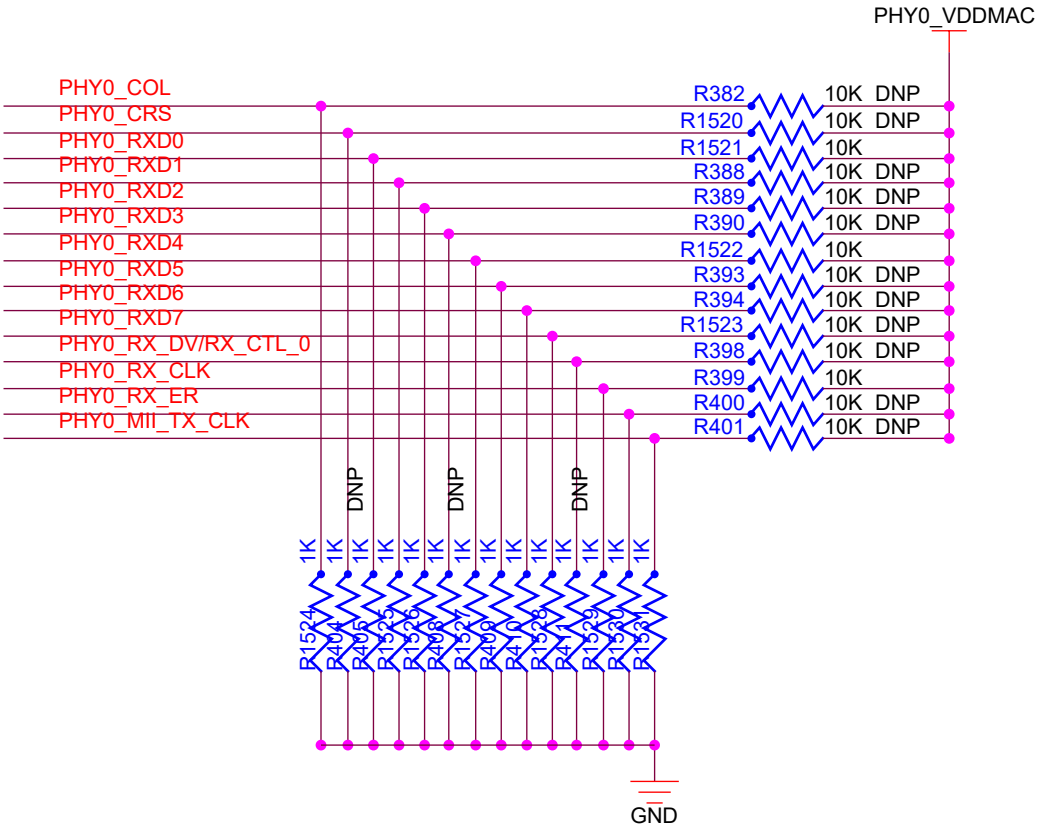

Figure 4. Pin strapping configuration

This setting configures the PHY work as RGMII 1000M full-duplex mode and adds 2 ns delay to both TX_CLK and RX_CLK.

3.2 Software configuration

During NETC initialization, the software first configures the IOMUX pins for the NETC RGMII interface and enables the required NETC and Ethernet clock sources. The clock for NETC MACs should be set to output 125 MHz to follow the requirement of RGMII. The PHY reset sequence is then performed before PHY register configuration.

After reset, the software initializes the MDIO interface and configures the PHY to auto-negotiation mode due to the pin strapping already set the PHY work as 1000M RGMII FDX. After auto-negotiation is complete, the software checks the link status and confirms that the link is established at 1000 Mbit/s.

The NETC driver is then initialized with RGMII as the MAC interface mode. Network parameters, such as MAC address, IP address, gateway, and subnet mask, are configured according to the target application. After the network interface is up, standard Ethernet communication can be verified by ping, TCP/UDP traffic, or throughput testing.

3.3 Test results

The NETC application was verified by configuring the shared PHY in RGMII 1000 Mbit/s mode and connecting the board to a Gigabit Ethernet link partner. After initialization and auto-negotiation, the PHY link was successfully established at 1000 Mbit/s full-duplex operation.

Basic network communication was verified by the NETC transfer test. The result confirms that the shared PHY solution supports NETC Gigabit Ethernet communication in RGMII 1000 Mbit/s mode.

Table 2 shows a typical NETC application validation result.

Table 2. NETC solution validation result

Test item	Expected result	Test result
PHY interface mode	RGMII	Pass
Link speed and mode	1000 Mbit/s Full-Duplex	Pass
Tx Rx transfer test	Successful response	Pass

4 Conclusion

4.1 Overall comparison of the solutions

Table 3 provides a comparison of the two solutions, conventional and the proposed.

Table 3. Feature comparison of the solutions

Parameter	Dual PHY solution	Single PHY solution (Proposed)
Number of PHYs	2	1
Supported protocols	EtherCAT + NETC	EtherCAT + NETC
Hardware complexity	High	Reduced
BOM cost	High	Lower
PCB routing	Complex	Simplified
Mode switching	Hardware selection	Software-controlled
System flexibility	Limited	High

As seen in the preceding table, the proposed single PHY architecture enables efficient hardware resource reuse and significantly reduces system cost while improving flexibility.

4.2 EtherCAT versus NETC configuration comparison

Table 4 shows the feature comparison of EtherCAT and NETC.

Table 4. Comparison of EtherCAT versus NETC configuration parameters

Parameter / Feature	EtherCAT mode	NETC mode
Interface	MII	RGMII
Link speed	100 Mbit/s	1000 Mbit/s
Duplex	Full-duplex	Full-duplex
MAC controller	EtherCAT controller	NETC controller
Pin multiplexing	EtherCAT pins enabled	NETC pins enabled
TX_CLK direction	PHY → MAC	MAC → PHY
Reference clock	25 MHz	125 MHz
PHY configuration	Forced 100M	Auto-negotiation
Typical use case	Real-time industrial control	High-bandwidth networking

4.3 Hardware design differences

Table 5 lists the hardware design differences EtherCAT and NETC.

Table 5. EtherCAT and NETC hardware design differences

Parameter	EtherCAT mode	NETC mode
PHY interface	MII	RGMII
TX_CLK source	PHY output	MAC output
Clock frequency	25 MHz	125 MHz

Table 5. EtherCAT and NETC hardware design differences*...continued*

Parameter	EtherCAT mode	NETC mode
Clock selection	Switch required	Switch required
Pinmux switching	Required	Required
RGMII delay	Not applicable	Required (internal or PCB)
Reference clock source	Preferable to use the MCU clock source	MCU or Crystal

.

4.4 Software initialization flow comparison

Table 6 shows the comparison of software initialization flow for EtherCAT and NETC.

Table 6. Software initialization flow comparison for EtherCAT and NETC

Step	EtherCAT mode	NETC mode
IOMUX configuration	Configure MII pins	Configure RGMII pins
Clock initialization	25 MHz	125 MHz
PHY reset	Required	Required
PHY configuration	Force 100 Mbit/s	Auto-negotiation
MAC initialization	EtherCAT controller	NETC MAC
Upper-layer stack	EtherCAT protocol stack	TCP/IP, TSN stack

4.5 Mode switching impact

Table 7 provides a comparison of the mode switching impact of EtherCAT and NETC.

Table 7. Mode switching impact of EtherCAT and NETC

Aspect	Impact
Pinmux switching	Must be consistent to avoid communication failure
Clock path selection	Must match the selected mode
TX_CLK direction	Critical difference between modes
PHY configuration	Must override default strap settings if needed
Software sequence	Reset → PHY config → MAC initialization

5 Acronyms

Table 8 describes the acronyms and abbreviations listed in this document.

Table 8. Acronyms and abbreviations

Acronym	Description
BOM	Bill of Materials
ECAT	EtherCAT
EtherCAT	Ethernet for Control Automation Technology
EVK	Evaluation Kit
FAE	Field Applications Engineer
FDX	Full Duplex
GPIO	General-Purpose Input/Output
IOMUX	Input/Output Multiplexer
IP	Internet Protocol
MAC	Media Access Control
MCU	Microcontroller Unit
MDC	Management Data Clock
MDIO	Management Data Input/Output
MII	Media Independent Interface
NDA	Non-Disclosure Agreement
NETC	Network Enabler and Traffic Controller
PCB	Printed Circuit Board
PHY	Physical Layer Device
PSIRT	Product Security Incident Response Team
RGMII	Reduced Gigabit Media Independent Interface
TCP	Transmission Control Protocol
TSN	Time-Sensitive Networking
UDP	User Datagram Protocol

6 Related documentation

Table 9 lists and explains the additional documents and resources that can be referred to for more information.

For the i.MX RT1180 product details, refer to the i.MX RT1180 web page. More documentation is available at the URL: i.MX RT1180 documentation.

Table 9. Related documentation

Document title	Description	Link/how to access
i.MX RT1180 reference manual	Provides a detailed description about the i.MX RT1180 MCU and its features, including memory maps, power supplies, and clocks.	IMXRT1180RM
i.MX RT1180 crossover processors data sheet	Provides information about electrical characteristics, hardware design considerations, and ordering information	IMXRT1180EC

7 Appendix

Figure 5 and Figure 6 describe the configurations that can be used to implement the design described in this document.

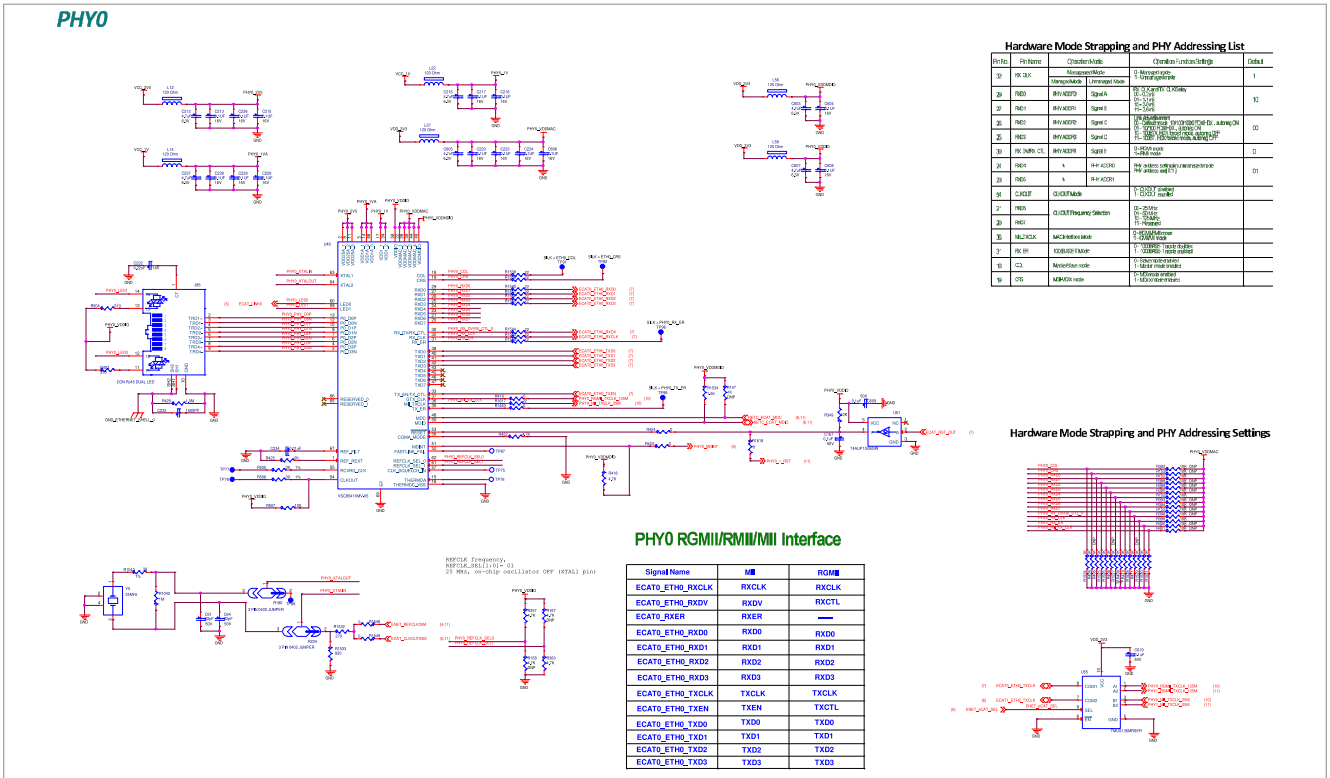

Figure 5. PHY0 configuration

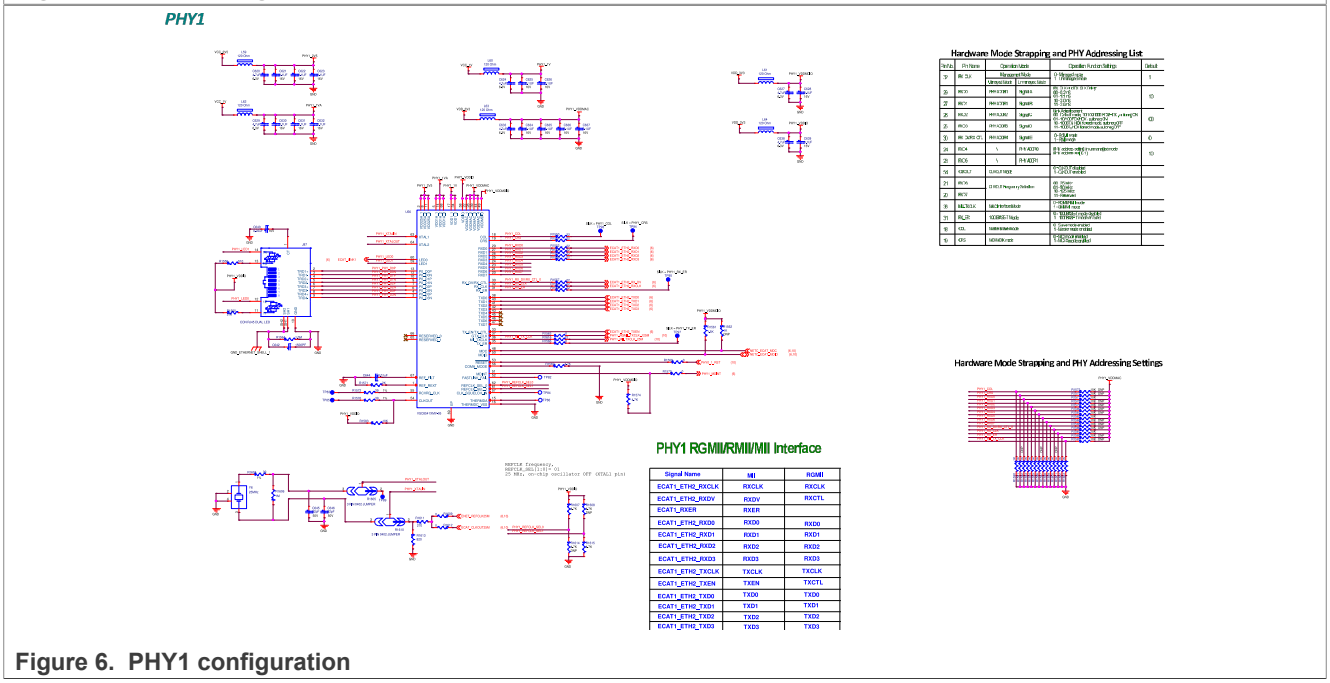

Figure 6. PHY1 configuration

8 Revision history

Table 10 summarizes revisions to this document.

Table 10. Revision history

Document ID	Release date	Description
AN15076 v.1.0	15 July 2026	Initial public release

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