AN15066

Direct Current Arc Fault Circuit Interrupters Solution with Time Series Studio

Rev. 1.0 — 23 June 2026 Application note

Document information

Information	Content
Keywords	AN15066, AFCI, MCX N54
Abstract	This document presents a DC AFCI reference solution based on MCX N547 MCU.

1 Introduction

Arc fault conditions caused by degraded wiring, loose connections, or insulation damage can generate high-energy and unpredictable electrical discharges, representing a significant fire hazard in low-voltage electrical systems. Due to their intermittent and non-linear characteristics, such faults are often not detected by conventional overcurrent or residual current protection devices. As a result, Arc Fault Circuit Interrupters (AFCI) have become an increasingly important safety feature in residential and commercial applications and are addressed by multiple international safety standards.

Once a Direct Current (DC) arc fault occurs, the line current exhibits broadband high-frequency components typically ranging from several kHz up to hundreds of kHz. These high-frequency signatures are characteristic of arc behavior and can be captured by appropriate sensing methods. By using a Current Transformer (CT), the variations in current are converted into proportional voltage signals, which can then be accurately sampled using the high-resolution on-chip ADC of the MCU for subsequent signal processing and arc fault detection.

NXP's AFCI solution is implemented on the MCX N547 microcontroller, using its integrated Neural Processing Unit (NPU) and PowerQuad Digital Signal Processing (DSP) accelerator to accelerate signal analysis and inference tasks. This hardware-assisted approach enables efficient processing of arc-fault-related features under real-time constraints while maintaining low CPU load and deterministic system behavior.

In addition to the hardware platform, NXP provides a comprehensive AFCI software and algorithm package designed to adapt to different equipment types and operating environments. The solution supports flexible parameterization and algorithm tuning to balance sensitivity and false-trip immunity across a wide range of loads. To further shorten development cycles, NXP also offers an AFCI evaluation and development board, allowing customers to rapidly develop, validate, and optimize their designs.

This application note presents a DC AFCI reference solution based on the MCX N547 MCU. It describes the system architecture, hardware design considerations, and software and algorithm concepts to assist system designers in implementing reliable and standards-compliant arc fault detection solutions.

2 DC AFCI solution overview and features

The NXP DC AFCI solution is based on the MCX N547 microcontroller and provides a high-performance, scalable platform for arc fault detection in DC systems. The solution integrates advanced signal processing and AI-based inference to achieve accurate and real-time arc fault detection.

- Hardware platform:
  - The single-chip solution based on the high-performance, cost-optimized MCX N547 multi-core MCU, integrating both a Neural Processing Unit (NPU) and PowerQuad DSP accelerator
  - Dual-core architecture
    - One core dedicated to real-time AFCI signal processing and detection
    - One core available for application-specific tasks (for example, Wi-Fi communication, OTA updates)
  - Built-in PowerQuad DSP can accelerate matrix, triangle functions, and transformations.
  - Built-in NPU can accelerate neural network computation ~30x depending on different work loads.
- Signal acquisition
  - Supports up to 8 AFCI sensing channels
  - Configurable sampling rate with ≥ 250 kSPS per channel
  - Integrated high-resolution 16-bit ADC enabling precise signal acquisition
- Signal processing and detection
  - Real-time signal preprocessing accelerated by PowerQuad DSP
  - AI-based arc fault detection using on-chip NPU acceleration

  - Typical detection latency within 10 ms, depending on system configuration
- Software and algorithm support
  - AI model development supported by NXP eIQ Time Series Studio (TSS)
    - Enables data collection, labeling, model training, and deployment
    - Supports deployment on both NPU and Arm Cortex-M cores
  - Supports simultaneous data sampling and real-time inference
  - Modular firmware architecture for easy customization
- System features
  - Built-in self-test functionality for detecting hardware and firmware faults
  - Supports High-Voltage (HV) test mode for data acquisition and dataset labeling
  - Interfaces available for system integration (for example, USB, CAN, RS-485, Wi-Fi)
- Power and electrical specifications
  - Input supply voltage: 12/24 V DC
  - Power consumption: application-dependent
  - Current sensor: Magnet DIA 35.8 mm

3 System architecture

The NXP DC AFCI solution includes both the hardware development platform (MCXN547-AFCI board kit) and the PC side NXP eIQ TSS software. Figure 1 shows AFCI solution system architecture.

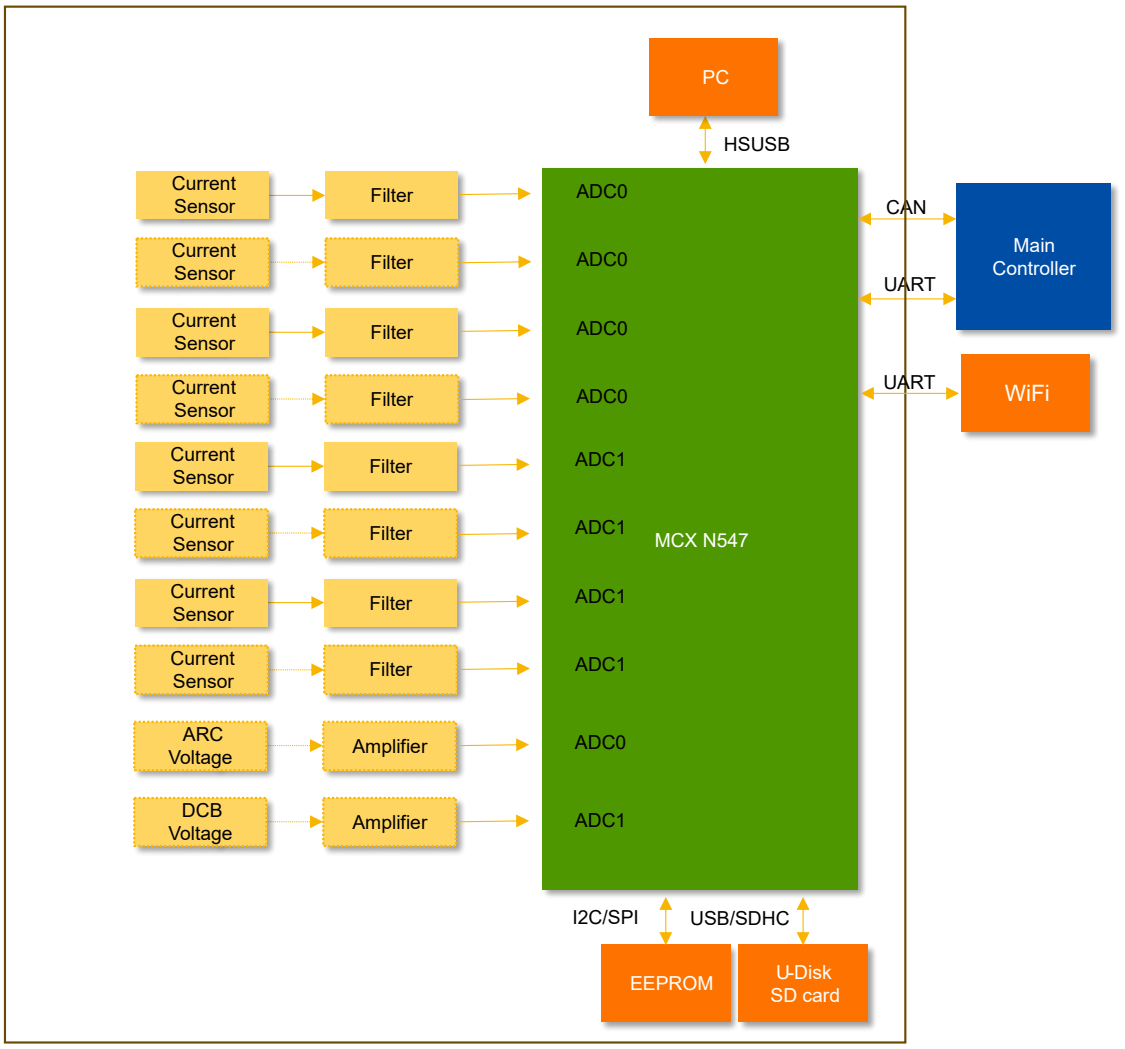

Figure 1. DC AFCI solution system architecture

The NXP DC AFCI solution software is designed as a layered and multi-core architecture, enabling efficient separation of real-time signal processing, inference, system control, and communication functions. The architecture runs on the MCX N547 MCU and uses its dual-core capability to improve system robustness and scalability. Figure 2 shows the DC AFCI solution software architecture.

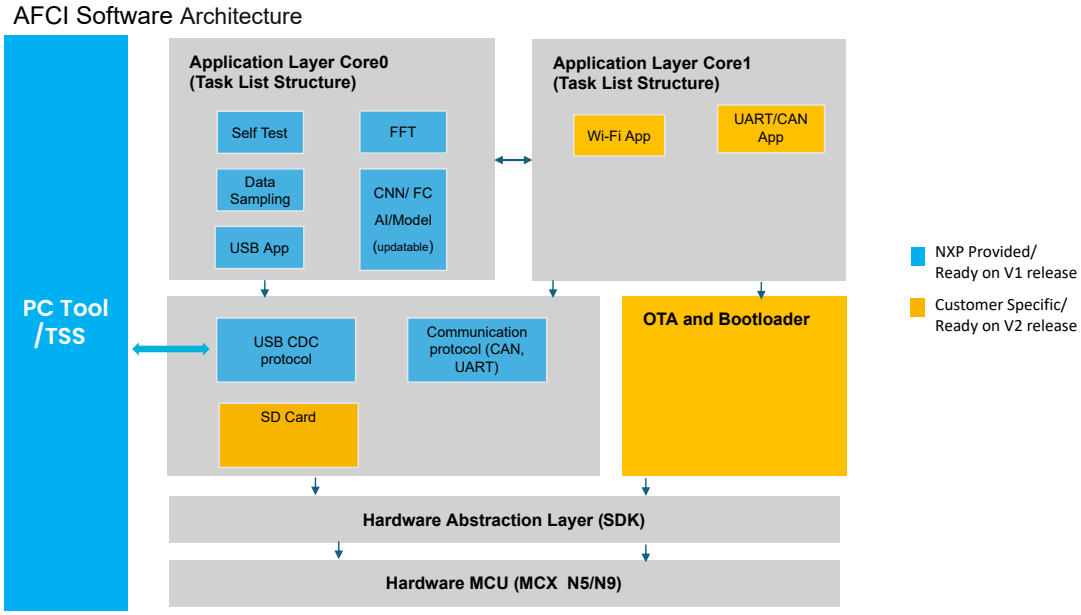

Figure 2. DC AFCI solution software architecture

The AFCI signal processing pipeline follows a deterministic streaming architecture:

- Sampling stage: High-speed ADC sampling (typically from 100 to 500 ksps depending on application) captures current waveform data.
- Feature extraction: Fast Fourier Transform (FFT) and time-domain statistical features are computed using PowerQuad accelerators.
- Inference stage: Extracted features are fed into a trained ML model (for example, CNN or TCN) running on the NPU.
- Decision logic: User can write their own code to implement the control behavior (for example, power off the load on the line, save fault data for analysis)

3.1 Application layer

At the application layer, AFCI functions are organized into independent tasks executed on different cores.

Core 0 is dedicated to real-time and safety-critical AFCI processing. It implements a task-list-based structure that includes signal acquisition, signal processing, inference, and system self-test functions. Typical tasks running on Core 0 include:

- Data sampling: Continuous acquisition of current signals from the analog front end.
- FFT processing: Frequency-domain analysis used for feature extraction related to arc fault behavior.
- AI model inference: Execution of CNN or Fully Connected (FC) models for arc fault classification. The AI model is updatable to support algorithm evolution and application-specific tuning.
- Self-test: Configurable periodic self-diagnostics to verify the integrity of signal paths, processing functions, and system health.
- USB application: A local interface for debugging.

Core 1 is dedicated to communication and non-critical application tasks. By isolating these functions from the real-time AFCI processing, the overall system determinism is improved. Core 1 typically runs:

- Wi-Fi application: Wireless communication for monitoring, configuration, or cloud connectivity.
- UART/CAN application: Wired communication interfaces for integration with external controllers or systems.

Inter-core communication mechanisms are used to exchange status information and control messages between Core 0 and Core 1 without impacting real-time performance.

3.2 Communication and storage

The software provides multiple communication protocol interfaces, including USB CDC, UART, and CAN. These interfaces enable interaction with external tools such as PC-based tuning and test software.

An SD card interface is supported for extended data logging, firmware updates, facilitating offline analysis and system validation.

3.3 OTA and Bootloader

The software architecture integrates an OTA update mechanism and a secure bootloader. The OTA function allows firmware and AI model updates to be deployed in the field while maintaining system integrity. OTA functionality operates independently from the core AFCI detection tasks to avoid interference with real-time operation. The secure bootloader allows an image to be booted from a specific area in a secure way, which depends on customer-specific requirements and is not implemented in this solution.

3.4 Hardware abstraction layer

Below the application layer, the Hardware Abstraction Layer (HAL), provided as part of the NXP MCUXpresso SDK, isolates application software from the underlying hardware. This layer simplifies portability and maintenance across MCX devices, which gives customer chances to choose better performance MCUs.

The complete software executes on the MCX N-series MCU platform (MCX N547), forming a scalable and maintainable AFCI software solution suitable for production deployment.

4 Hardware design

The NXP DC AFCI reference hardware (MCXN547-AFCI board) is a reference board designed to support multi-channel arc fault signal acquisition, high-resolution analog signal conditioning, and safe operation under high-voltage environments. The hardware platform is centered on the MCX N547 MCU and integrates dedicated analog front-end circuits design, flexible communication interfaces, and a robust power management subsystem.

The reference design is intended as a development and evaluation platform and can be adapted to different AFCI end applications, such as circuit breakers, outlets, and industrial protection devices.

4.1 Arc fault signal acquisition and analog front end

The reference hardware supports multiple arc fault sensing channels, organized into eight groups. Each channel is designed to interface with external current sensing.

The analog circuit design for each AFCI channel includes:

- Input protection and clamping circuits to improve robustness against transient events.
- High-pass and low-pass filtering stages to suppress low-frequency components and out-of-band noise.
- Amplification and level-shifting circuits that scale the arc fault signals to match the ADC input range of the MCU.

Filter components can be selectively populated or bypassed, allowing flexibility in frequency response tuning to accommodate different sensing methods and regulatory requirements.

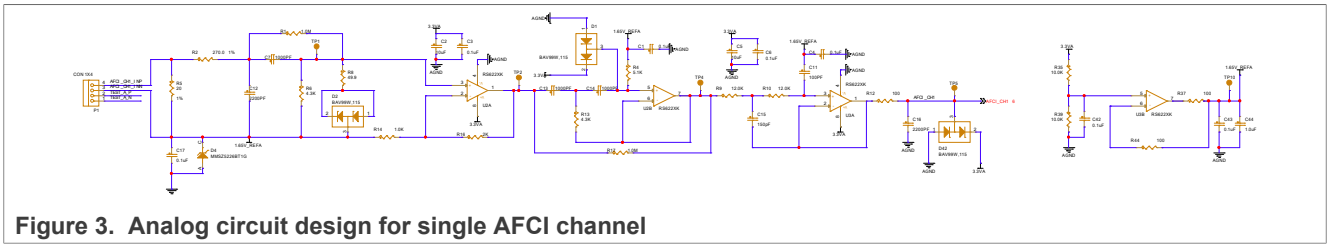

Figure 3. Analog circuit design for single AFCI channel

The circuit must be regarded as a reference design only. The final component values, gain distribution, protection level, filter bandwidth, and layout strategy must be designed and validated according to the actual application, sensor type, and other environment to achieve the best performance. For DC AFCI solution, the bandwidth of the analog front end is a critical design parameter. Arc fault signatures typically contain frequency components ranging from several kHz up to hundreds of kHz. Therefore, the analog front-end design must consider bandwidth and signal-to-noise optimization.

4.2 Voltage sensing and isolation

To support arc voltage and DC bus voltage monitoring, the hardware integrates isolated voltage sensing circuits. Isolation amplifiers are used to safely interface high-voltage signals with the low-voltage digital domain, providing reinforced isolation and improved system safety. NXP TSS uses the voltage sensing function to help users label the data.

The voltage sensing circuits are designed to scale high input voltages to the 3.3 V ADC range of the MCU while maintaining adequate resolution for arc fault analysis. Separate reference voltages and analog grounds are implemented to improve measurement accuracy and reduce noise coupling.

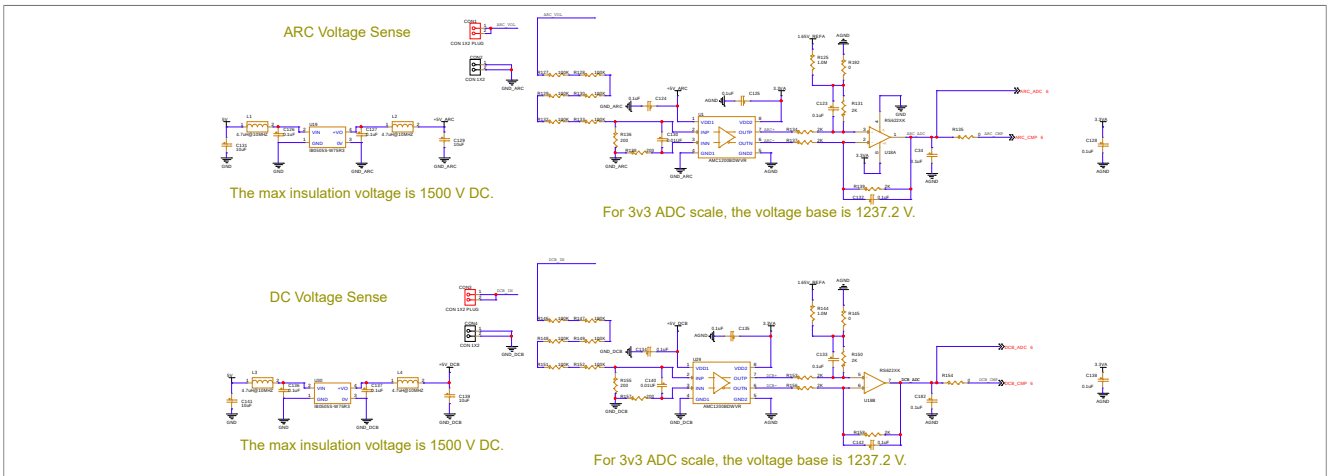

Figure 4. Voltage Sense circuit design

4.3 MCU and peripheral interfaces

The MCX N547 MCU serves as the central processing unit of the AFCI system, providing high-performance analog-to-digital converters, dual-core processing capability, and dedicated acceleration resources.

Multiple ADC channels are used to sample conditioned AFCI signals and voltage sensing outputs. Comparator inputs are optionally used for diagnostic functions.

The hardware platform also integrates a rich set of peripheral interfaces, including:

- USBs (Type-C) for debugging, configuration, and data streaming.
- CAN and RS-485 for industrial and system-level communication.

- UART and SD card interfaces for logging and firmware update support.

These interfaces enable seamless integration with external tools and system controllers.

4.4 Power supply design

The reference hardware supports a wide input voltage range suitable for development and evaluation environments. On-board DC-DC converters and low-dropout regulators generate the required voltage rails for the MCU core, digital logic, and analog circuitry.

Separate analog and digital power domains are implemented to minimize noise coupling into sensitive signal acquisition paths. Proper decoupling and filtering are applied at each supply node to ensure stable operation under dynamic load conditions.

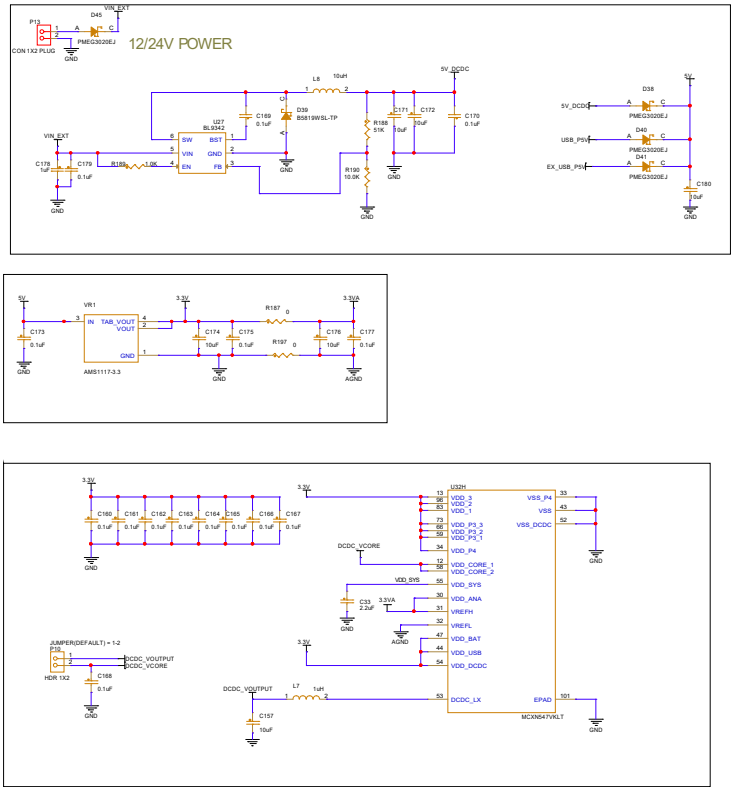

Figure 5. Power supply design

4.5 Development and test support

To facilitate development and validation, the reference design includes test points for key analog signals, voltage rails, and communication interfaces. Configuration jumpers and mode selection switches are provided to support different operating modes and debugging scenarios.

These features allow engineers to efficiently evaluate signal quality, tune algorithm parameters, and validate system behavior during development and compliance testing.

5 Algorithm and software development support

NXP's AFCI solution uses the eIQ TSS platform to support full algorithm life-cycle development – from data collection to model deployment – enabling efficient adaptation and optimization of arc-fault detection algorithms.

5.1 Data collection and labeling

Using the TSS AFCI workflow, users can import raw current waveform datasets directly from the MCXN547-AFCI development board via the built-in Data Logging feature. This process facilitates streamlined collection of representative data under real-world load and arc-fault scenarios.

Once data is imported (such as CSV or float32 WAV format), the data labeling tool allows engineers to tag sections as "arc" or "no arc" within a visual interface. The labeled segments are automatically partitioned into training datasets suited for both time-domain and frequency-domain modeling.

In DC AFCI solution, dataset diversity is a key factor affecting model performance. Training datasets must include:

- Different load types
- Various arc fault conditions
- (Most Important) Normal operating disturbances (such as switching noise, motor startup, load transients)

This ensures that the trained model can effectively distinguish arc faults from normal electrical disturbances.

5.2 Model training and evaluation

TSS supports the creation of AFCI-specific machine learning models. Users can configure project parameters such as:

- Target board (select MCXN547-AFCI for board-specific optimization)
- Number of classes
- Sampling rate
- Library RAM and flash constraints
- Sensor type and channel configuration

The platform automatically generates training datasets and trains models – typically using classical ML or lightweight neural networks – to balance accuracy and resource usage.

5.3 Emulation, benchmarking, and deployment

Prior to deployment, models can be emulated and benchmarked within TSS to evaluate performance and resource utilization (RAM, flash, CPU cycles). Once validated, the platform supports a cloud-based Deployment process that generates optimized libraries or binaries compatible with the MCX N547, including support for hardware acceleration such as PowerQuad DSP accelerator and NPU.

The output includes:

- Optimized library (*.a/.lib*) or binary (*.bin*) versions
- Sample MCUXpresso project templates for seamless integration
- Support for multiple compilers (GCC, Keil, IAR) and architecture

5.4 Integration into MCX N547

The generated AFCI algorithm library is integrated into the MCX N547 software stack, typically in Core 0 where real-time signal processing and inference are executed. The use of hardware accelerators enables efficient

execution of FFT transforms and inference workloads with minimal CPU load, improving system determinism and responsiveness.

TSS also supports Multi-Library generation, enabling deployment of multiple independent models (such as separate models for solar panel arc and other for high-voltage transformer arc) within the same MCU environment.

5.5 Decision and protection strategy

The AFCI system does not rely solely on instantaneous detection results. Instead, a multi-level decision mechanism is used:

- Frame-level inference results are accumulated over time.
- A configurable threshold (such as N detections within M frames) is applied.
- Additional validation logic may include current magnitude and duration checks.

Once an arc fault is confirmed, the system triggers a protection action such as:

- Relay or breaker trip signal
- Fault reporting via communication interface

This approach significantly reduces nuisance trippings while maintaining safety compliance.

5.6 AFCI firmware reference

To further accelerate customer development and evaluation, NXP provides a full open-source AFCI firmware reference implementation based on the MCX N547 MCU. The firmware is available on TSS and serves as a complete starting point for AFCI system development.

The AFCI firmware includes:

- Multi-channel arc fault signal acquisition and preprocessing
- Integration of TSS-generated AFCI algorithm libraries
- Real-time inference execution optimized for the MCX N547 architecture
- Support for hardware acceleration, including DSP math accelerators and the on-chip NPU
- Communication, data logging, and debugging interfaces consistent with reference hardware

The firmware is structured in a modular manner, allowing customers to easily customize signal processing pipelines, algorithm parameters, and application logic to meet specific product and regulatory requirements.

6 Compliance and certification

The final user DC AFCI product must comply with the related regional safety standards depending on the application domain. Typical standards include:

- UL 1699 – Standard for Arc-Fault Circuit-Interrupters
- IEC 62606 – General requirements for arc fault detection devices
- GB/T standards – Applicable for low-voltage electrical systems

Compliance requires verification under defined arc fault conditions, including:

- Series arc and parallel arc scenarios
- Different load types and current levels
- Immunity tests against normal operating conditions

The NXP DC AFCI solution, including both hardware development platform and easy-to-use software tool, supports online rapid dataset collection and algorithm tuning. It not only greatly helps users shorten the AFCI product development cycle time, but also helps their products easily meet the related certification requirements.

7 Acronyms and abbreviations

Table 1 lists and explains the acronyms and abbreviations used in this document.

Table 1. Acronyms and abbreviations

Acronyms	Description
ADC	Analog-to-Digital Converter
AFCI	Arc Fault Circuit Interrupters
CAN	Controller Area Network
CDC	Communications Device Class
CNN	Convolutional Neural Network
CSV	Comma Separated Variables
CT	Current Transformer
DC	Direct Current
DSP	Digital Signal Processing
FFT	Fast Fourier Transform
GCC	GNU Compiler Collection
HAL	Hardware Abstraction Layer
HV	High Voltage
NPU	Neural Processing Unit
OTA	Over-The-Air
RAM	Random Access Memory
TCN	Temporal Convolutional Network
TSS	Time Series Studio
UART	Universal Asynchronous Receive Transmit
USB	Universal Serial Bus

8 Revision history

Table 2 summarizes the revisions to this document.

Table 2. Revision history

Document ID	Release date	Description
AN15066 v.1.0	23 June 2026	Initial public release.

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