

AN15064

i.MX RT ROMs Log Events

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Application note

Document information

Information	Content
Keywords	AN15064, i.MX RT microcontrollers, ROM log, ROM events, ROM code, ROM boot, log buffer, boot attempt, boot process, debugging
Abstract	This document describes the details of ROM log events for i.MX RT series ROM.



1 Introduction

ROM events are defined for ROM debug purpose. When the ROM code executes to a significant node, a specific ROM event is recorded in the ROM event log buffer. Events are captured in the ROM log buffer for every boot attempt, success, or fail. This provides the developer with a snapshot of the ROM boot process for analysis.

This document describes the details of ROM log events for i.MX RT series ROM.

1.1 Glossary

[Table 1](#) lists the terms and acronyms required to interpret this document.

Table 1. Glossary

Term	Definition
ROM event	Identifies a specific point in ROM boot processing, to show the ROM boot-related information. For example: • which boot mode ROM is retrieved from fuses or GPIOs; • which boot device is used for this boot try; • is boot device initialization complete; • is loading data from the boot device complete; • does boot image authentication pass, and so on.
ROM event log buffer	A section or several sections (for some devices) in RAM where ROM events are logged.

2 ROM events

Each ROM event is stored in the ROM event log buffer. The buffer contains several event entries, and the type of event can be distinguished using the ROM event ID inside each ROM event entry.

2.1 ROM event entry

The ROM event entries are saved in the ROM event log buffer. For i.MX RT10xx series, the log buffer is simple as below. Unused `rom_event_ID` buffer is set to all 0x00s.

```
uint32_t rom_event_ID[64];
```

For i.MX RT3digits and i.MX RT11xx series, it uses a new log context structure as below:

```
typedef struct _log_context
{
    uint32_t entryNum;
    uint32_t logEntries[64];
} log_context_t;
```

One single ROM event entry consists of the ROM event ID and its parameters.

Table 2. A ROM event entry

Offset	Bits [31:0]
0x00	ROM event ID
0x01	Parameter0 (Optional, available for some events)

Table 2. A ROM event entry...continued

Offset	Bits [31:0]
0x02	Parameter1 (Optional, available for some events)
0x03	Parameter2 (Optional, available for some events)

For i.MX RT700, it doesn't support ROM event log, but it stores boot state information into `SYSCON0->ELS_BOOT_STATE0`, `SYSCON0->ELS_BOOT_STATE1`, `SYSCON0->ELS_BOOT_STATE2` registers. As boot state is different from event log, so i.MX RT700 ROM project is not included in this document.

2.2 ROM event ID format

There are two versions of ROM event ID formats:

Table 3. ROM event format version

ROM event ID format versions	User
ROM event ID format version 0	i.MX RT10xx series
ROM event ID format version 1	i.MX RT3digits, i.MX RT11xx series

2.2.1 ROM event ID format version 0

Table 4. ROM event format version 0

Bits 31-24	Bits 23-0
Reserved as 0x00	Log event ID

2.2.2 ROM event ID format version 1

Table 5. ROM event format version 1

Bits 31-24	Bits 23-16	Bits 15-8	Bits 7-0
Log State	Log Substate	Log Status	Remaining log parameters

2.3 ROM event ID definitions

Table 6. ROM event ID definition version

ROM event ID definition versions	ROM event ID format	User
ROM event ID definition version 0	ROM event ID format version 0	i.MX RT10xx series.
ROM event ID definition version 1	ROM event ID format version 1	i.MX RT3digits, i.MX RT11xx series

2.3.1 ROM event ID definition version 0

[Table 7](#) describes the ROM event IDs used in i.MX RT10xx series.

Table 7. ROM event ID definition version 0

Log event ID	Description
0x010000	Boot mode is Boot from Fuse
0x010001	Boot mode is Serial Download
0x010002	Boot mode is Internal Boot

Table 7. ROM event ID definition version 0...continued

Log event ID	Description
0x010003	Boot mode is Test Mode
0x020000	Secure config is FAB
0x020033	Secure config is Field Return
0x0200F0	Secure config is Open
0x0200CC	Secure config is Closed
0x030000	DIR_BT_DIS Fuse is not blown
0x030001	DIR_BT_DIS Fuse is blown
0x040000	BT_FUSE_SEL Fuse is not blown
0x040001	BT_FUSE_SEL Fuse is blown
0x050000	Boot from the primary boot image
0x050001	Boot from the secondary boot image
0x050002	Boot from the third boot image
0x050003	Boot from the fourth boot image
0x060001	Primary boot from SD or EMMC device
0x060008	Primary boot from FLEXSPI NOR device
0x060009	Primary boot from FLEXSPI NAND device
0x06000A	Primary boot from SEMC NOR device
0x06000B	Primary boot from SEMC NAND device
0x061005	Recovery boot from LPSPI NOR device
0x061FFF	No recovery boot device
0x062001	Manufacture boot from SD or EMMC
0x070000	Start to perform the device initialization
0x0700F0	The boot device initialization completes
0x070033	The boot device initialization fails
0x080000	Start to read data from boot device
0x0800F0	Reading data from boot device completes
0x080033	Reading data from boot device fails
0x090000	Image authentication result (Bit[7:0]==0xF0: pass)
0x0A0000	Start to execute the plugin program
0x0A00F0	The plugin program returns success
0x0A0033	The plugin program returns failure
0x0B0000	Jump to the boot image soon
0x0C0000	Enters serial download processing
0x0D0000	Jump to the SDP boot image soon
0x0E0000	Internal use for ROMCP PATCH

2.3.2 ROM event ID definition version 1

The ROM event IDs used in the i.MX RT3digits and i.MX RT11xx series are as follows.

Table 8. ROM event ID (log state) definition version 1

Log state	Description	Log parameter																								
0x00	Startup	—																								
0x01	Hardware Init	—																								
0x02	ROM Patch	—																								
0x03	Secure Boot	—																								
0x04	Boot Mode	—																								
0x05	Master Boot	Parameter0: boot type <table><tr><td>0x00000001</td><td>Primary Boot</td></tr><tr><td>0x00000002</td><td>Recovery Boot</td></tr><tr><td>0x00000003</td><td>Manufacture Boot</td></tr><tr><td>0x00000004</td><td>Serial Boot</td></tr></table>	0x00000001	Primary Boot	0x00000002	Recovery Boot	0x00000003	Manufacture Boot	0x00000004	Serial Boot																
0x00000001	Primary Boot																									
0x00000002	Recovery Boot																									
0x00000003	Manufacture Boot																									
0x00000004	Serial Boot																									
0x06	Passive Boot	—																								
0x07	Recovery Boot	—																								
0x08	Isp Boot	—																								
0x09	Boot Device	Parameter0: boot type (When substate is 0x01 – init) <table><tr><td>0x00000001</td><td>Primary Boot</td></tr><tr><td>0x00000002</td><td>Recovery Boot</td></tr><tr><td>0x00000003</td><td>Manufacture Boot</td></tr><tr><td>0x00000004</td><td>Serial Boot</td></tr></table> Parameter0: image index (When the substate is 0x02 – call) Parameter1: boot peripheral (When parameter0 is primary boot) <table><tr><td>0x00000000</td><td>QuadSPI</td></tr><tr><td>0x00000001</td><td>MMC</td></tr><tr><td>0x00000002</td><td>SD</td></tr><tr><td>0x00000003</td><td>SEMC NAND</td></tr><tr><td>0x00000004</td><td>SEMC NOR</td></tr><tr><td>0x00000005</td><td>FLEXSPI NOR</td></tr><tr><td>0x00000006</td><td>FLEXSPI NAND</td></tr></table> Parameter1: boot peripheral (When parameter0 is recovery boot) <table><tr><td>0x00000000</td><td>SPI NOR</td></tr></table> Parameter1: boot peripheral (When parameter0 is manufacture boot)	0x00000001	Primary Boot	0x00000002	Recovery Boot	0x00000003	Manufacture Boot	0x00000004	Serial Boot	0x00000000	QuadSPI	0x00000001	MMC	0x00000002	SD	0x00000003	SEMC NAND	0x00000004	SEMC NOR	0x00000005	FLEXSPI NOR	0x00000006	FLEXSPI NAND	0x00000000	SPI NOR
0x00000001	Primary Boot																									
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0x00000001	MMC																									
0x00000002	SD																									
0x00000003	SEMC NAND																									
0x00000004	SEMC NOR																									
0x00000005	FLEXSPI NOR																									
0x00000006	FLEXSPI NAND																									
0x00000000	SPI NOR																									

Table 8. ROM event ID (log state) definition version 1...continued

Log state	Description	Log parameter	
		0x00000000	SDMMC
		Parameter1: boot peripheral (When parameter0 is serial boot)	
		0x00000001	UART
		0x00000002	I2C Slave
		0x00000004	SPI Slave
		0x00000008	CAN
		0x00000010	USB HID
		0x00000020	USB CDC
		0x00000040	USB DFU
		0x00000080	USB MSC
		0x00000011	UART/USB HID
		0x00000100	QuadSPI
		0x00000200	MMC
		0x00000400	SD
		0x00000800	SEMC
		0x00001000	SpiFlash
		Parameter2: peripheral instance	
0x0a	Load Image	—	
0x0b	Auth Image	Parameter0: Cost time in us	
0x0c	Jump to Image	Parameter0: image entry address	
0x0d	TZ-M	—	
0xff	Fatal	—	

Table 9. ROM event ID (log substate) definition version 1

Log Substate	Description
0x00	Common
0x01	Init
0x02	Call
0x03	Deinit
0x04	Source
0x05	Check
0x20	Img - Initial Load
0x21	Img - Remaining Load
0x30	Auth - Check Secure State
0x31	Auth - Image Type Check

Table 9. ROM event ID (log substate) definition version 1...continued

Log Substate	Description
0x32	Auth - Read Key Store
0x33	Auth - Read Mac Key
0x34	Auth - Verify HMAC
0x35	Auth - Image Entry Check
0x36	Auth - Authenticate
0x37	Auth - Crc Check
0x38	Auth - DICE
0x39	Auth - Boot Seed
0x70	Boot Device
0x71	Load Image
0x72	Auth Image
0x73	Jump to Image

Table 10. ROM event ID (log status) definition version 1

Log Status	Description
0x01	Master Boot
0x02	Passive Boot
0x03	Recovery Boot
0x04	Isp Boot
0xdc	Disabled
0xea	Enabled
0xf0	Pass
0xf3	Fail
0xf5	Fatal
0xfc	Invalid
0xff	Default

3 ROM event log buffer

The ROM event log buffer is located at a fixed address in the on-chip RAM.

3.1 Base address of ROM event log buffer

The 32-bit base address of the ROM event log buffer is recorded in a fixed location that varies by device type. Users must reference the ROM event log buffer base address to locate the log buffer data.

Table 11. ROM event log buffer addresses

i.MX RT device	Log buffer base address
i.MX RT118x	0x3048a000

Table 11. ROM event log buffer addresses...continued

i.MX RT device	Log buffer base address
i.MX RT117x	0x2024ad78
i.MX RT116x	0x2024ad78
i.MX RT106x	0x2020523c
i.MX RT105x	0x202051c8
i.MX RT104x	0x2020523c
i.MX RT102x	0x2020515c
i.MX RT1015	0x2020515c
i.MX RT1011	0x20203d38
i.MX RT6xx	0x10017f00
i.MX RT5xx	0x10017ef8

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5 Revision history

Table 12 summarizes the revisions to this document.

Table 12. Revision history

Document ID	Release date	Description
AN15064 v.1.0	01 September 2026	Initial public release.

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