AN15028

NFC controller external watchdog

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Document information

Information	Content
Keywords	NFC controller, external watchdog, low power
Abstract	This document describes different approaches to achieve a power cycle with various external components and outlines the operative boundaries and specifications to follow.

1 Introduction

Field observations have shown that, in rare cases, an NFC controller may not exit the ULPCD mode when a card is presented. These cases have been associated with external electrical disturbances occurring during the wake-up sequence, such as supply-line noise, transient glitches, or ESD-related events.

To ensure consistent and resilient system behavior, NXP requires the implementation of an appropriate recovery mechanism that prevents the system from entering a nonrecoverable state. When ULPCD is used, it is recommended to include an alternative wake-up path based on a controlled chip power cycle. This approach ensures that the system can reliably recover from Powersaving mode, including in exceptional cases where external disturbances prevent ULPCD from triggering a wake-up.

This document describes different approaches to achieve a power cycle with various external components and outlines the operative boundaries and specifications to follow.

1.1 Supported devices

This document and the functionality explained within it applies to the following NXP ICs:

- PN76AC
- PN7642

Note: *For more information, refer to product pages on nxp.com (PN76AC ref.[1], PN7642 ref.[2]).*

2 Functionality

The objective is to have an external low power mechanism, to power cycle the connected NFC controller in case of unresponsiveness. The power cycle is achieved by toggling a load switch, which is temporarily removing power (VBAT/VBATPWR/VDDIO/...) from the NFC controller.

Requirements:

- VBAT must be below 200 mV for more than 5 milliseconds to guarantee a proper internal reset.
- Connected pins, like GPIO or Host-Interface (I2C/SPI/UART), must be put low to avoid cross-supply of VBAT.
- VBAT, VDDIO, VDDC, and other supplies must be controlled according to the data sheet.

Depending on the system architecture, there are various possibilities to control the load switch. The following chapters cover some possible scenarios.

If the planned architecture can control the NFC supply domains and is capable to achieve the objective, an additional load switch is not necessary.

3 Host-controlled external watchdog

If a host controller is available, it can have the role of the observer if the NFC controller is responsive. The host controller periodically wakes up and checks the system liveness.

How to check if the NFC controller is responsive can be done via the host-interface. In case the NFC controller is not responsive, the host controller toggles the load switch to ultimately reset the NFC controller.

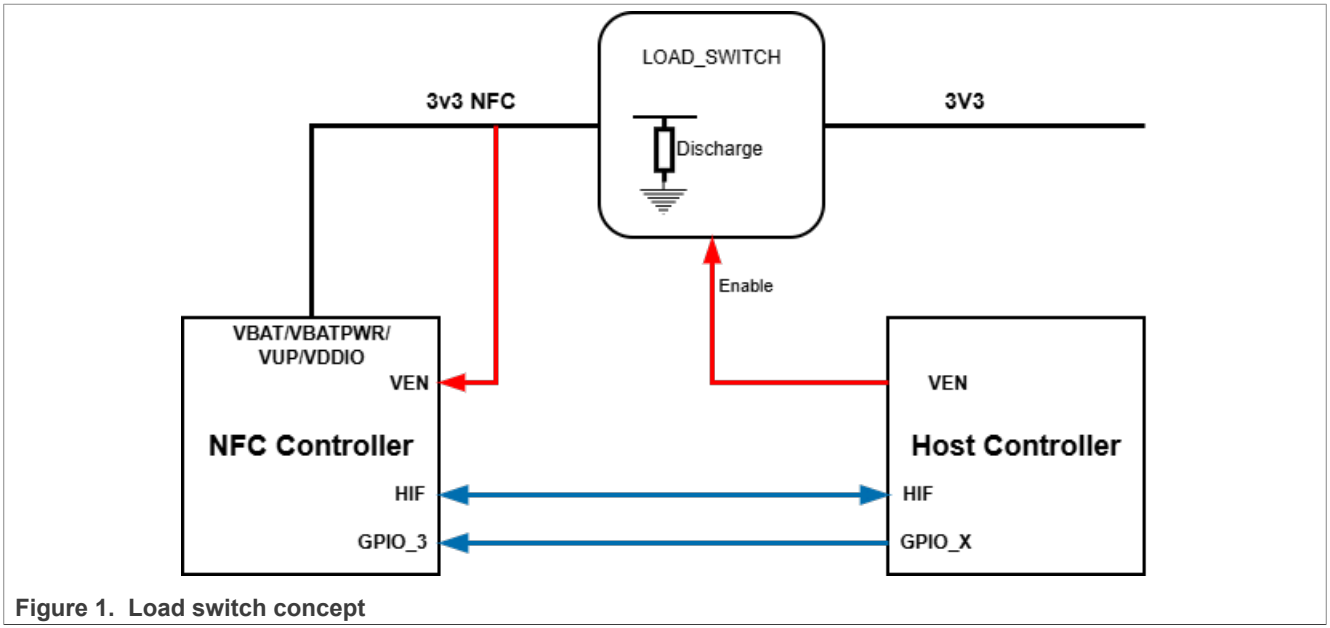

Figure 1. Load switch concept

3.1 Liveness check via HIF

The NFC controller is supposed to be in ULPCD, before any host interface command can be sent the host controller has to wake up the NFC controller via GPIO_3.

Note: *While being in ULPCD only GPIO_3/WKUP_PIN will properly wake up the NFC controller. Host interface activity is not monitored while in ultra low power modes.*

After the NFC controller is woken up, the host issues a host command and expects a response. If no response is observed, the NFC controller is assumed to be in an unresponsive state and the host controller must act, like toggling the load switch.

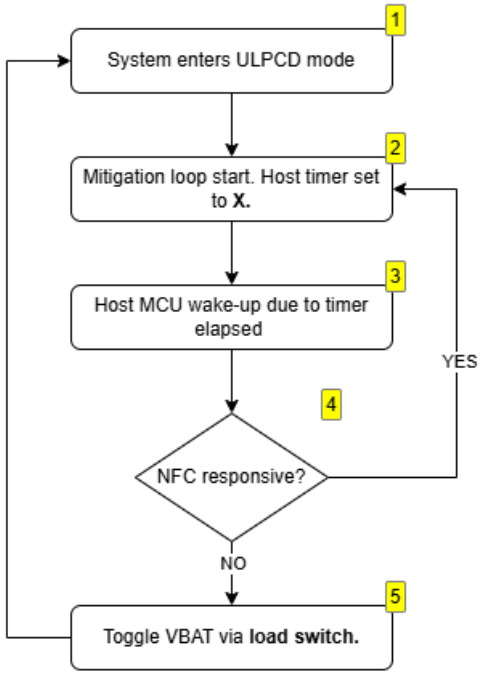

Figure 2. Control loop flowchart

[1] System enters ULPCD mode.

The host controller sets the NFC controller into ULPCD.

[2] Mitigation loop start

The host controller starts a timer. The timeout value (for example, 10 minutes) can freely be chosen and depends on power budget and application. Worst case the NFC controller is unresponsive for this amount of time.

This timer can be a low-power timer or any other system available timer. The host continues with normal operations, which can be going to sleep, and assumes that the NFC controller is operating as expected.

[3] Host MCU wake-up

Host awakes due to timer elapse.

[4] NFC responsiveness check

The host toggles GPIO_3/WKUP_PIN (see Section "*Technology Detection Activity when the ULPCD has detected an "object"*" in UM12399) to wake up the NFC controller from ULPCD. After that, the NFC controller is assumed to be awake, and a command is issued to check responsiveness.

PN76AC: After waking up the PN76AC, the controller is in RFST_DISCOVERY. A CORE_GET_CONFIG command can be issued and a STATUS_SEMANTIC_ERROR response is expected.

If a response is received, the NFC controller is alive and no mitigation action must be taken. The host controller pulls GPIO_3/WKUP_PIN low and sets the NFC controller back to ULPCD mode. The mitigation loop starts again → [2].

If no response is received, the NFC controller is assumed to be unresponsive → [5].

[5] Load switch toggle

The host controller toggles the load switch to reset the NFC controller. The NFC controller is operational again the host controller configures and sets the NFC controller to ULPCD again → [1].

3.2 Toggle load switch

In case the NFC controller proves that unresponsive the load switch shall be toggled. The host, or external controlling entity, is responsible to do so.

In the NXP NCI Library provided for PN76AC a method for VEN toggle is already provided as part of the standard library:

```
/**
* This function will toggle ven pin
*/
void phApp_Ven_Toggle(void)
{
    phDriver_Pin_Config_t pinVenCfg = {
        .bPullSelect = PH_DRIVER_PULL_UP,
  .bOutputLogic = PH_DRIVER_SET_LOW
    };

    /* toggle VEN PIN */
    phDriver_PinConfig(PH_DRIVER_PIN_VEN, PH_DRIVER_PINFUNC_OUTPUT, &pinVenCfg);
    phDriver_TimerStart(PH_DRIVER_TIMER_MILLI_SECS, 20U, NULL);

    phDriver_PinWrite(PH_DRIVER_PIN_VEN, PH_DRIVER_SET_HIGH);
    phDriver_TimerStart(PH_DRIVER_TIMER_MILLI_SECS, TVEN_BOOT_POR, NULL);
}
```

If the host-interface is SPI the chip-select (SSP) must be brought low as well, before VEN is raising again. The VEN method can be extended for this purpose:

```
/**
* This function will toggle ven pin
*/
void phApp_Ven_Toggle(void)
{
    phDriver_Pin_Config_t pinVenCfg = {
         .bPullSelect = PH_DRIVER_PULL_UP,
   .bOutputLogic = PH_DRIVER_SET_LOW
    };

    phDriver_Pin_Config_t pinSspConfig = {
   .bPullSelect = PH_DRIVER_PULL_DOWN,
   .bOutputLogic = 1
    };

    /* toggle VEN PIN */
    phDriver_PinConfig(PH_DRIVER_PIN_VEN, PH_DRIVER_PINFUNC_OUTPUT, &pinVenCfg);
    phDriver_TimerStart(PH_DRIVER_TIMER_MILLI_SECS, 20U, NULL);

    phDriver_PinConfig(((GPIO_PORT_B << 8) | THIRD_PINNUM_SSP) ,
 PH_DRIVER_PINFUNC_OUTPUT, &pinSspConfig);
    phDriver_TimerStart(PH_DRIVER_TIMER_MILLI_SECS, 5U, NULL);
    phDriver_PinConfig(((GPIO_PORT_B << 8) | THIRD_PINNUM_SSP) , PH_DRIVER_PINFUNC_INPUT,
 &pinSspConfig);

    phDriver_PinWrite(PH_DRIVER_PIN_VEN, PH_DRIVER_SET_HIGH);
    phDriver_TimerStart(PH_DRIVER_TIMER_MILLI_SECS, TVEN_BOOT_POR, NULL);
}
```

The load switch controlling pin must be held low long enough to guarantee that VBAT is below 200 mV for more than 5 ms.

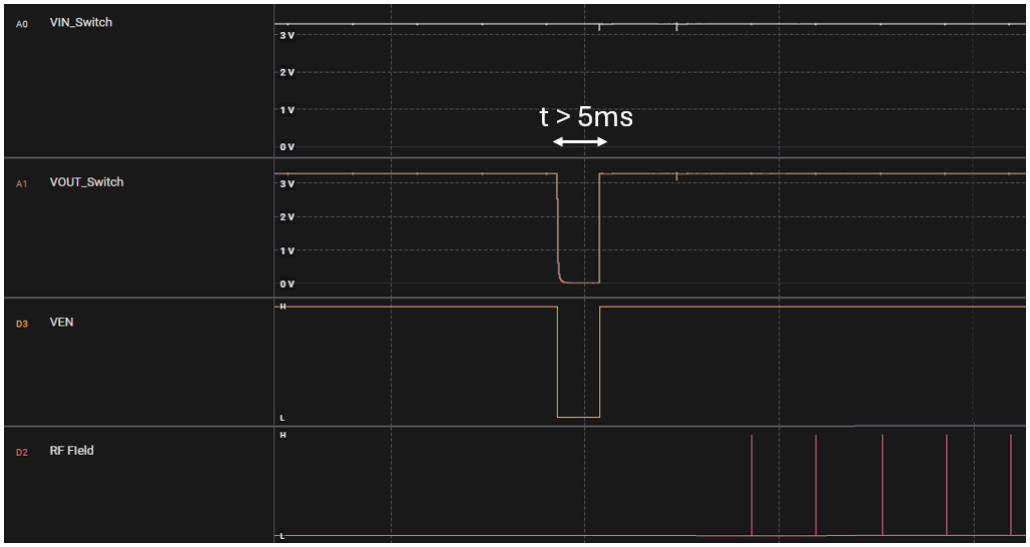

Figure 3. Load switch toggle: VEN, VBAT (VOUT_Switch)

4 No-host external watchdog

Note: *The no-host external watchdog functionality is only available on PN7642. For more information, refer to ref.[2] and ref.[4].*

If no host controller is available or the NFC controller shall be independent, the power domain control can be done via an external watchdog. The watchdog is periodically fed by the NFC controller itself. In case the NFC controller gets unresponsive the watchdog is no longer fed and triggers a load switch to reset the NFC controller's power domains.

In ULPCD a test bus signal can be used to feed the watchdog. On PN7642, the test bus is tide to GPIO_0/1/2/3. On GPIO_0 the ULPCD_ON signal can be output, which feeds the watchdog periodically with every ULPCD ping.

The external watchdog shall only be enabled during ULPCD mode. This can be implemented using any available GPIO, with the exception of GPIOs 0–3.

See the external watchdog concept in the Figure 4.

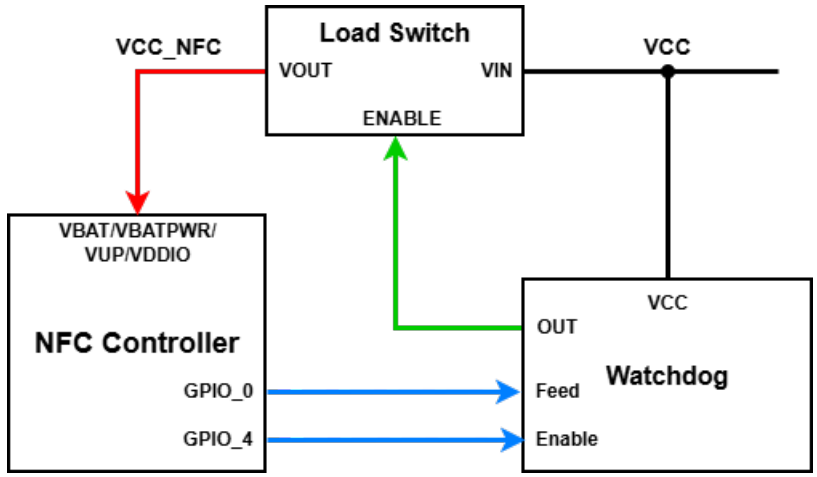

Figure 4. External watchdog concept

4.1 Test bus and pin configuration

The watchdog needs to be fed periodically. For this the test bus needs to be enabled and configured. If the test bus is enabled, the GPIO_0/1/2/3 are exclusively used for test bus signals and cannot be used for any other function during ULPCD operation.

Table 1. Watchdog concept mapping

NFC controller	Watchdog	Load switch	Comment
GPIO_0	FEED	NC	GPIO_0 is configured for the ULPCD_ON signal and will feed the watchdog with every ULPCD ping.
GPIO_4	ENABLE	NC	GPIO_4 is used from the NFC controller to enable/disable the watchdog. Before entering ULPCD mode, GPIO_4 shall be pulled low to enable the watchdog. If the NFC controller is in application (active) mode, GPIO_4 shall be pulled high to disable the watchdog. (1)
NC	OUT	ENABLE	The watchdog OUT signal is triggering the load switch (ENABLE) in case the watchdog timer elapses.

Note: *(1) - Valid for ENABLE pin with Active-low logic.*

IMPORTANT**:** This excludes GPIO_3 as the wake-up source of ULPCD. The host cannot wake-up the NFC controller by toggling GPIO_3.

Instead of using GPIO_3, the *VEN* can be used to bring the NFC controller out of ULPCD.

Test bus configuration on PN7642

The test bus configuration must be set every time before entering ULPCD, this includes the calibration phase:

```
PN76_HALREG_SET_REG(PCRM_ULPCD_CTRL4, 0x000100E4); //enables test bus
```

After waking up from ULPCD due to ULPCD detection the test bus shall be disabled and cleared, and the GPIOs can be freely used again.

```
PN76_HALREG_SET_REG(PCRM_ULPCD_CTRL4, 0x00000000); //sets test-bus configuration to all 0
PN76_HALREG_SET_REG(PCRM_ULPCD_CTRL3, 0x80000000); //clears test-bus configuration
```

4.2 Watchdog requirements

For this application, it is recommended to use an independent watchdog timer circuit. The selected watchdog shall provide the following functions:

- Watchdog type → Timeout watchdog
- Support **enable** function
- Timeout period → Several multiples of the *wULPCDWakeUpTime*. Recommended within a second-long range.
- Watchdog Active Time → This period must be long enough to meet this condition: ***VBAT must be below 200 mV for more than 5 milliseconds to guarantee a proper internal reset.*** Typically tens of milliseconds (It depends on the selected load switch and its quick output discharge characteristic).
- Low current consumption

See examples of watchdogs that meet these criteria and were empirically tested by NXP:

- SGM819S-FBXUDL6G/TR: ref.[7]
- TPS3435CAKAGDDFR: ref.[8]
- TPS3435CAIEGDDFR: ref.[9]

Customers are required to conduct robustness testing at the application level using the selected watchdog and their HW.

5 Load switches

The purpose of the load switch is to be able to control the power supply domain of the connected NFC controller. Due to the capacitance in the system, a discharge path is recommended to shorten the time of discharge significantly.

The customer can choose an integrated load switch with a fast output discharge feature or design and implement a custom MOSFET-based switch.

Tested load switches :

NX3P1108UK: ref.[5] (Max input voltage 3.6 V)

TPS22991L02: ref.[6] (Max input voltage 5.5 V)

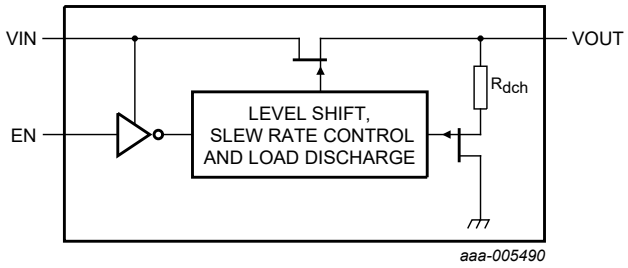

Figure 5. Logic diagram NX3P1108UK

6 Abbreviations

Table 2. Abbreviations

Abbreviation	Description
ULPCD	Ultra Low Power Card Detection
HIF	Host Interface
NFC	Near Field Communication

7 References

[1] Webpage – PN76AC – Plug-and-Play NFC Controller Connecting to NXP's MCU and MPU Portfolio (link)
[2] Webpage – PN7642 – Single-Chip Solution with High-Performance NFC Reader, Customizable MCU, and Security Toolbox (link)
[3] User Manual – UM12399 – PN76AC NFC controller user manual
[4] User manual – UM11905 – PN76 family instruction manual (link)
[5] Datasheet – NX3P1108UK – Logic controlled high-side power switch (link)
[6] Datasheet – TPS22991L02 – Load Switch With Quick Output discharge (link)
[7] Datasheet – SGM819S-FBXUDL6G/TR – Watchdog Timer Circuit (link)
[8] Datasheet – TPS3435CAKAGDDFR – Watchdog Timer Circuit (link)
[9] Datasheet – TPS3435CAIEGDDFR – Watchdog Timer Circuit (link)

8 Note about the source code in the document

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9 Revision history

Table 3. Revision history

Document ID	Release date	Description
AN15028 v.1.1	11 May 2026	Document security status updated to "public". • Section 1.1 "Supported devices": added PN7642. • Section 3.2 "Toggle load switch": updated. • Section 4 "No-host external watchdog": added. • Section 5 "Load switches": updated. • Section 7 "References": updated. • Section 8 "Note about the source code in the document": added.
AN15028 v.1.0	29 April 2026	Initial version

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Tables

Figures

Contents