AN14910

PF09 Hardware guidelines

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Document information

Information	Content
Keywords	PF09, system basis chip, power management, functional safety, ISO pulses, non-ISO pulses, EMC, external components, SPI, hardware.", PF09, I2C, hardware.
Abstract	This application note provides product guidelines and performance results (ISO pulses, EMC...) for the PF09 system basis chip (SBC) family in automotive electronic systems.

1 General description

The PF09 power management integrated circuit (PMIC) is optimized for high-performance i.MX95 based applications. It features five high-efficiency buck converters and four linear regulators for powering the processor, memory and miscellaneous peripherals. PF09 provides low quiescent current in standby and low-power off modes.

The PF09 is developed in compliance with automotive ISO 26262 and industrial IEC 61508 safety standards, including safety features, with failsafe outputs and integrated self-test mechanisms, becoming part of a safety oriented system partitioning targeting high integrity safety levels up to automotive ASIL D and industrial SIL-2.

2 Features and benefits

2.1 System support

- Two external voltage monitoring inputs.
  - Dynamic monitoring voltage selection
  - Selectable monitoring threshold with up to 1% monitoring accuracy
- Programmable I/O interface pins
- Advance frequency management with frequency spread spectrum
- Multi-channel analog multiplexer for system voltage monitoring
- High speed I_2C interface with up to 3.4 MHz operation
- Advance thermal monitoring and thermal shutdown protection

2.2 Configuration and enablement

- QFN 56 pins with exposed pad for optimized thermal management
- Permanent device customization via multiple time programmable configuration (OTP and MTP) fuse memory
- OTP Emulation mode for hardware development and evaluation
- Debug mode for software development, MCU programming, and debugging

2.3 Operating range

- Pre-regulated input voltage from 2.7 V to 5.5 V but optimized for 3.3 V to 5.0 V
- Ultra-low power always-on LDO supply
- Low power OFF mode with 10 µA quiescent current
- Low power Standby mode with 200 µA quiescent
- Up to five buck regulators with internal power stage and programable current limit and three low dropout linear regulators with load switch operation
- Operating switching frequency from 1.9 MHz to 3.15 MHz

2.4 Power supplies

- SW1: Single phase synchronous buck converter with integrated field effect transistors (FET). Configurable output voltage (0.5 V to 3.3 V) and switching frequency, output DC current capability up to 3.5 A, and PFM mode for low power Standby mode operation.
- SWx: Multi phase synchronous buck converter (4 in total) with integrated field effect transistors (FET). Configurable output voltage (0.3 V to 3.3 V) and switching frequency, output DC current capability up to 2.5 A, and PFM mode for low power Standby mode operation.
- LDO1: LDO/Load switch with output voltage from 0.75 V to 3.3 V and up to 500 mA current capability.

- LDO2 and LDO3: Low power LDO/Load switch with output voltage from 0.65 V to 3.3 V and up to 200 mA current capability.
- Ultra-low power Always-on LDO supply: Configurable output voltage: 1.8 V, 3.0 V or 3.3 V with up to 2% DC accuracy.
- Two external voltage monitoring inputs.

2.5 Compliancy

- Electromagnetic compatibility (EMC) optimization techniques for switching regulators, including spread spectrum, slew rate control, and manual frequency tuning
- Electromagnetic interference (EMI) robustness supporting various automotive EMI test standards
- Automotive qualified by AEC-Q100 rev J up to Grade 1

2.6 Functional safety

- Functional safety architecture to target up to ASIL-D automotive applications
- Functional safety architecture to target up to SIL-2 industrial applications
- Independent monitoring circuitry, dedicated interface for microcontroller monitoring, simple or challenger watchdog function
- Analog built-in self-test (ABIST) and logical built-in self-test (LBIST) at startup
- Analog built-in self-test (ABIST) on demand
- Dedicated Fail-safe output (FS0B)
- Safety outputs with latent fault detection mechanism (RSTB, FS0B, INTB)
- External fault detection inputs (FCCU, ERRMON)
- Protected I2C protocol with CRC verification
- Hash fault monitoring (dynamic CRC)

3 Applications

- Automotive infotainment
- High-end consumer and industrial
- Connectivity domain controller
- Telematics

4 Simplified diagrams

Figure 1 shows a simplified block diagram for a typical system with an PF09.

The PF09 PMIC is fully programmable via the I2C interface however additional interfacing between MCU, using provided direct logic interfacing pins.

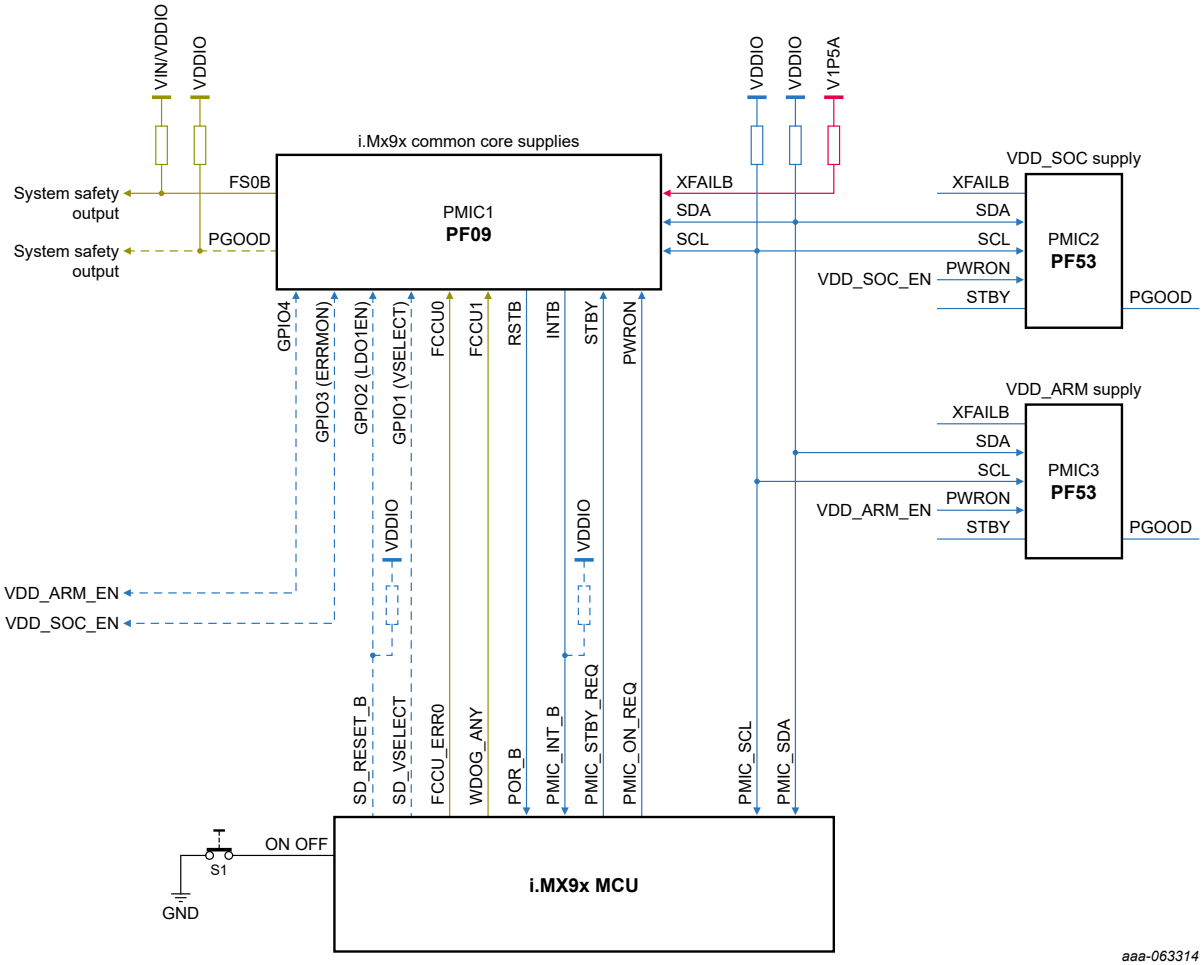

Figure 1. Example of application diagram

5 PF09 external components

All external components must be automotive grade, AEC-Q100 (for IC chip), AEC-Q101 (for discrete components), and AEC-Q200 (for passive components).

5.1 SMPS Buck power supplies

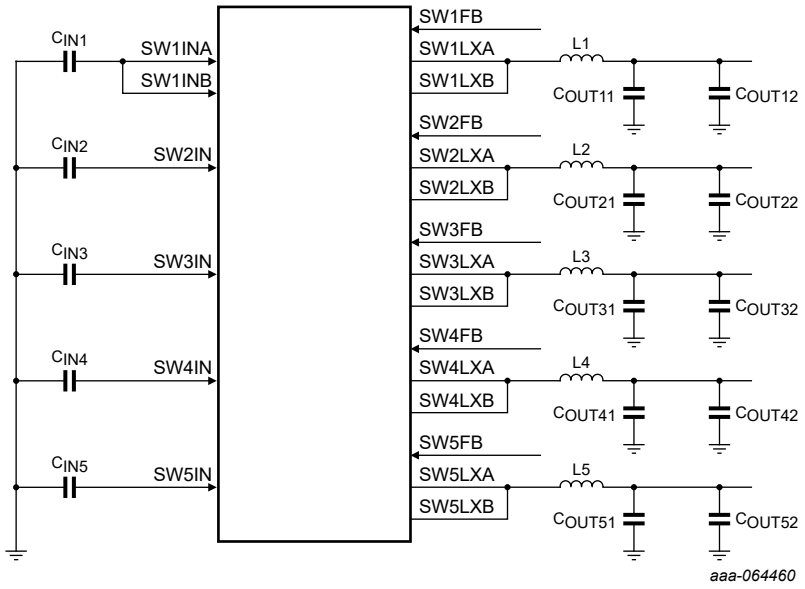

Figure 2. Power supply connections with buck configuration

Table 1. Bucks power supply components list

Components	Description	Recommendation
C_{IN1}, C_{IN2}, C_{IN3}, C_{IN4}, C_{IN5}	Input capacitor for the switched power outputs.	• 4.7 µF nominal capacitor or more, ceramic. • X7R Low ESR ceramic capacitor • Place closed to the PMIC • Do not exceed maximum capacitance. • Capacitor voltage is recommended to be 2 to 3 times the Rail voltage, 10V or 16V at 5V rail for commercial ratings.
C_{OUT11}, C_{OUT12}, C_{OUT21}, C_{OUT22}, C_{OUT31}, C_{OUT32}, C_{OUT41}, C_{OUT42}, C_{OUT51}, C_{OUT52},	Output capacitance for the switched ower outputs.	• Place 2 x 22 µF nominal capacitor or more per output., ceramic • X7R Low ESR ceramic capacitor • Place closed to the inductor • Do not exceed maximum capacitance • Place close to inductor
L_2, L_3, L_4, L_5,	Switchers 2 to 5 inductor.	• 0.47uH nominal • Shielded, ± 20 % tolerance • L_{DCR} resistance < 24mΩ • $I_{SATURATION}$ >5.8A • Soft saturation recommended • Place inductor close to the switching node
L_1	Switcher 1 inductor.	• 0.47uH nominal • Shielded, ± 20 % tolerance • L_{DCR} resistance < 14mΩ • $I_{SATURATION}$ ≥10A (Select according to the application inrush current) • Soft saturation recommended

Table 1. Bucks power supply components list*...continued*

Components	Description	Recommendation
		• Place inductor close to the switching node

5.2 LDO power supply

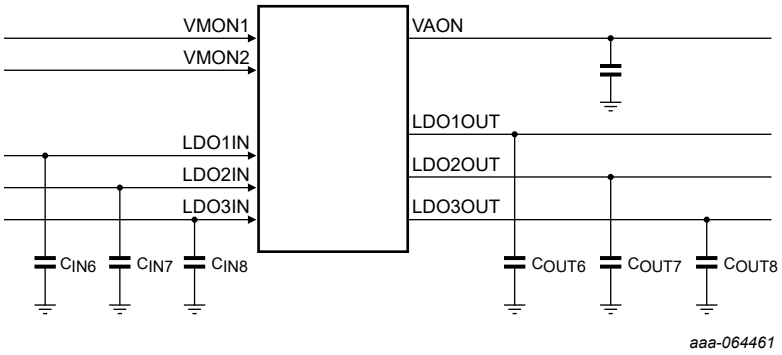

Figure 3. Power supply connections with buck configuration

Table 2. LDO power supply components list

Components	Description	Recommendation
C_{IN6}, C_{IN7}, C_{IN8}	Input capacitor for the switched power outputs.	• 1 µF nominal ceramic capacitor • X7R Low ESR ceramic capacitor • Place closed to the PMIC • Do not exceed maximum capacitance • Capacitor voltage is recommended to be 2 to 3 times the rail voltage, 10 V or 16 V at 5 V rail for commercial ratings
C_{OUT6}, C_{OUT7}, C_{OUT8}	Output capacitor for the Switched Power outputs.	• 4.7 µF nominal ceramic capacitor or more • X7R low ESR ceramic capacitor • Place closed to the PMIC • Do not exceed maximum capacitance • Capacitor voltage is recommended to be 2 to 3 times the rail voltage, 10 V or 16 V at 5 V rail for commercial ratings

5.3 Device interface

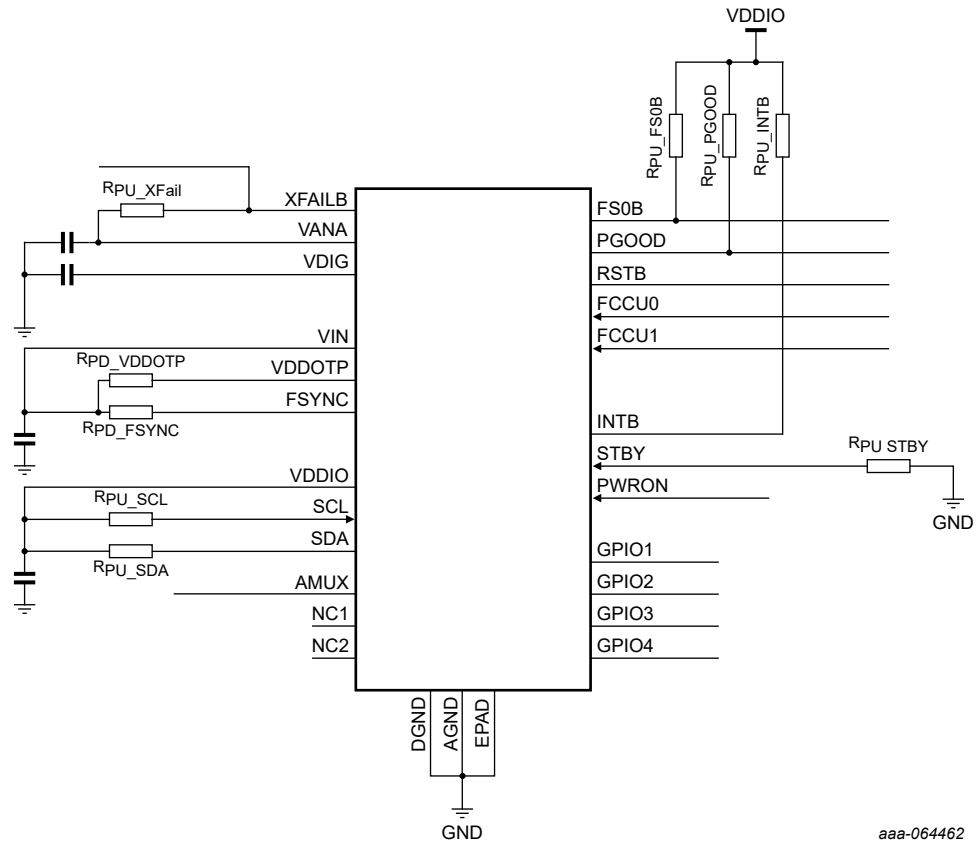

Figure 4. Device interface

Table 3. Device configuration

Components	Description	Recommendation		
RPU_XFAILB	XFAILB Pin for PMICs synchronization.	• Pull-up resistor to VANA, typical value, 10 KΩ		
RPD_VDDOTP	VDDOTP pin for PMIC operation mode configuration.	• Normal mode, pull-down resistor to GND, resistance higher than 1kΩ. recommended 100 KΩ		
RPD_FSYNC	FSYNC pin for switching synchronization with external devices.	• Pull-down resistor to GND, 100 KΩ recommended.		
RPU_SCL	SCL pin for I2C clock line.	• Pull-up resistor to VDDIO. According on the operation mode. Only one set of resistors in the line	External pull-up fast mode plus	2.2 KΩ
			External pull-up high speed	0.8 KΩ
RPU_SDA	SDA pin for I2C Data line.	• Pull-up resistor to VDDIO. According on the operation mode. Only one set of resistors in the line.	External pull-up fast mode plus	2.2 KΩ
			External pull-up high speed	0.8 KΩ
RPU_FS0B	FS0B pin for safe fail notification and	• Pull-up resistor of 10 KΩ to VDDIO recommended		

Table 3. Device configuration*...continued*

Components	Description	Recommendation
	synchronization with external PMICs.	
RPU_RPU_PGOOD	PGOOD pin indicator.	• Pull-up resistor of 10 KΩ to VDDIO recommended
RPU_INTB	INTB pin for interruption events notification.	• Pull-up resistor of 10 KΩ to VDDIO recommended
RPD_STBY	STBY pin to enter into Standby mode.	• Pull-down resistor to GND, 100 KΩ Recommended
VAON	Always On LDO (10mA)	• Use a 2.2 uF capacitor
VDIG	Internal use only LDO.	• Use a 1 uF capacitor
VAN	Internal use only LDO.	• Use a 1 uF capacitor
VDDIO	PMIC internal circuitry power	• Place a 100 nF capacitor

6 Schematic, board layout, and bill of materials

6.1 PF09 IO interface

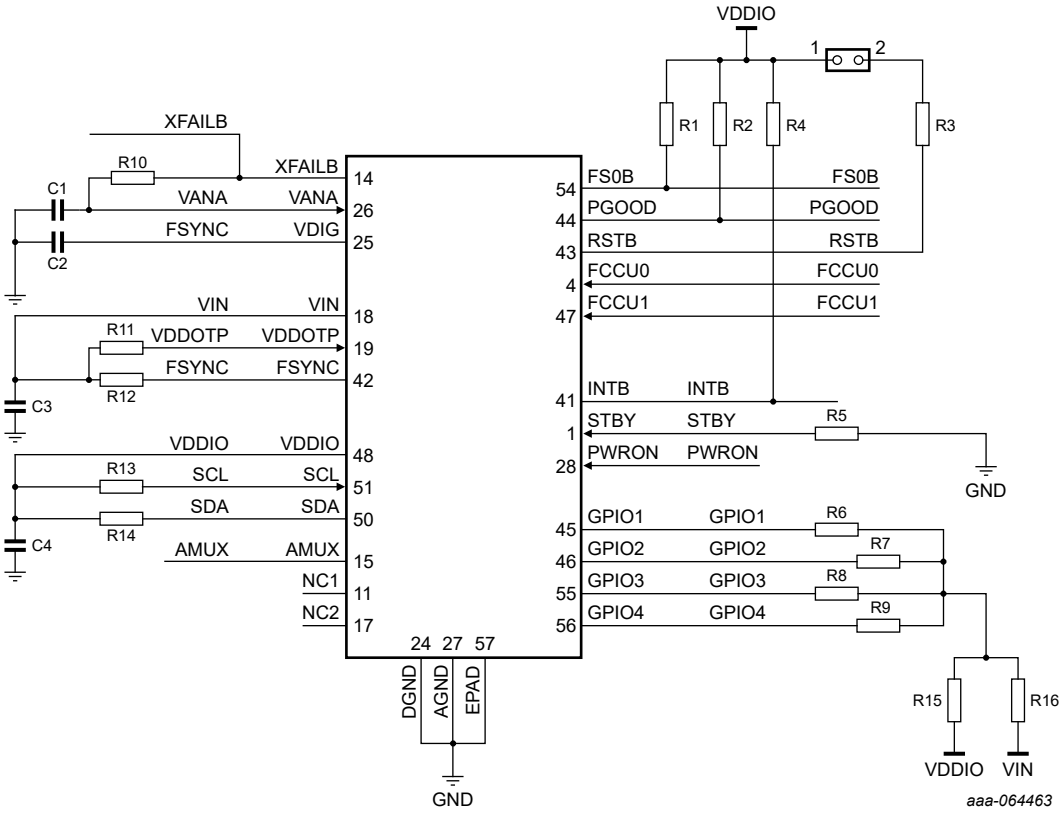

Figure 5. PF09 IO INTERFACE

Circuitry for:

- Configuration

- Safety outputs
- Voltage monitoring
- Communication

Table 4. I/O interface

Reference	Qty	Description	Vendor	Part Nbr	Value
C1, C2, C3	3	CAP CER 1uF 10V 10% X7S AEC-Q200 0402	MURATA	GCM155C71A105 KE38D	1 uF
C4	1	CAP CER 0.1uF 16V 10% X7R AEC-Q200 0402	MURATA	GCM155R71C104 KA55D	0.1 uF
R1,R2,R3,R4	4	RES MF 10K 1/10W 5% AEC-Q200 0603	KOA SPEER	RK73B1JTTD103J	10 K
R5, R6, R7, R8, R9, R10, R11, R12	8	RES MF 100K 1/10W 5% AEC-Q200 0603	VISHAY INTERT ECHNOLOGY	CRCW0603100KJNEA	100 K
R13, R14	2	RES MF 2.20K 1/10W 1% AEC-Q200 0603	KOA SPEER	RK73H1JTTD2201F	2.20 K
R15 (NP), R16	1	RES MF ZERO OHM -- AEC-Q200 0603	KOA SPEER	RK73Z1JTTD	0

6.2 Switcher's circuitry

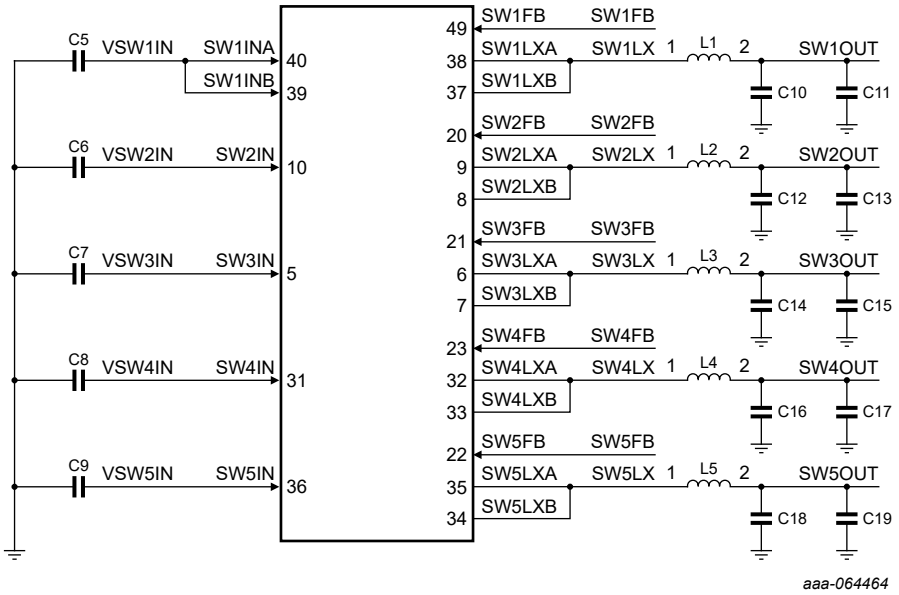

Figure 6. Switching regulators

Table 5. Switchers

Reference	Qty	Description	Vendor	Part Nbr	Value
C10, C11, C12, C13, C14, C15, C16, C17, C18, C19	15	CAP CER 22uF 10V 20% X7T AEC-Q200 0805	MURATA	GRT21BD71 A226ME13	22 uF
C5, C6, C7, C8, C9	5	CAP CER 4.7uF 16V 10% X7S AEC-Q200 0603	MURATA	GRT188C71 C475KE13	4.7 uF

Table 5. Switchers...*continued*

Reference	Qty	Description	Vendor	Part Nbr	Value
L1	1	IND PWR 0.47uH@100kHz 6.8A 0.014OHM 20% SMT	WURTH ELE KTRONIK EISOS GMBH & CO. KG (ELECTRONIC & ELECTROME HANICAL COMP)	744373240047	0.47 uH
L2, L3, L4, L5	4	IND PWR 0.47uH@1MHz 5.8A 20% AEC-Q200 SMT	TDK	TFM252012 ALMAR47MTAA	0.47 uH

6.3 LDO outputs circuitry

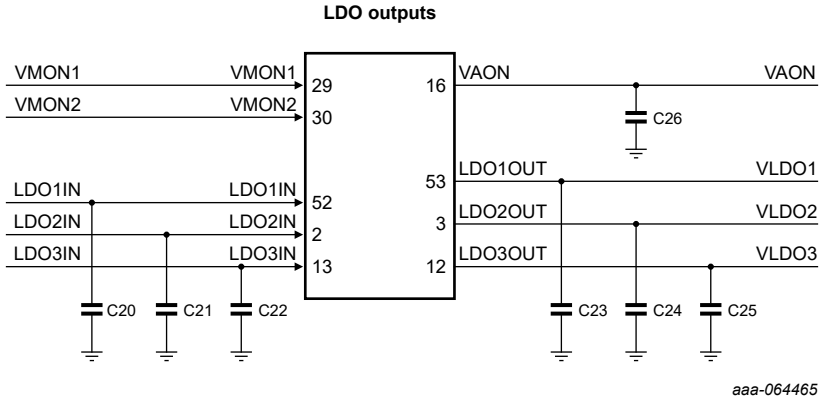

Figure 7. LDOs

Table 6. LDOs

Reference	Qty	Description	Vendor	Part Nbr	Value
C20, C21, C22	3	CAP CER 1uF 10V 10% X7S AEC-Q200 0402	MURATA	GCM155C71A105 KE38D	1 uF
C23, C24, C25	3	CAP CER 4.7uF 16V 10% X7S AEC-Q200 0603	MURATA	GRT188C71C475 KE13	4.7 uF
C26	1	CAP CER 2.2uF 10V 10% X7S AEC-Q200 0402	MURATA	GRT155C71A225KE13	2.2 uF

7 EMC performances

7.1 PCB components placement

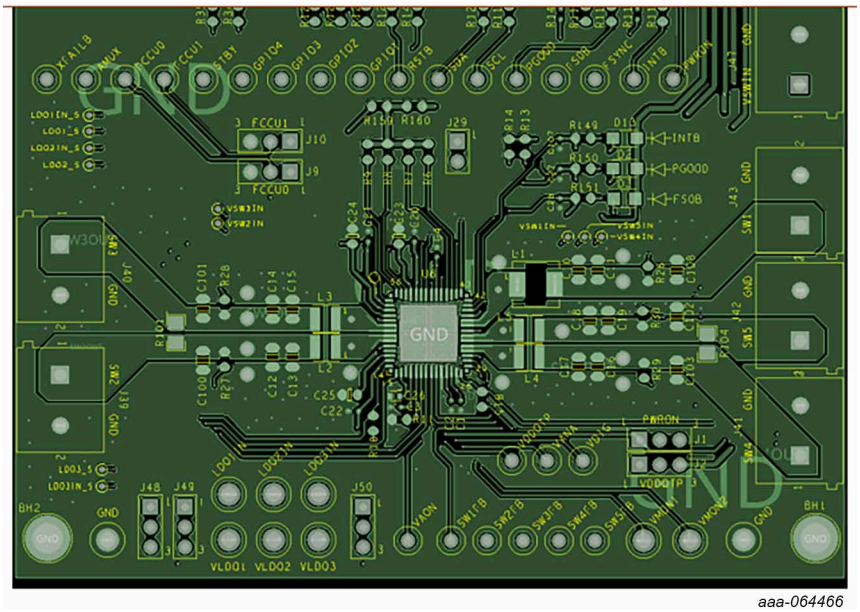

Figure 8. Example of component placement - Top PCB view

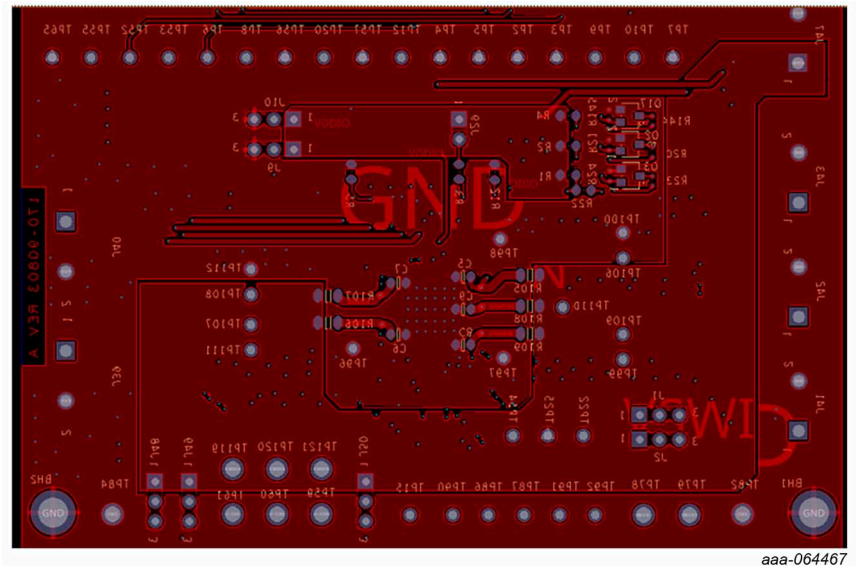

Figure 9. Example of component placement - Bottom PCB view

7.2 Layout guidelines

The design uses six PCB layers:

- L1: Top layer used as DC-DC output power planes, signals and ground
- L2: System ground
- L3: Mainly Ground and signals

- L4: Mainly Ground and signals
- L5: System Ground
- L6: Ground and SWVIN

7.2.1 General layout guidelines/recommendations

Layout is important to the EMC/EMI in SMPS. Layout recommendations are:

- High current lines should remain in the same plane, if required to route the high-current loop through multiple PCB layers, use multiple vias to mitigate the parasitic (R and L) in the high current path.
- Keep ground always close to the power line.
- When a signal is going through multiple PCB layers, ground vias around the layer interconnection are recommended to contain the electrical field.
- Some inductors have placement polarity. Ensure proper polarity to ensure the minimum magnetic field.
- Do not place inductors over control lines, feedback, etc. Trace together with ground.
- Input and output capacitors must have proper return.
  - Current loops (SMPS and LDOS) must be routed as small as possible.
  - Avoid broken grounds.
  - Power line must be one dielectric away from ground.
- Avoid low-level signals below SMPS power components, specially inductors.
- Do not route feedback lines in parallel to inductor lines, have them ideally 90 degrees when close to the inductor.
- Have SMPS current loops as small as possible with wide tracks. Use shorter traces as possible for all lines. Specially feedback.
- Use thermal pads with thermal vias.

7.3 Thermal management

The PF09 package is HVQFN56, plastic thermal enhanced very thin quad flat pack; no leads, wettable flank, 56 terminals, 0.5 mm pitch, 8 mm x 8 mm x 0.53 mm body. Details of the PCB footprint design are available in the section titled 'Package Drawing' of the PF09 data sheet.

7.4 Product setup

All EMC tests were performed at 25 °C, with all regulators configured and loaded according to the *EMC compliance* section of the product data sheet.

7.5 Conducted emission at IC level (CE)

Table 7. Conducted emission at IC level (CE)

Document	Reference	Comments
IEC 62132-4	Measurement of electromagnetic immunity 150kHz to 1GHz. Part4: Direct RF Power Injection Method.	International Electrotechnical Commission, IEC
IEC 61967-4	Measurement of electromagnetic emissions, 150kHz to 1GHz. Part4: measurement of conducted emissions, 1Ω/150Ω direct coupling	
IEC 62228-3	EMC evaluation of transceivers – Part 3: CAN transceivers	
Product datasheet	https://www.nxp.com/products/PF09	NXP
Application board	https://www.nxp.com/products/PF09	NXP

7.5.1 Test Summary

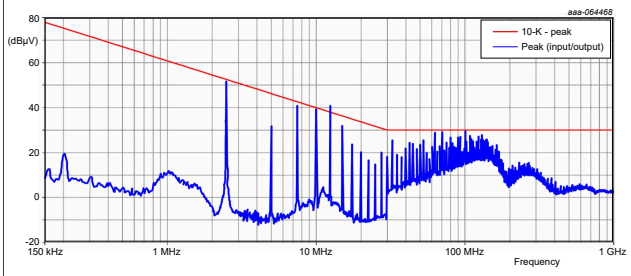

Figure 10. PF09 B0, RUN mode, CE on VIN

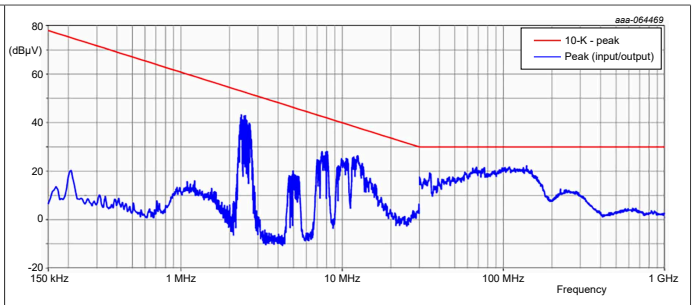

Figure 11. PF09 B0, RUN mode, CE on VIN with FSS_EN=1 (Triangular modulation)

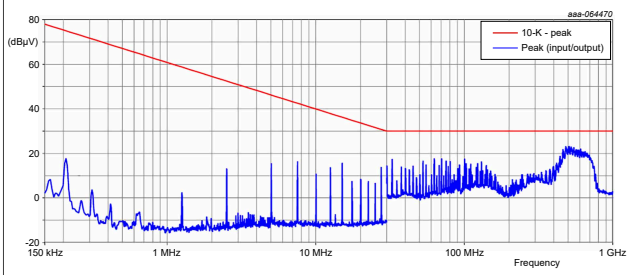

Figure 12. PF09 B0, RUN mode, CE on VAON

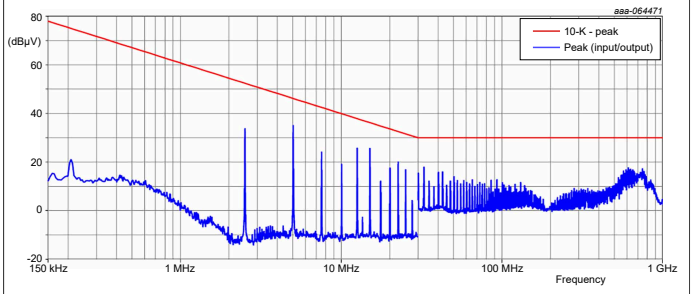

Figure 13. PF09 B0, RUN mode, CE on SW1

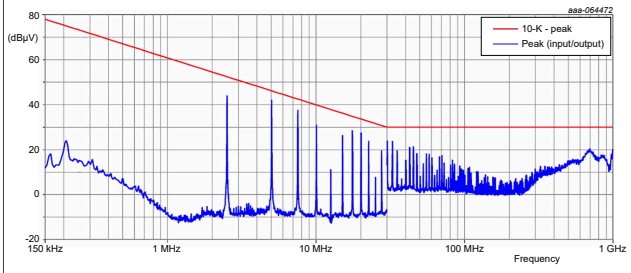

Figure 14. PF09 B0, RUN mode, CE on SW2

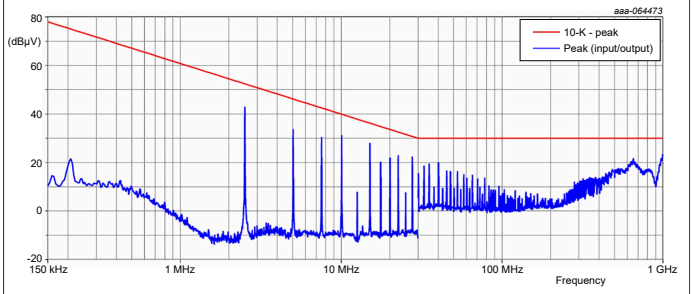

Figure 15. PF09 B0, RUN mode, CE on SW3

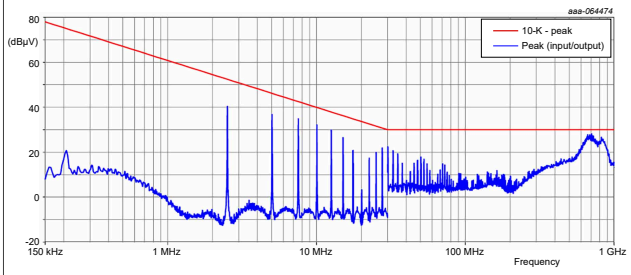

Figure 16. PF09 B0, RUN mode, CE on SW4

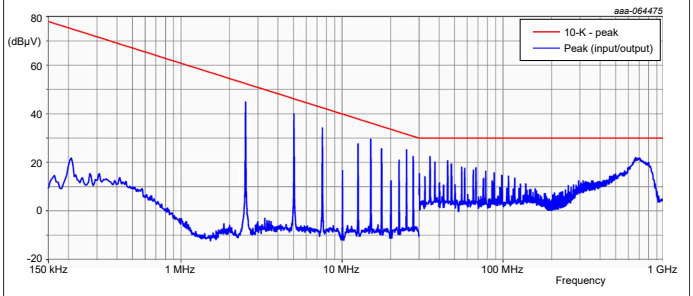

Figure 17. PF09 B0, RUN mode, CE on SW5

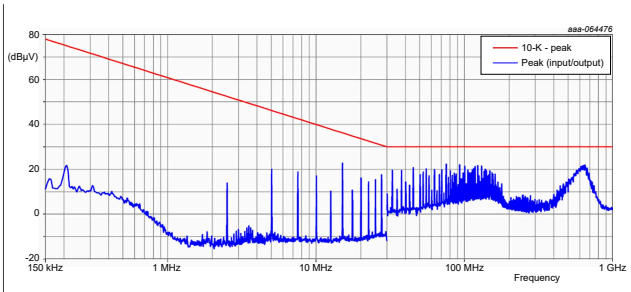

Figure 18. PF09 B0, RUN mode, CE on LDO1

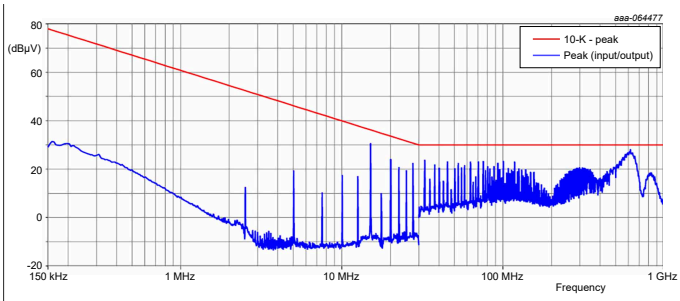

Figure 19. PF09 B0, RUN mode, CE on LDO2

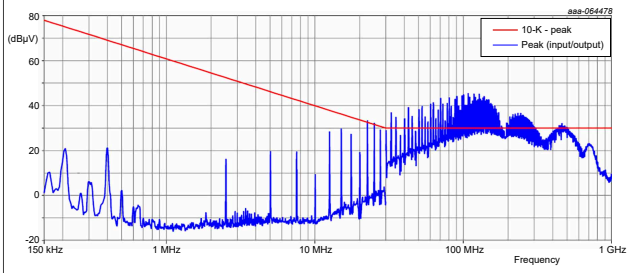

Figure 20. PF09 B0, RUN mode, CE on RSTB

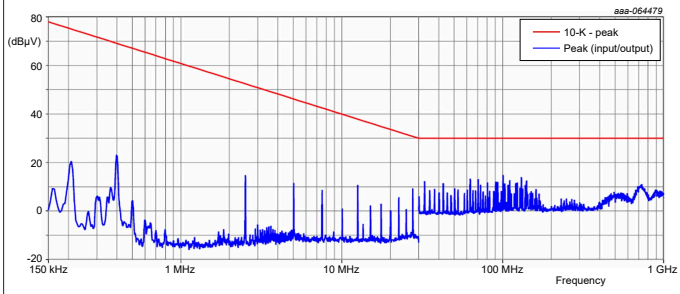

Figure 21. PF09 B0, RUN mode, CE on RSTB with an additional cap 1nF

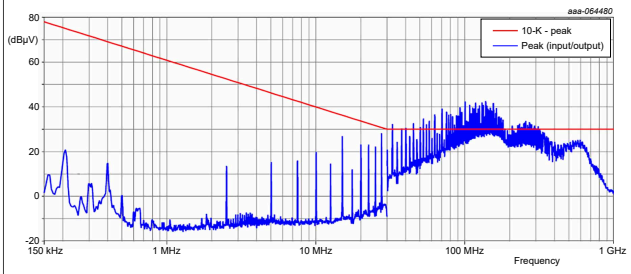

Figure 22. PF09 B0, RUN mode, CE on FS0B

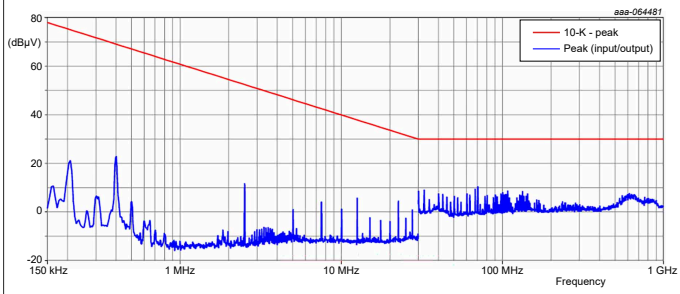

Figure 23. PF09 B0, RUN mode, CE on FS0B with an additional cap 1nF

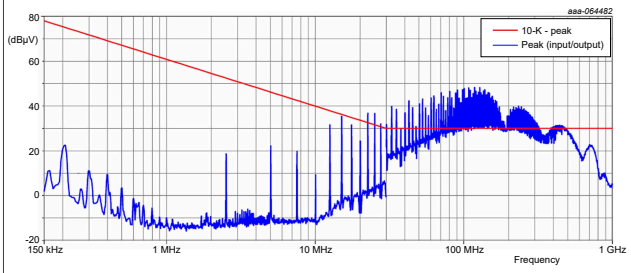

Figure 24. PF09 B0, RUN mode, CE on INTB

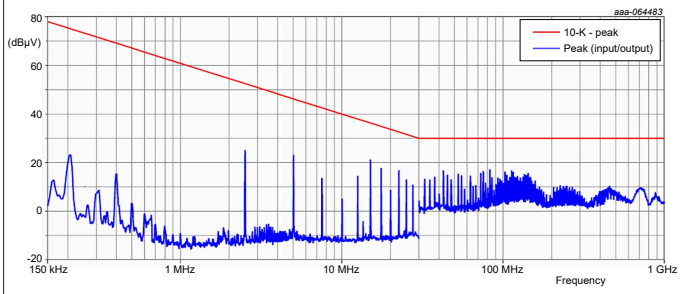

Figure 25. PF09 B0, RUN mode, CE on INTB with an additional cap 1nF

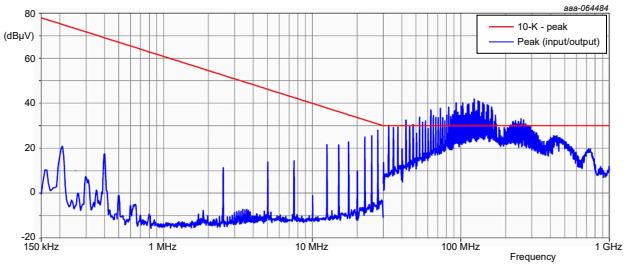

Figure 26. PF09 B0, RUN mode, CE on PGOOD

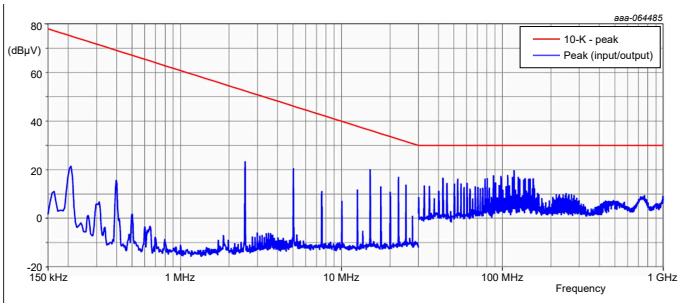

Figure 27. PF09 B0, RUN mode, CE on PGOOD with an additional cap 1nF

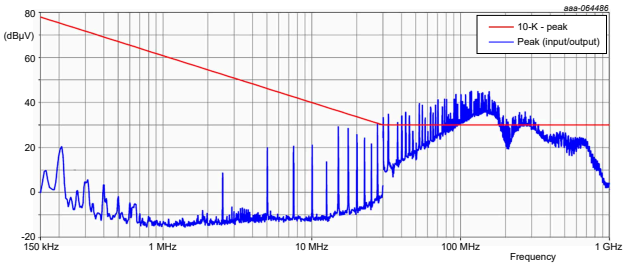

Figure 28. PF09 B0, RUN mode, CE on XFAILB

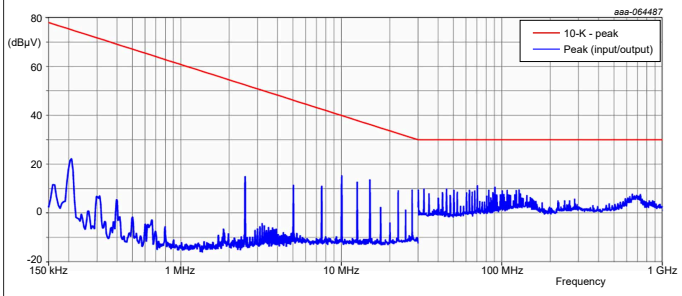

Figure 29. PF09 B0, RUN mode, CE on XFAILB with an additional cap 1nF

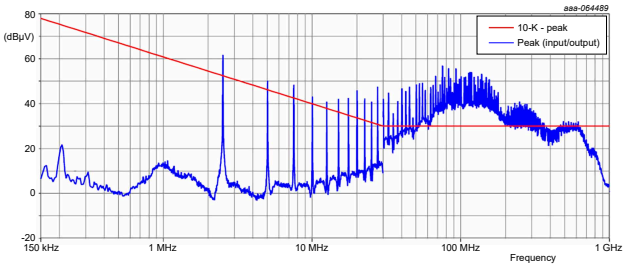

Figure 30. PF09 B0, RUN mode, CE on GPIO3

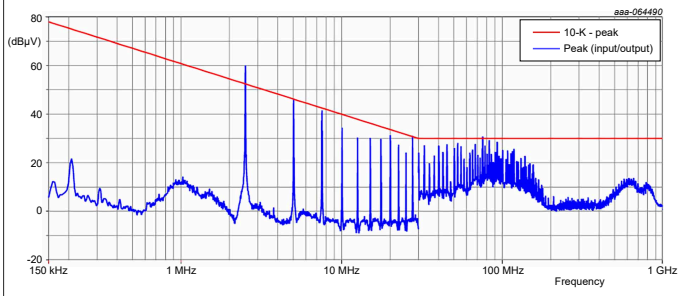

Figure 31. PF09 B0, RUN mode, CE on GPIO3 with an additional cap 1nF

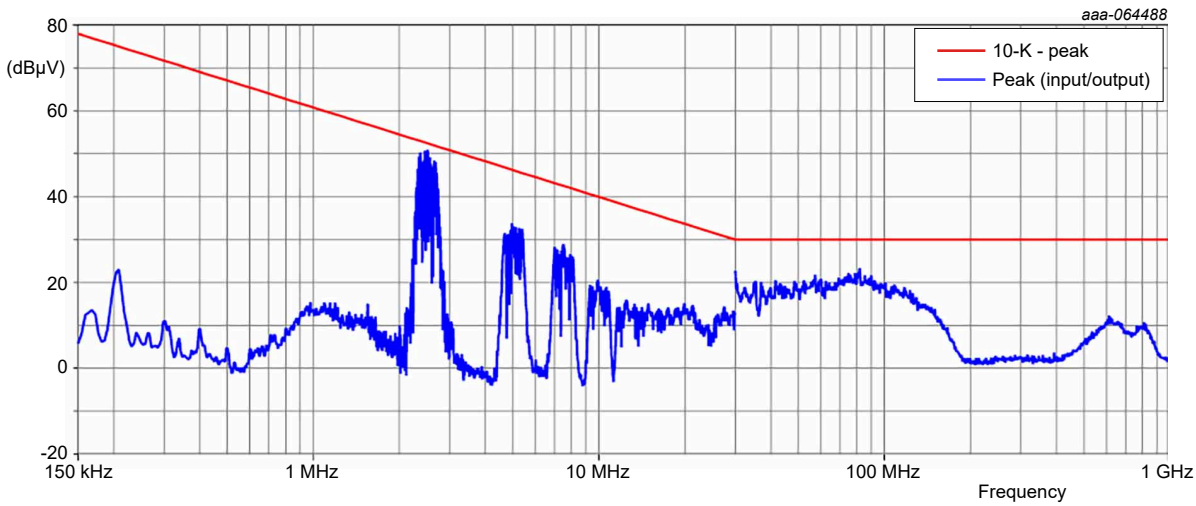

Figure 32. PF09 B0, RUN mode, CE on GPIO3 with a, additional cap 1nF, FSS_EN=1 (triangular modulation)

8 Revision history

Document ID	Release date	Description
AN14910 v.1.0	22 January 2026	Initial version

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