AN14901

MCX E31x Product Family Memory Management

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Document information

Information	Content
Keywords	AN14901, MCX E31x
Abstract	This application note provides a guideline about the memory features included in the MCX E31x Product Family. It also details the available functions and best practices for running applications with performance improvements.

1 Introduction

The purpose of this application note is to provide a guideline about the memory features included in the MCX E31x Product Family. This document details the available functions and best practices for running applications with performance improvements.

You can find four kinds of memories inside the MCX E31x Product Family—the flash memory, the SRAM, the Tightly Coupled Memory (TCM), and the cache memory. The MCX E31x Product Family also has some modules with dedicated memory, such as EMAC and CAN. This document focuses on flash memory, TCM, and SRAM.

The flash memory is dedicated for program code and data storage. Also, all devices in the family have a UTEST sector of 8 kB to store important configurations or to reserve information for the application. The MCX E31x Product Family has devices from 512 kB to 4 MB of Flash program memory.

The RAM is integrated by the SRAM memory and the TCM. Part of the SRAM memory is available in Standby mode. This means that the contents of this memory are retained after setting the MCU in Standby mode. The MCX E31x product family uses the TCM feature of Arm Cortex-M7, to ensure fast and deterministic access time to the cores to important data without delays. This feature can be exploited in real-time operating systems.

The cache memory is a dedicated memory for the cores. This memory is not part of the system memory and does not have a physical address available for the programmer. This memory serves as an intermediate buffer between the processor and the main memory to reduce memory access time for the cores.

2 Features

Table 1 describes the MCX E31x family devices memory features.

Table 1. MCX E31x memory features

Feature	NCX E315	MCX E316	MCX E317	MCX E31B
Core qty	1x Cortex-M7			
Program flash memory (MB)	512 kB	1	2	4
Data flash memory (kB)	64		128	
Cache	I Cache 8 kB D Cache 8 kB			
Total RAM (kB)	112 kB (including 96 kB TCM)	128 kB (including 96 kB TCM)	192 kB (including 96 kB TCM)	512 kB (including 192 kB TCM)
Standby RAM	16 kB		32 kB	

An important feature to note is that all memories inside the MCX E31x Product Family have Error Detection and Error Correction code.

3 Flash memory

The flash memory on MCX E31x devices is integrated by blocks. There are five blocks as maximum and two blocks as minimum. Table 2 describes detailed information about these blocks.

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Table 2. Flash memory architecture for MCX E31x

Flash blocks	MCX E315	MCX E316	MCX E317	MCX E31B
	End address – Start address (size)	End address – Start address (size)	End address – Start address (size)	End address – Start address (size)
UTEST	0x1B00_1FFF – 0x1B00_0000 (8 kB)	0x1B00_1FFF – 0x1B00_0000 (8 kB)	0x1B00_1FFF – 0x1B00_0000 (8 kB)	0x1B00_1FFF – 0x1B00_0000 (8 kB)
Block4 – Data flash memory	0x1000_FFFF – 0x1000_0000 (64 kB)	0x1000_FFFF – 0x1000_0000 (64 kB)	0x1001_FFFF – 0x1000_0000 (128 kB)	0x1001_FFFF – 0x1000_0000 (128 kB)
Block3– Code flash memory 3	Not available	Not available	Not available	0x007F_FFFF – 0x0070_0000 (1 MB)
Block2 – Code flash memory 2	Not available	Not available	Not available	0x006F_FFFF – 0x0060_0000 (1 MB)
Block1 – Code flash memory 1	Not available	0x004F_FFFF – 0x0048_0000 (512 kB)	0x005F_FFFF – 0x0050_0000 (1 MB)	0x005F_FFFF – 0x0050_0000 (1 MB)
Block0 – Code flash memory 0	0x0047_FFFF – 0x0040_0000 (512 kB)	0x0047_FFFF – 0x0040_0000 (512 kB)	0x004F_FFFF – 0x0040_0000 (1 MB)	0x004F_FFFF – 0x0040_0000 (1 MB)

In the MCX E31x Product Family, the devices are available from 512 kB to 4 MB of flash memory. The Table 2 classifies the MCX E31x Product Family devices by flash memory size.

There are some regions inside the flash memory that are protected for use by the application cores. These are only available for HSE_B core. For further details, see the *MCX E31x Reference Manual*.

There are three operations modes for the flash memory. When the device is working in User mode, the flash memory array is accessible to execute a read, program, or erase operation. The User mode is the default operating mode of the flash memory. All the registers have read and write access. In low power mode, the flash memory is not accessible because its power source is turned off, so operations are not allowed in this mode. Finally, the Utest mode is a test mode where the integrity of the flash memory can be verified.

The flash memory can perform multiple reads between different blocks by a single, dual, or quad read feature.

The following are four important operations to consider while working with the flash memory:

- Read flash memory
- Lock and unlock sector or super sector
- Program flash memory
- Erase flash memory

3.1 Read

After reset, the flash memory is in a default state, which has the arrays and register available to be read by the controller. A read operation from flash memory returns 256 bits of data length and register reads return 32 bits. For this operation, it is not necessary to consider a Lock or Unlock sector. The read operation is performed by the PFlash controller, which is an interface between the system bus and the embedded flash memory.

3.2 Write or program

The minimum program size is 2 words (64 bits) and data must be 64 bit aligned. A maximum of 4 pages can be programmed at the same time, where 1 page is 8 words (256 bits). This means that up to 1024 bits can be altered in a single program operation. When a program operation or write operation is made, the ECC bits are calculated and stored. The ECC is handled on 64-bit doubleword. Eight bits of ECC are needed.

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A program operation changes the logic value of a bit from 1 to 0, this means that a program operation from 0 to 1 is not allowed and the flash memory must be erased before any program operation.

Before a program operation occurs the sector that contains the specified address must be unlocked. If a locked sector or super sector is attempted to be programmed, program operation fails and an error is reported in the MCRS[PEP] bit.

Figure 1 shows the flow diagram to explain the program operation.

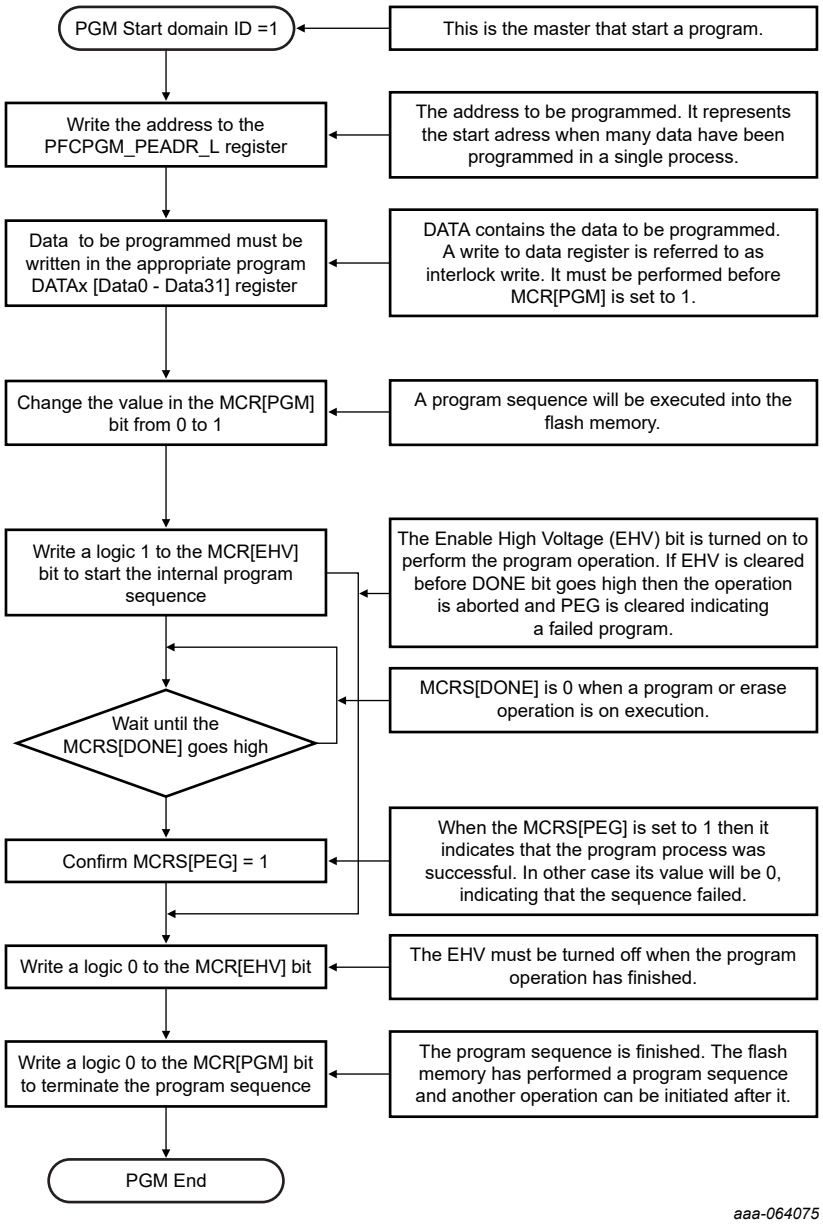

Figure 1. Program sequence flow diagram

3.3 Erase

The erase operation is the process to set all bits from a sector or block to 1. The minimum erase size can be performed in a sector, where a sector size is 8 kB. To erase a sector or block, it must be unlocked previously to the erase operation. The erase process also cleans the ECC bits.

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Figure 2 shows the flow diagram to explain the erase sequence.

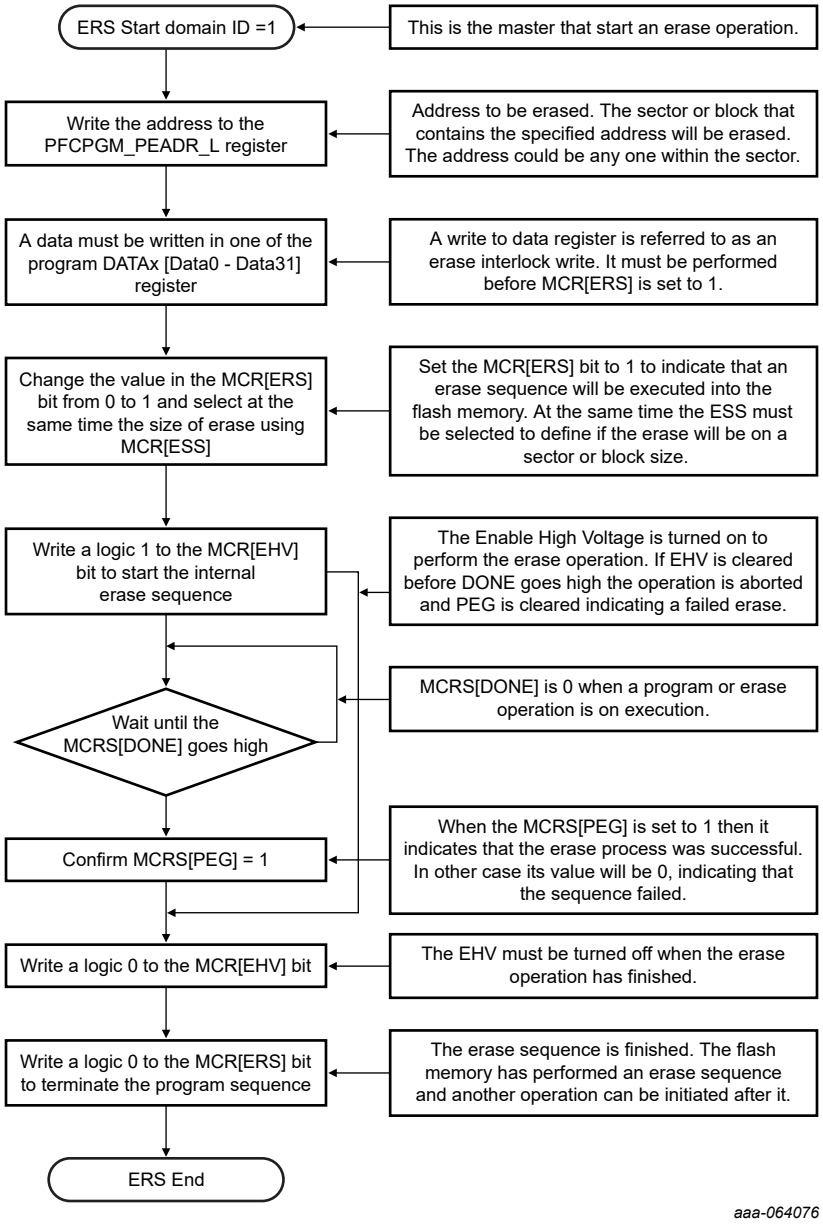

Figure 2. Erase sequence flow diagram

3.4 Locking and unlocking sector or super sector

A block is integrated by sectors and super sectors with sizes of 8 kB and 64 kB respectively. These sectors can be protected from write or erase operations by using the locking feature. The last 256 kB of the block has a sector protection feature, while the rest has the Super Sector protection feature. The data flash has a sector protection feature and the UTEST sector has independent sector program protection. The MCX E31x Product Family has some devices where Super Sector protection is not available due to memory size. For more information about these devices, see the *MCXE31x Reference Manual*.

Figure 3 shows the sector and super sector distribution for a 1 MB block.

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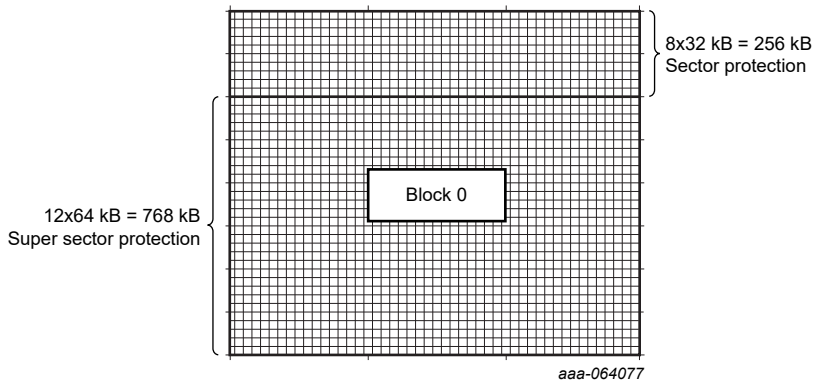

Figure 3. Sector distribution inside 1 MB block

The PFCBLKn_SSPELOCKn registers control the lock and unlock process for super sectors, and the PFCBLKn_SPELOCKn registers control it for sectors. The PFCBLKn_SSPELOCKn register has 12 available bits, where each bit corresponds to each super sector. Similarly, the PFCBLKn_SPELOCKn register has 32 available bits for 32 available sectors. If an unlock process is required to allow a program or erase operation, the corresponding register PFCBLKn_SSPELOCKn or PFCBLKn_SPELOCKn must be changed from 1 to 0. Writing 1 to any bit of PFCBLKn_SPELOCKn or PFCBLKn_SSPELOCKn locks the sector or super sector against programming and erasing operations.

After reset, all bits in the PFCBLKn_SSPELOCKn and PFCBLKn_SPELOCKn registers are set to 1, indicating that all sectors are protected from program and erase operations.

Figure 4 shows the steps to unlock a sector or super sector.

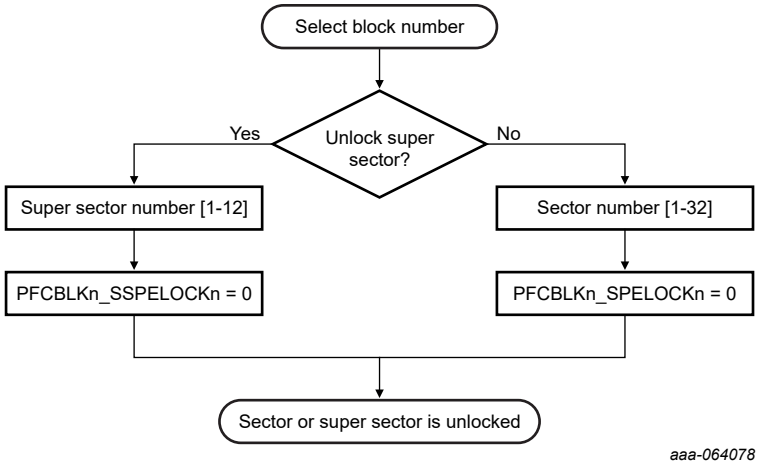

Figure 4. Unlock process for Sector or Super Sector

3.5 UTEST sector

The 8 kB UTEST sector is available in all devices from the MCX E31x Product Family. In this sector, it is possible to store important information about the application, such as version number, permanent parameters, and configurations (boot or applications). Inside the UTEST sector there are some regions that are reserved for the SoC and its use is reserved for NXP. For further details, see the *MCXE31xx_DCF_client.xlsx* attached in the *MCX E31x Reference Manual*.

The UTEST sector is a One Time Programmable (OTP) space when the Test mode seal is written. The Test mode seal is allocated in the UTEST sector and programmed with the value 0x5A4B3C2D for security. This means only new data or configuration can be appended in the UTEST sector, and erase is not allowed.

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The process to write a data in the UTEST sector is the same process used to program a data in other blocks. The unlocking process is similar, but the UTEST sector has its own register PFCBLKU_SPELOCK[SLCK] to lock or unlock the sector for program operations. As mentioned before, the UTEST sector is an 8 kB sector so there is only 1 bit to change in the PFCBLKU_SPELOCK register. Following the sector protection logic, if the SLCKbit is set to 0 then the UTEST sector is available for program operations.

4 Tightly coupled memory

Tightly Coupled Memory (TCM) is a memory implemented from the Arm Cortex-M7 architecture, having a dedicated connection to the core as the main characteristic. This memory is divided in Instruction TCM (I-TCM) and Data TCM (D-TCM). In the MCX E31x Product Family, there are two dedicated connections to the Cortex M7, one for the I-TCM and another for the D-TCM. Each CM7 core has an I-TCM and D-TCM memory available. Therefore, the sizes and addresses of the TCM memories depend on the number of cores available on the variant and its configuration. For details, see Table 3.

TCM is memory-mapped and can be accessed through two possible buses—a dedicated core connection and a backdoor access for any other Master on the AHBS bus. Each access has a defined start address for TCM and the end address is determined by the size of the memory. For details, see Table 3.

For the dedicated access for the core, the I-TCM has a bus interface of 64 bits and the D-TCM a bus interface of 32 bits. The TCM memory can be accessed via 32-bit AHB interface by any other master, such as the eDMA, a different core (when decoupled configuration), the EMAC, and the HSE core.

As TCM is a part of the memory map and has a physical address, the content can be stored in TCM at compile time. One advantage of using TCM is its deterministic access time (one clock cycle). Therefore, TCM can be used to store critical data and code, such as frequently updated variables, interrupt handlers, and data processing. This data is decided by the user and not by a control logic, such as the Cache memory.

TCM also has ECC protection as other memories. After power-on reset, it must be initialized to avoid ECC errors, this write operation is required to set up the initial ECC code words after the chip's power-on reset phase. In the MCX E31x Product Family, the cores can initialize I-TCM and D-TCM via direct and backdoor accesses. Also, the D-TCM can be initialized by the DMA via the backdoor, however, the DMA cannot initialize the I-TCM due to the 32-bit access that the backdoor provides (I-TCM needs 64-bit write to avoid ECC error).

5 SRAM

The MCX E31x Product Family devices can be integrated from 1 SRAM and up to 2 SRAM blocks. The Table 3 shows the RAM memory blocks available for each device.

Note: *The TCM memory is considered as part of the RAM memory.*

Table 3. RAM memory architecture for MCX E31x

RAM	MCX E315	MCX E316	MCX E317	MCX E31B
	End address – Start address (size)	End address – Start address (size)	End address – Start address (size)	End address – Start address (size)
SRAM2	Not available	Not available	Not available	Not available
SRAM1	Not available	Not available	Not available	0x2044_FFFF – 0x2042_8000 (160 kB)
SRAM0	0x2040_3FFF – 0x2040_0000 (16 kB)	0x2040_7FFF – 0x2040_0000 (32 kB)	0x2041_7FFF – 0x2040_0000 (96 kB)	0x2042_7FFF – 0x2040_0000 (160 kB)
Standby	ALL SRAM0 16 kB	ALL SRAM0 32 kB	0x2040_ FFFF – 0x2040_0000 (64 kB of SRAM0)	0x2040_ FFFF – 0x2040_0000 (64 kB of SRAM0)
DTCM2	Not available	Not available	Not available	Not available

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Table 3. RAM memory architecture for MCX E31x*...continued*

RAM	MCX E315	MCX E316	MCX E317	MCX E31B
	End address – Start address (size)	End address – Start address (size)	End address – Start address (size)	End address – Start address (size)
DTCM1	Not available	Not available	Not available	BD 0x2140_FFFF – 0x2140_0000 (64 kB)
DTCM0	0x2000_FFFF – 0x2000_0000 (64 kB)	0x2000_FFFF – 0x2000_0000 (64 kB)	0x2000_FFFF – 0x2000_0000 (64 kB)	0x2000_FFFF – 0x2000_0000 (64 kB)
ITCM2	Not available	Not available	Not available	Not available
ITCM1	Not available	Not available	Not available	BD 0x1140_FFFF – 0x1140_0000 (32 kB)
ITCM0	0x0000_7FFF – 0x0000_0000 (32 kB)	0x0000_7FFF – 0x0000_0000 (32 kB)	0x0000_7FFF – 0x0000_0000 (32 kB)	0x0000_7FFF – 0x0000_0000 (32 kB)
TOTAL	112 kB	128 kB	192 kB	512 kB

Each SRAM block has its own SRAM controller (PRAMC) to support fast read/write accesses to the cores. The PRAM controller is the interface between the system bus and the integrated RAM array. The system bus supports 64 bits of data and the RAM array supports 64 bits of data + 8 bits for ECC.

Inside the SRAM memory, a region is available when the microcontroller is in Standby mode. The Standby SRAM is allocated at the first 32 kB of the SRAM memory. This region is sourced by the Power Domain 0. Therefore, when a Standby mode is performed, the information that is stored in the Standby region is retained. The rest of the SRAM memory is sourced by the Power Domain 1 and it is only available in Run mode.

Similar to TCM memory, the SRAM memory must be initialized to avoid ECC errors and this can be done by the core or by the DMA as well. If the initialization is omitted, any read or write to the SRAM memory generates an uncorrectable ECC error event.

5.1 Read

Read events can be configured to complete with a zero wait state or one wait state for any data size. The PRAM controller register Flow Through Disable field, PRCRx[FT-DIS], inserts a wait state on read events prior to returning the data to the system bus. Insertions of wait states should be considered when the system frequency is greater than 120 MHz. This wait state does not affect write events. For more information about wait states, see the Gasket configurations in the 'Clocking' Chapter of the *MCX E31x Reference Manual*.

5.2 Write

Write operations can be in 64 bits or less. When an aligned 64-bit write is performed, the write operation is executed in a single phase cycle with a zero wait state. When a write less than 64 bits or unaligned write is performed, a Read-Modify-Write (RMW) action is executed to perform the write and recalculate the new ECC code. The RMW process inserts some cycles to the write process, so aligned 64-bit writes offer better performance than unaligned or < 64-bit writes to the SRAM memory.

The following sequence explains the RMW action:

1. The PRAMC performs a SEC/DED in the corresponding read data
2. The write data is merged with the previous read data and only bits of the write data are changed
3. A new ECC code is generated according to the new 64 bits
4. The new double word and ECC is written to RAM

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6 SW recommendations and conclusions

The correct use of different memories available in the MCX E31x Product Family can improve application performance. Users must evaluate which functions and application data to be stored in the different memories to achieve the best performance.

The three important recommendations for achieving good application performance are as follows:

- Deterministic tasks should be placed inside the I-TCM and D-TCM because cores can avoid significant access time to other memories.
- Enabling caches provides a great advantage for the applications because it fetches code and data that cores need quickly. Caches can be enabled and disabled in certain locations of the code to have a better control of what code or data must be fetched. It is important to note that the cache must be invalidated before fetching new code or data. Unfortunately, the cache size is small, however, you can use TCM to support the lack of cache space.
- The Standby SRAM is another advantage that can be explored in different applications because after the application wakes up from Standby mode the data stored in Standby SRAM can be used without any other operation. A good example is sending the stored data when an external communication wakes up the MCU from Standby mode.

7 Acronyms

Table 4. Acronyms

Term	Definition
CAN	Controller Area Network
DED	Double Error Detection
ECC	Error Correcting Code
EMAC	Ethernet Media Access Controller
SEC	Single Error Correction
TCM	Tightly Coupled Memory

8 References

Table 5 lists the references used in this document.

Table 5. References

Document	Link
MCXE31x Reference Manual	MCXE31XRM
MCXE315/316/317/31B Data Sheet	MCXEP172M160FB0

9 Revision history

Table 6 summarizes the revisions to this document.

Table 6. Revision history

Document ID	Release date	Description
AN14901 Rev.1.0	15 December 2025	Initial public release

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