AN14879

FS6500 and FS4500 software quick start guide

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Document information

Information	Content
Keywords	FS4500, FS6500, safety, SBC, software, ASIL B, ASIL D
Abstract	This application note is meant to be used as a launching point for software engineers, as a complement or a substitute for NXP’s software drivers.

1 Introduction

This application note is meant for software engineers who use the FS6500 and FS4500 series of devices.

This document gives guidelines on the implementation of the serial peripheral interface (SPI) communication protocol between the MCU and the SBC, illustrates the initialization procedure of the FS6500 and FS4500 series of devices, watchdog refresh, and fail-safe pin releases to help software engineers quickly start with development.

1.1 Device introduction

The FS6500 and FS4500 SMARTMOS devices are a multi-output, power supply, integrated circuit (IC), including controller area network (CAN) flexible data (FD) and/or local interconnect network (LIN) transceivers, dedicated to the automotive market. The FS6500 and FS4500 include configurable fail-safe/fail-silent safety behavior and features, with two fail-safe outputs, becoming a full part of a safety-oriented system partitioning. There are ASIL B and ASIL D parts to fit different system requirements.

1.2 Reference documents

Reference documents and various materials are available on the FS6500 and FS4500 series devices webpage and NXP SBC/PMIC - real-time drivers site. The webpage provides more detailed information about specific topics:

FS4500-FS6500 data sheet: Information, such as features, functional description, parametric description, register mapping.

FS4500-FS6500 hardware design guideline application note (AN5238): Information, such as application schematics, bill of materials, placement and layout guidelines, application validation data including ISO/non-ISO pulses, electromagnetic compatibility (EMC).

BSPs and device drivers: There are demo drivers and examples with MPC574xP-MC33FS65xx/MC33FS45xx and Embedded Software Driver.

FS6500 and FS4500 SBC Autosar 4.4 version 0.8.0: AUTOSAR and ISO 26262-compliant basic start-up drivers for low-level interfaces, software driver package (FS4500 and FS6500 series devices share the same driver), detailing supported features, such as:

- SBC_FS65 CDD: Complex driver for the device.
- WDG_FS65: Watchdog function services.
- CANTRCV_FS65: CAN PHY driver and functions.
- LINTRCV_FS65: LIN PHY driver and functions.

2 SPI protocol and configurations

Shown in Figure 1, the device uses a 16-bit SPI with the following register bits definitions and arrangements:

- MOSI Bit 15: R/W: 0 - Read, 1 - Write
- MOSI Bit 14: M/FS: 0 - Main, 1 - Fail-safe
- MOSI Bit 9~13: Register address
- MOSI Bit 8: Parity bit, 0 - Number of 1 (bit 15:9 and bit 7:0) is odd. 1 - Number of 1 (bit 15:9 and bit 7:0) is even.
- MOSI Bit 7~0: in Write mode. Must be set to 00h in Read mode.
- MISO Bit 15~8: Device status
- MISO Bit 7~0: Extended device status. Register control bits or device flags.

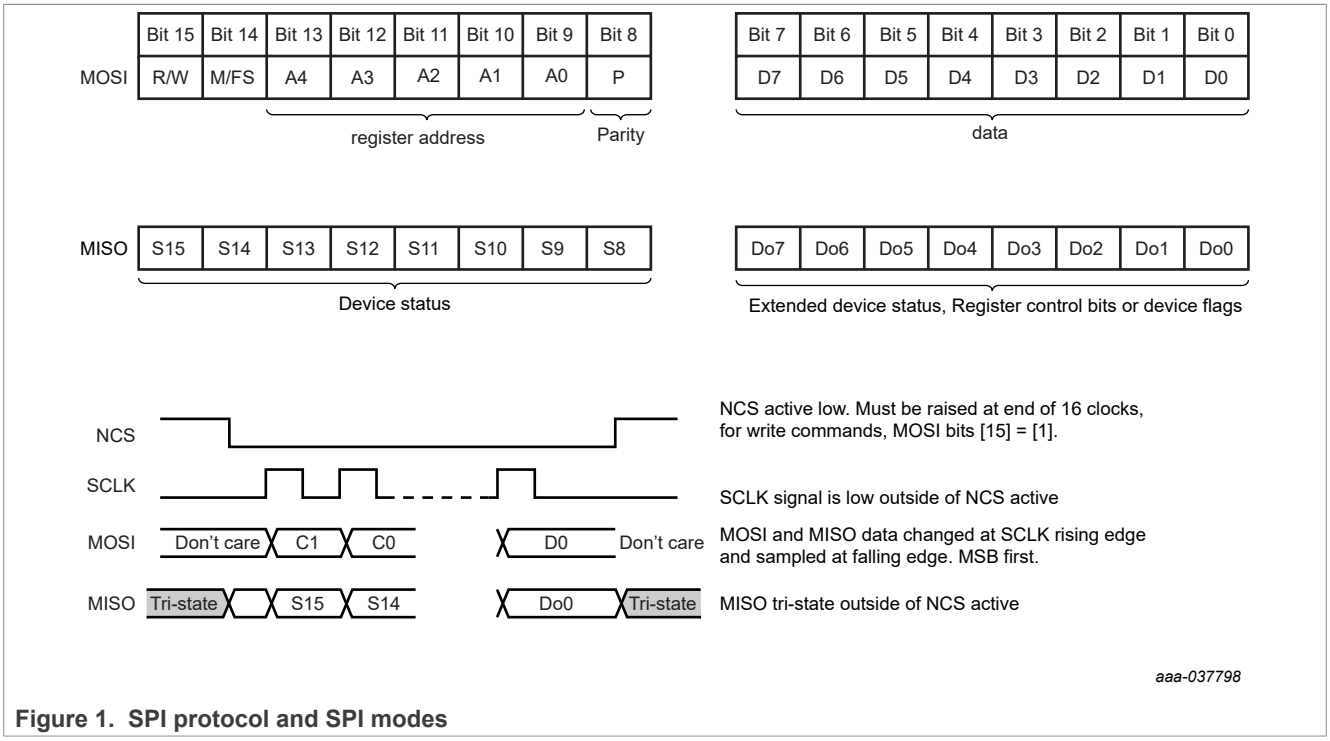

Figure 1. SPI protocol and SPI modes

When configuring the SPI protocol in the MCU driver or in the configuration tool, configure it as:

- 16-bit SPI
- NCS active low
- MSB first
- SPI mode1: CPOL = 0 and CPHA = 1: CLK idle state = low, data sampled on the falling edge and shifted on the rising edge

Detailed main and fail-safe register addresses and bits descriptions can reach to data sheet ref.[1], in Section 13.2, *"Detailed operation"*.

3 FS6500 and FS4500 initialization flow chart and demo commands

3.1 Software flow chart

Figure 2 is a flow chart to describe the initialization process of FS6500 and FS4500 devices. The process can be described as follows:

1. Check LBIST/ABIST1 check result. FSxB cannot be released when either check is a failure.
2. Check power-up reason: When the device is POR(BAT_FAIL = 1) and wakeup is from LPOFF/DFS, both main and fail-safe initial registers are configured and all Diag registers are read once to clear initial states. When the device has entered Main mode and an RSTB event happens, only fail-safe initial registers are configured.
3. ABIST2 is run by MCU SPI commands to check VAUX and FS1B block safety states. If either ABIST2 fails, FSxB cannot be released.
4. Seven continuous good watchdog refreshes are needed to clear a fault error counter value, as it is 1 by default when device goes through power-on reset (POR) or wakes up from LPOFF.
5. Configure non-initial registers.
6. Release FSxB with required commands.

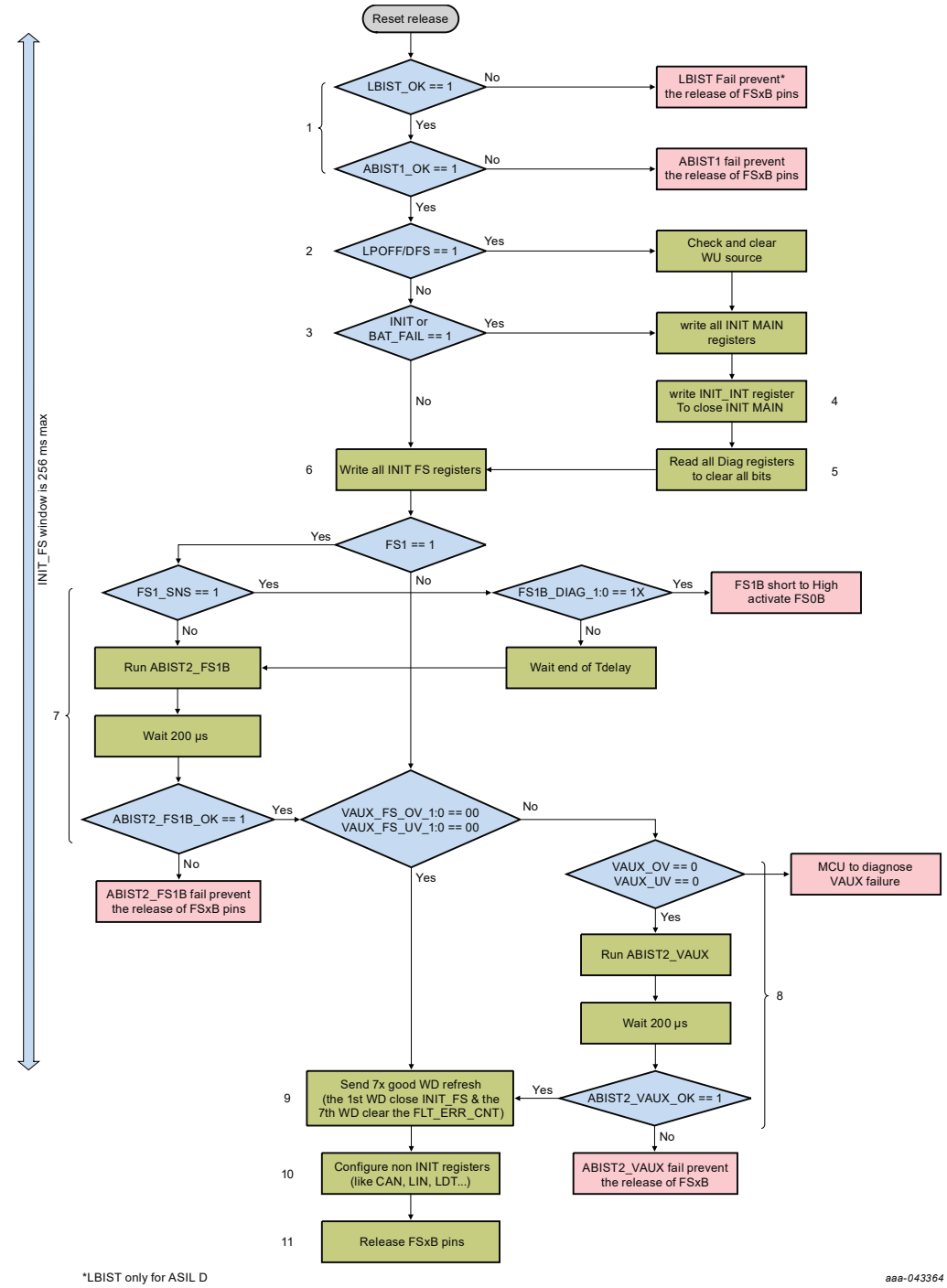

Figure 2. Initialization flow chart

3.2 SPI commands of initialization

Startup SPI sequence example SPI commands based on FS6500 and FS4500 flow chart. A SPI command can be a quick-check command to quick start or issue debug.

Table 1. Startup SPI sequence

		Register	Read	Write	Comment
1	Check BIST	BIST	0x4400	—	Check LBIST_OK and ABIST1_OK bits[1]
2	Check WU source	WU_SOURCE	0x1200	—	Check wake-up sources if wake-up from LPOFF
3	Check POR	INIT_VREG	0x0200	—	Check BAT_FAIL bit
4	INIT_MAIN	INIT_VREG	—	0x8210	Activate Vcan monitoring Vaux tracker disable
		INIT_WU1	—	0x8440	Default value IO_0 wake-up on rising edge or high-level enable
		INIT_WU2	—	0x8600	Default value
		INIT_INH_INT	—	0x8A00	Default value
		INIT_INT	—	0x8900	Default value
5	Read Diag registers	DIAG_VPRE	0x1800	—	Clear VPRE_UV after POR or wake-up
		DIAG_VCORE	0x1A00	—	Clear VCORE_FB_UV after POR or wake-up
		DIAG_VCCA	0x1C00	—	Clear VCCA_UV after POR or wake-up
		DIAG_VAUX	0x1E00	—	Clear VAUX_UV after POR or wake-up
		DIAG_VSUP_VCAN	0x2000	—	Clear VSNS_UV and VSUP_UV_7 after POR Clear VCAN_UV after wake-up
6	INIT_FS	INIT_FS1B_Timing	—	0xC265	Default value
		INIT_SUPERVISOR	—	0xC70C	Default value
		INIT_FAULT	—	0xC80C	FLT_ERR_CNT = 6, FS1B has no impact on CAN
		INIT_FSSM	—	0xCB0C	IO_2:3 and IO_4:5 are not safety critical
		INIT_SF_IMPACT	—	0xCD18	Default value FS1B Tdelay. Reset only at WD_CNT_ERR final value
		INIT_WD_CNT	—	0xD90C	Default value WD_CNT_ERR = WD_CNT_RFR = 6
		INIT_VCORE_UVOV_IMPACT	—	0xE3E7	Default value VCORE_FB_OV impact on RSTB and FS0B, VCORE_FB_UV impact on FS0B only
		INIT_VCCA_UVOV_IMPACT	—	0xE5E7	Default value VCCA_OV impact on RSTB and FS0B, VCCA_UV impact on FS0B only
		INIT_VAUX_UVOV_IMPACT	—	0xE6E7	Default value VAUX_OV impact on RSTB and FS0B, VAUX_UV impact on FS0B only
7	ABIST FS1B	Device_ID_FS	0x6800	—	Check FS1 bit
		RELEASE_FSxB	0x5400	—	Check FS1B_SNS bit
		BIST	—	0xC44D	Start FS1B ABIST
		BIST	0x4400	—	Check FS1B ABIST result
8	ABIST VAUX	BIST	—	0xC424	Start VAUX ABIST[2]
		BIST	0x4400	—	Check VAUX ABIST result
9	7x good WD refresh	WD_LFSR	0x5000	—	Read LFSR
		WD_ANSWER	—	0xD34D	Watchdog answer to be calculated[3]
		WD_LFSR	0x5000	—	Read LFSR
		WD_ANSWER	—	0xD29B	Watchdog answer to be calculated[3]

Table 1. Startup SPI sequence*...continued*

		Register	Read	Write	Comment
		WD_LFSR	0x5000	—	Read LFSR
		WD_ANSWER	—	0xD237	Watchdog answer to be calculated[3]
		WD_LFSR	0x5000	—	Read LFSR
		WD_ANSWER	—	0xD26E	Watchdog answer to be calculated[3]
		WD_LFSR	0x5000	—	Read LFSR
		WD_ANSWER	—	0xD2DC	Watchdog answer to be calculated[3]
		WD_LFSR	0x5000	—	Read LFSR
		WD_ANSWER	—	0xD2B9	Watchdog answer to be calculated[3]
		WD_LFSR	0x5000	—	Read LFSR
		WD_ANSWER	—	0xD372	Watchdog answer to be calculated[3]
10	CAN_LIN_MODE	CAN_LIN_MODE	—	0xB0C0	CAN in normal operation mode
11	RELEASE FSxB	SF_OUTPUT_ REQUEST	—	0xD60C	Close S1 switch between VPRE and VPU_FS[4]
		WD_LFSR	0x5000	—	Read LFSR
		RELEASE_FSxB	—	0xD4A7	Release both FS0B and FS1B at the same time RELEASE_FSxB_4:0 to be calculated

[1] LBIST for ASIL D only.
[2] ABIST on FS1B and VAUX can be launched simultaneously with SPI command 0xC465. The wait time remains 200 µs for both ABIST.
[3] For ASIL B version, only write commands in WD_ANSWER register are needed.
[4] When FS1B is used, the switch S1 can be closed earlier, just after ABIST2 on FS1B, to allow the charge of Cpd while the fault error counter is cleared, reducing the application starting time.

4 Watchdog refresh procedure

A windowed watchdog is implemented in the FS6500 and FS4500, and is based on the question/answer principle (challenger). The watchdog must be continuously triggered by the MCU in the open watchdog window, otherwise an error is generated. The Fail-Safe state machine manages error handling and watchdog operations.

The first good watchdog refresh closes the initialization phase (INIT_FS). As soon as the initialization phase is closed, the watchdog monitors the software failures from the MCU by doing a periodic handshake with the FS6500 and FS4500 through the SPI communication protocol. The watchdog must be continuously triggered by the MCU in the open watchdog window, otherwise an error is generated. The Fail-Safe state machine manages error handling and watchdog operations. The MCU must refresh the watchdog periodically in the middle of the open window by writing the right watchdog answer in the WD_ANSWER register.

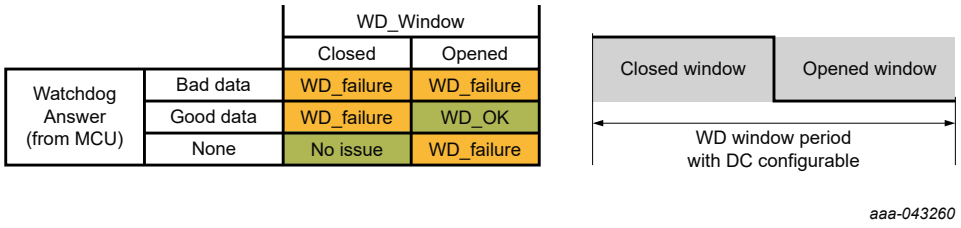

Figure 3. Watchdog refresh window

For FS6500 and FS4500 ASIL B version, the watchdog is simple and refreshed by the MCU using any key. The only requirement is the watchdog refresh time must in the second half (open window) of the whole watchdog window. It is suggested to make the watchdog refresh at 3/4 of the watchdog window.

For FS6500 and FS4500 ASIL D version, the watchdog is a challenger watchdog that must be refreshed with a key calculated from the seed value, which can be read in the WD_LFSR register. (The seed can also be written by the MCU during INIT_FS). At the INIT_FS phase, the MCU must read the seed value before starting in order to calculate the watchdog answer using the formula shown in Figure 4. It is suggested to make the watchdog refresh at 3/4 of the watchdog window.

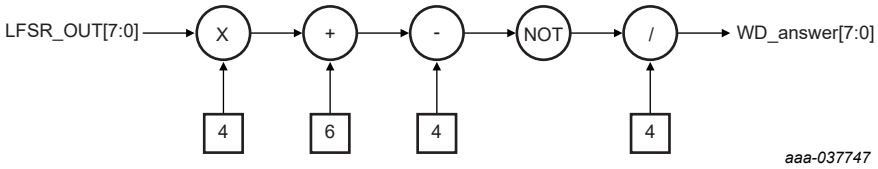

Figure 4. Watchdog calculation formula

5 Release FSxB calculation procedure

1. ABIST2_VAUX_OK = 1, except if VAUX_FS_OV_1:0 = VAUX_FS_UV_1:0 = 00
2. ABIST2_FS1B_OK = 1, if part number with FS1B
3. Close S1 switch between VPRE and VPU_FS if FS1B is pulled up to VPU_FS
4. Fault error counter must be at 0; decrease it with N consecutive good WD refreshes with N = FLT_ERR_2:0 x (WD_RFR_2:0 + 1)
5. Read LSFR data via the SPI
6. Invert all bits of LFSR and swap MSB and LSB bits; the new byte is used to fill in the RELEASE_FSxB register as described in Table 2:

Table 2. RELEASE_FSxB register

	WD_LFSR_7:0	b7	b6	b5	b4	b3	b2	b1	b0
Release FS0B	Release_FSxB_7:0	0	1	1	$\overline{b0}$	$\overline{b1}$	$\overline{b2}$	$\overline{b3}$	$\overline{b4}$
Release FS1B	Release_FSxB_7:0	1	1	0	$\overline{b3}$	$\overline{b4}$	$\overline{b5}$	$\overline{b6}$	$\overline{b7}$
Release FS0B and FS1B	Release_FSxB_7:0	1	0	1	$\overline{b0}$	$\overline{b1}$	$\overline{b2}$	$\overline{b6}$	$\overline{b7}$

Note: *It is recommended to release FS0B in Application mode rather than Boot Loader mode.*

The RELEASE_FSxB write command must be done after the WD_LFSR read command within the same WD period, and one time only. If FS0B and FS1B are released sequentially, the procedure must be done a first time for FS0B, and a second time for FS1B.

6 References

[1] FS6500-FS4500-ASILD Safety power system basis chip with CAN FD and LIN transceivers, data sheet
[2] AN5238 FS6500 and FS4500 safe system basis chip hardware design and product guidelines, application note
[3] FS45FS65 software drivers at NXP website: https://www.nxp.com/products/FS4500 , https://www.nxp.com/products/FS6500
[4] FS45FS65 AUTOSAR Driver website: https://nxp.flexnetoperations.com/control/frse/product?entitlementId=672573417&lineNum=1&authContactId=113165297&authPartyId=120061187

7 Revision history

Table 3. Revision history

Document ID	Release date	Description
AN14879 v.1.0	17 December 2025	Initial version

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