AN14860

Using Segment Liquid Crystal Displays (SLCD) controller on MCX A series

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Document information

Information	Content
Keywords	AN14860, SLCD, MCX A366, FRDM-MCXA366, MCX A
Abstract	This document describes the usage of the on-chip SLCD controller on MCX A366 and tested on FRDM-MCXA366 board.

1 Introduction

We can find customized Segment Liquid Crystal Displays (SLCD) technologies everywhere. For example:

- In the products that measure the PH level of swimming pools.
- In the monitors that are used to measure specific gases in a mine.
- In the thermometers that are used to see whether a child is running a fever.

SLCD is one of the oldest display technologies. It is still one of the most popular technologies, due to the lowest price and power consumption.

Segment LCD displays, also called static displays or glass-only displays, consist of two pieces of Indium Tin Oxide (ITO) glass with a twisted nematic fluid sandwiched in between. A static display is a segment display with one pin for each segment. A segment is any line, dot, or symbol that can be turned on and off independently.

Some products from the NXP MCX A series integrate an SLCD controller module. For details, see the NXP website.

The SLCD module has up to 48 pins for SLCD control, which can generate up to four back planes, such as 4 × 44 and 2 × 46. This document describes the usage of the on-chip SLCD controller on MCX A366 and tested on FRDM-MCXA366 board.

2 LCD basics

The most common LCD is called as Twisted Nematic (TN) display, which is the type of LCD used in this application note.

2.1 Structure and display principle

The main structure of the LCD screen consists of five layers:

- Top polarizer
- Top electrode
- Liquid crystal molecules
- Bottom electrode
- Bottom polarizer

In TN displays, the polarizers and alignment layers are orientated perpendicular to each other, as shown in Figure 1. There are two situations when LCD displays:

- OFF (invisible): when no voltage is applied to the electrodes, the light entering the display from the top is polarized by the top polarizer and, as it travels through the liquid crystals, its polarization rotates with the molecules. When it emerges, its polarization has been changed by 90 degrees and it passes through the bottom polarizer. See the left side of Figure 1. Since the light passes through the LCD, nothing is displayed on the LCD.
- ON (visible): when the alternating voltage is applied to the electrodes, most molecules arrange vertically. In this case, the polarization of the light passing through the liquid crystals remains unchanged and the light beam is blocked by the bottom polarizer. See the right side of Figure 1. Since the light is blocked, the shape filled by the liquid crystal molecules is displayed.

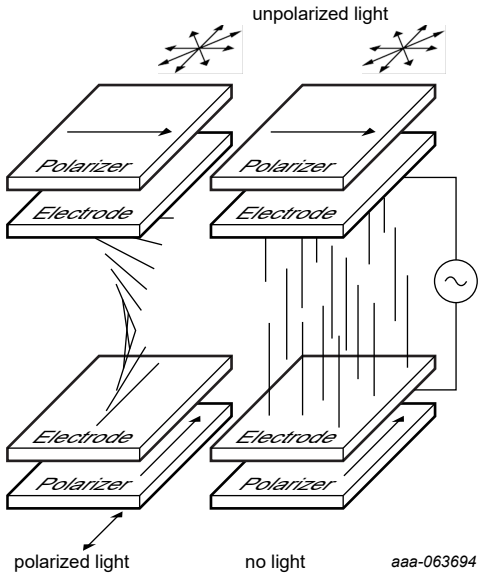

Figure 1. Principle of TN LCD operation

Note: *The voltage waveforms applied to the LCD electrodes must have no DC component. If DC voltage exists across the LCD cell, any impurity ions present migrate toward the electrodes, under the action of the electric field, and may become embedded at the cell surfaces. Therefore, on removal of the stimulating voltage, an electric field across the cell may persist, due to the captured charges, and may hinder cell switching.*

2.2 Polarizer type

According to the type of bottom polarizer, LCD can be divided into three types:

- Reflective
  - Using ambient light as the light source, and the bottom polarizer can reflect light. This type of LCD is often used in low-power scenarios, such as electronic calculator.
- Transmissive
  - Using backlight as the light source, and the bottom polarizer is light-transmissive. This type of LCD is often used in situations where high-brightness display is required, such as computer monitors.
- Transflective
  - Both ambient light source and backlight source are supported. When external light is sufficient, the LCD operates as a reflective type, and when external light is insufficient, it can be used as a transmissive type.

The type of LCD used in this application note is reflective.

2.3 Transmittance characteristics

To obtain better display effects, there are requirements for the RMS value of the applied voltage. Figure 2 shows an example of the TN LCD cell optical characteristics. The goal of the drive scheme is to keep the RMS voltage on invisible segments ($V_{OFF(RMS)}$) below the threshold voltage (V_T) and the RMS voltage on the visible segments ($V_{ON(RMS)}$) above the saturation voltage (V_S).

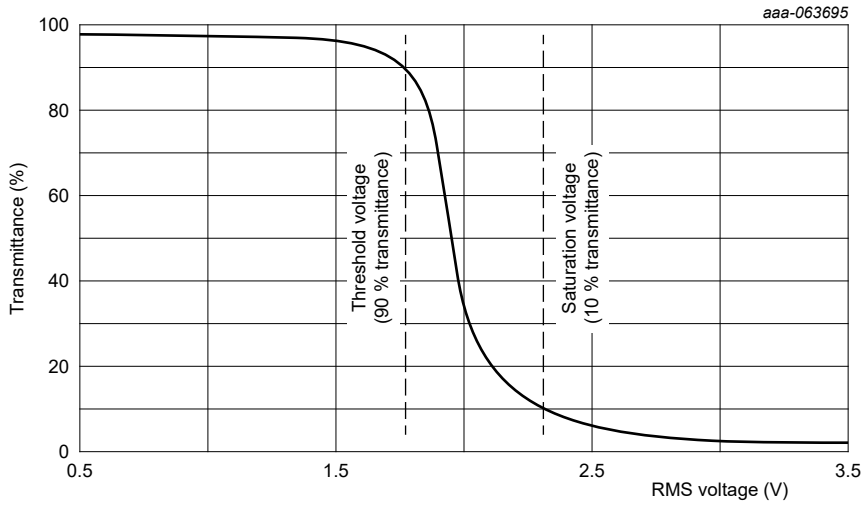

Figure 2. Example of TN LCD cell transmittance characteristics

2.4 Voltage waveforms for driving LCD

Like a keyboard with rows and columns, the LCD is electrically connected in two ports:

- Front Plane (FP)
- Back Plane (BP)

In terms of the principle of the driving scheme, there are two basic types of LCD:

- **Statically driven LCD**
  There is only one back plane, and the driving voltage is directly loaded between the front and back planes.
- **Dynamically driven LCD**
  There are more back planes, and more segments can be effectively displayed by scanning the back plane. When the scanning speed is fast, due to the persistence of vision, it looks like they are displayed together.

The process of refreshing an LCD with **n** back planes and **m** front planes is similar to the keyboard operation. The driver selects one particular back plane BPx (corresponding to a column on a keyboard) and drives the appropriate voltage levels (> V_S) to all front planes FP1 to FPm (corresponding to keyboard rows). The remaining back planes (BP1 to BPx-1, BPx+1 to BPn) are driven to a non-selected voltage level (< V_T). This process is then repeated for all back plane electrodes of the display.

Note: *The LCD cells must be driven with a pure AC voltage, which is resolved by inverting the voltages in every other refresh cycle.*

Below are the terms to describe the properties of the waveforms:

- **Duty**
  The ratio of a back plane scanning time to the period is called as the duty cycle (1/n), n is equal to the number of back planes.
- **Bias**
  The voltage across the LCD cell during the inactive phases is expressed as a fraction of the supply voltage of the driving device and is called as a bias. The number of discrete voltage levels used by the driver is normally equal to b+1. LCD manufacturers typically use the reciprocal of **b** and call it the bias ratio (1/b).

The duty and bias parameters are properties of the driving waveforms. Each type of LCD display has its own optimal waveform parameters associated with it, but it does not mean that waveforms with different parameters fail to work. The subject of the suitability of different waveforms for driving different types of LCDs is discussed in Section 2.5.

2.5 Voltages on LCD Cells Created by Different Drive

As described in Section 2.3, the apparent darkness of a segment on the display depends on the voltage across the LCD cell. To establish the optical effect of an arbitrary voltage waveform, we must calculate its RMS voltage:

$$V_{RMS} = \sqrt{\int_0^T V^2 dt} \tag{1}$$

The voltages across the LCD cells are constant during each phase. The equation can, therefore, be simplified to:

$$V_{RMS} = \sqrt{\frac{\sum_{i=0}^{n-1} V_{Phase}^2(i)}{n}} \tag{2}$$

As mentioned in Section 2.4, the voltage across the LCD cell in the phases in which the corresponding back plane electrode is not selected is always the same (the “inactive” voltage level). This simplifies the equation even further.

$$V_{RMS} = \sqrt{\frac{V_{SelPh}^2 + (n-1) \times V_{nonSelPh}^2}{n}} \tag{3}$$

Equation 3 is a general equation that can be used for any waveforms that keep the voltages across the cells constant in the non-selected phases.

A simple algorithm exists for creating waveforms with any duty and bias ratios. The algorithm is outlined in a pseudo-C programming language in below. The voltage levels used by the algorithm range from 0 (corresponding to the lowest voltage) up to VDD (corresponding to the highest voltage), and 1/b represents the bias ratio (see Section 2.4). The interesting property of this algorithm is that the waveforms use only six voltage levels even for bias factors above five. The algorithm does not create any link between the duty factor n and the bias factor b. This means that it is possible to create waveforms with 1/4 duty ratio and only 1/2 bias ratio. On the other hand, it is also possible to drive an LCD with only two backplane electrodes (1/2 duty ratio) with waveforms that use many voltage levels (such as 1/5 bias ratio).

```
 /* Even refresh cycle */
for (phase=0;phase<n;phase++)
{
  Drive electrode BPphase to voltage level 0
  Drive all other BP electrodes to voltage level VDD*((b-1)/b)
  Drive FP electrodes of visible segments to voltage level VDD
  Drive FP electrodes of invisible segments to voltage level VDD*((b-2)/b)
}

/* Odd refresh cycle */
for (phase=0;phase<n;phase++)
{
  Drive electrode BPphase to voltage level VDD
  Drive all other BP electrodes to voltage level VDD*(1/b)
  Drive FP electrodes of visible segments to voltage level 0
  Drive FP electrodes of invisible segments to voltage level VDD*(2/b)
}
```

For waveforms generated according to the algorithm above, we can substitute V_{SelPh} = VDD for visible segments, V_{SelPh} = VDD*((b-2)/b) for invisible segments (backplane selected) and $V_{nonSelPh}$ = VDD/b (backplane not selected), where VDD corresponds to the voltage level b in the algorithm description (such as the full supply voltage).

The above substitutions can now be used to derive equations for $V_{ON(RMS)}$ and $V_{OFF(RMS)}$ across cells corresponding to the visible and invisible segments:

$$V_{ON(RMS)} = VDD \times \sqrt{\frac{1+(n-1)\times\left(\frac{1}{b}\right)^2}{n}} \quad (4)$$

$$V_{OFF(RMS)} = VDD \times \sqrt{\frac{\left(\frac{b-2}{b}\right)^2+(n-1)\times\left(\frac{1}{b}\right)^2}{n}} \quad (5)$$

Equation 4 and Equation 5 only apply to waveforms generated according to the algorithm above.

The difference between $V_{ON(RMS)}$ and $V_{OFF(RMS)}$ gets smaller as the number of back plane electrodes n increases (such as the duty ratio gets smaller). Therefore, it becomes increasingly difficult to ensure that $V_{ON(RMS)}$ is greater than the saturation voltage V_S and $V_{OFF(RMS)}$ is lower than the threshold voltage V_T. This is why the basic TN LCDs can be used only down to a certain level of duty ratio (down to 1/32, but the limit depends on the liquid crystal material and the supply voltage available).

To assess whether a particular set of waveforms is suitable for driving a particular SLCD, we can calculate the $V_{ON(RMS)}/V_{OFF(RMS)}$ ratio (discrimination ratios, D) and compare it with the V_S/V_T ratio. If the D is greater than the V_S/V_T ratio, then the band between the voltages generated by the waveforms is greater than the band required by the SLCD, and the waveforms can be used for driving the particular display.

Discrimination is the ratio of $V_{ON(RMS)}$ to $V_{OFF(RMS)}$:

$$D = \frac{V_{ON(RMS)}}{V_{OFF(RMS)}} = \sqrt{\frac{b^2+n-1}{(b-2)^2+n-1}} \quad (6)$$

Calculating the ratio for a few combinations of **n** and **b** reveals the optimum drive waveform configurations for SLCD with different numbers of backplane electrodes **n**. Table 1 summarizes these results (1/n corresponds to duty and 1/b corresponds to bias).

Table 1. Discrimination for different combinations of duty and bias

Duty	Bias 1/2	Bias 1/3	Bias 1/4	Bias 1/5	Bias 1/6
1/2	**2.236**	**2.236**	1.844	1.612	1.475
1/3	1.732	**1.915**	1.732	1.567	1.453
1/4	1.528	**1.732**	1.648	1.528	1.433
1/5	1.414	**1.612**	1.581	1.494	1.414
1/6	1.342	**1.528**	**1.528**	1.464	1.397
1/7	1.291	1.464	**1.483**	1.438	1.382
1/8	1.254	1.414	**1.446**	1.414	1.367

The highest value of the $V_{ON(RMS)}/V_{OFF(RMS)}$ ratio available for a given number of back plane electrodes is highlighted in bold type on each line, as shown in Table 1.

3 SLCD module overview

The SLCD module is designed for low-voltage and low-power operation. SLCD is designed to generate the appropriate waveforms to drive multiplexed numeric, alphanumeric, or custom SLCD panels. SLCD also has several timing and control settings that can be software configured depending on the application's requirements. Timing and control consist of registers and control logic for:

- LCD frame frequency
- Duty cycle selection
- Front plane/back plane selection and enabling
- Blink modes and frequency
- Operation in low-power modes

Below is the block diagram for SCLD:

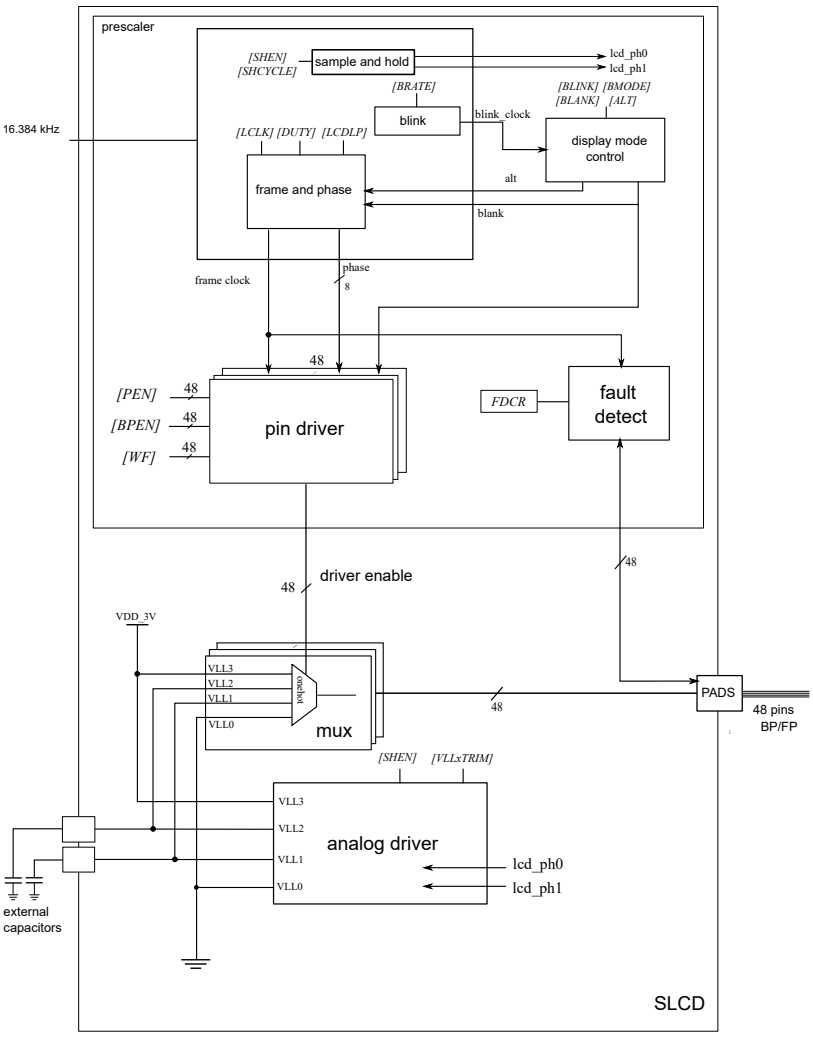

Figure 3. SLCD block diagram

Note: *When SLCD is enabled, a 0.1 µF capacitor must be added to each of the VLL1 and VLL2 connection pins (such as P1_5 and P1_4 for MCX A366) to ensure power supply stability. Do not use these two pins for any other functions when SLCD is enabled.*

3.1 Features

- LCD waveforms functional in Sleep and Deep Sleep modes
- 48 LCD pins with selectable frontplane/backplane configuration to:
  - Generate up to 47 frontplane signals (with one backplane)
  - Generate up to four backplane signals
- Programmable LCD frame frequency
- Programmable blink modes and frequency
  - All segments are blank during the blink period
  - Alternate display for each LCD segment
  - Blink operation in low-power modes
- Configurable sample and hold mode for bias voltage generation
- Programmable standard waveform or low-power waveform
- Programmable LCD duty cycle from static to 1/4
- Waveform storage registers (WF)
- Low power consumption in standby modes
- Backplane reassignment to assist in vertical scrolling on dot-matrix displays
- Software configurable LCD frame frequency interrupt
- Support for segment fault detection

3.2 Functional description

This section provides a complete functional description of SLCD.

Before enabling SLCD by asserting [LCDEN], configure SLCD based on the end application requirements. Out of reset, SLCD is configured with default settings, but these settings are not optimal for every application. SLCD provides several versatile configuration settings and options to support varied implementation requirements, including:

- Frame frequency
- Duty cycle (number of back planes)
- Back plane assignment (where LCD_P[47:0] pins operate as back planes)
- Frame frequency interrupt enable
- Blinking frequency and options
- Power-supply configurations
- Fault detection configuration

3.2.1 Driving modes

The LCD controller driver has four basic modes of operation:

- 1/1 duty (one back plane) (Phase A), static mode
- 1/2 duty (two back planes) (Phase A, B), 1/3 bias (four voltage levels)
- 1/3 duty (three back planes) (Phase A, B, C), 1/3 bias (four voltage levels)
- 1/4 duty (four back planes) (Phase A, B, C, D), 1/3 bias (four voltage levels)

3.2.2 Clock configuration

SLCD is optimized to operate using a 16.384 kHz clock input with only one clock source.

Figure 4 shows the LCD clock tree. The clock tree shows the clock source, and the LCD frame frequency and blink frequency clock source. The LCD blink frequency is discussed in Blink frequency.

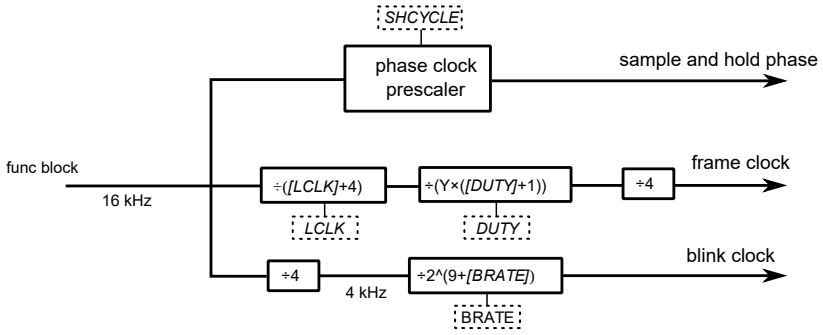

Figure 4. SLCD clock tree

Where:

- [SHCYCLE]: Sample and hold cycle select. It configures a sample and holds phase clock period.
- [LCLK]: LCD clock prescaler, used as a clock divider to generate the SLCD frame frequency.
- [DUTY]: LCD duty select
  - 00b for 1/1 duty cycle (one BP)
  - 01b for 1/2 duty cycle (two BP)
  - 10b for 1/3 duty cycle (three BP)
  - 11b for 1/4 duty cycle (four BP)
- [BRATE]: Blink-rate configuration
  - Write 1 to [BLINK] to enable blinking

3.2.3 Sample and Hold mode

SLCD can be configured to enable sample and hold mode to reduce power consumption of the voltage driver that generates VLL1 and VLL2. By periodically turn on and off the switches (as phases in figure below), voltages are sampled and held for a period, so that the power is saved. To enable a sample and hold the function, set [SHEN]. Register bit [SHCYCLE] is for setting the phase period.

Where:

- [SHCYCLE] = 0b, phase cycles = 64
- [SHCYCLE] = 1b, phase cycles = 128

Figure 5 shows the timing of sample and hold phases.

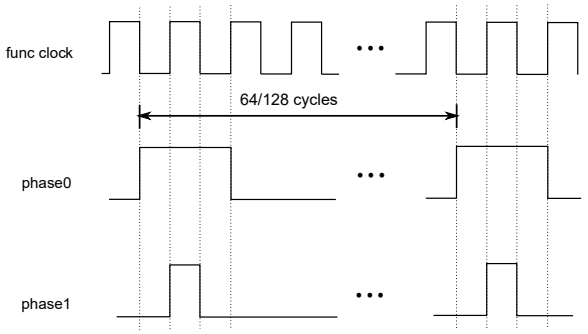

Figure 5. LCD driver analog sample and hold timing

Note: *When the ambient temperature is greater than 105 degrees, it is not recommended to enable this mode because it causes the output of VLL1 to show sawtooth.*

3.2.4 Low power mode operation

There are four low power modes for MCX A series:

- Sleep
- Deep Sleep
- Power Down
- Deep Power Down

For details, see the **Power Management** section in the reference manual.

Table 2 shows the functions of SLCD in different low power modes.

Table 2. SLCD functions in low power modes

Mode	Keep display	Refresh display
Sleep	Yes	Yes
Deep Sleep	Yes	No
Power Down	No	No
Deep Power Down	No	No

Before loading the SLCD waveform, the pre-configuration operations must be completed. In this case, if entering Deep Sleep mode immediately after configuring the SLCD, the waveform is not loaded due to the pre-configuration cutoff (bus clock is gated). A delay must be added before entering Deep Sleep mode in this case, and the delay time can be calculated as below:

$$T_{delay} = T_{func} \times \left(LCLK + 4\right) \times \left(2Y - 1\right) \tag{7}$$

Where:

- T_{func}: Function clock (16 kHz) period
- LCLK: LCD Clock Prescaler
- Y: Related to duty cycle configuration, Y = 16, 8, 5, 4 when duty cycle = 1/1, 1/2, 1/3, 1/4

Note: *Write 1 to [LCDDOZE] and [LCDSTP] to disable the LCD driver in Deep Sleep mode, which is enabled by default.*

3.2.5 SLCD waveform examples

Take the 1/4 duty waveform as an example, and below are the main configuration steps:

1. Write 0b11 to [DUTY]
   - Set the duty cycle to 1/4
2. Write 1 to [PIN_0_EN], [PIN_1_EN], [PIN_2_EN], [PIN_3_EN], [PIN_4_EN], [PIN_5_EN]
   - Enable the related LCD pins
3. Write 1 to [PIN_0_BPEN], [PIN_1_BPEN], [PIN_2_BPEN], [PIN_3_BPEN]
   - Set LCD_P0,1,2,3 as back planes (default is front plane, LCD_P4,5 are front planes)
4. Write 0x01, 0x02, 0x04, and 0x08 to [WF0], [WF1], [WF2] and [WF3] respectively
   - LCD_P0,1,2,3 assigned to Phase A,B,C,D respectively
5. Write 0x05 and 0x0B to [WF4] and [WF5] respectively
   - Set value for front planes
6. Write 0 to [LCDLP]
   - Set standard waveform
7. Write 1 to [LCDEN]
   - Enable LCD waveform

Figure 6 shows the waveform for this example.

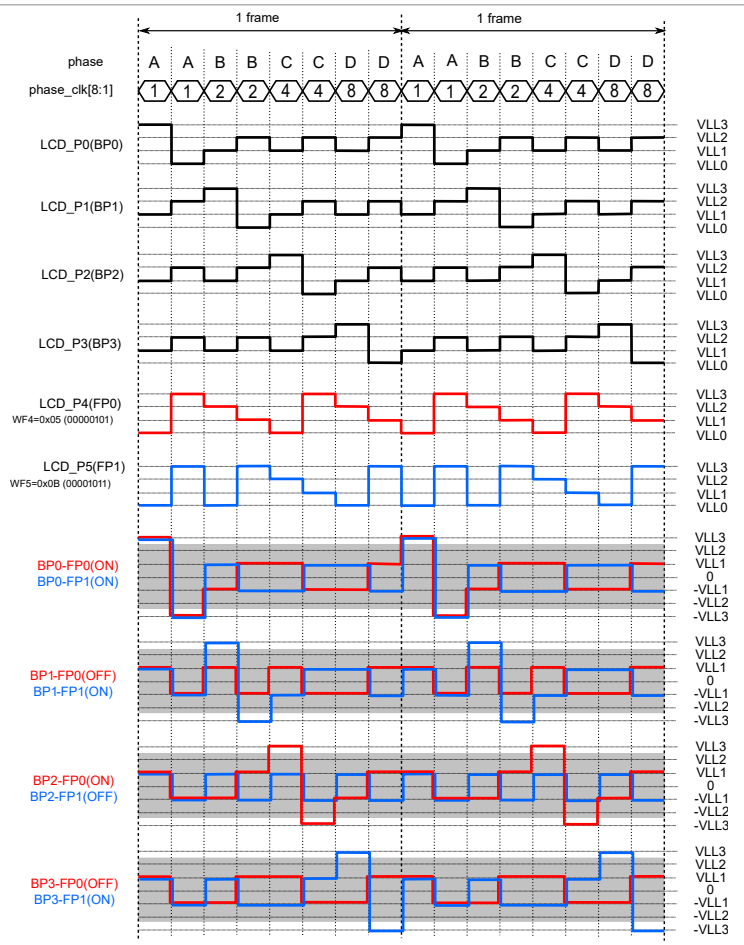

Figure 6. SLCD waveform example

Table 3 shows the results of the set.

Table 3. SLCD display results

FP	BP3	BP2	BP1	BP0
FP0	OFF	ON	OFF	ON
FP1	ON	OFF	ON	ON

When writing 1 to [LCDLP], the low-power waveforms are enabled, and below is the comparison:

- Standard waveforms when [LCDLP] = 0, frame structure: “A-A-B-B-C-C-D-D”, as shown in Figure 6.
  - The waveforms maintain a zero DC component over a period that is only two phases long. Therefore, it is possible to update the segment visibility much more often compared to low-power waveforms. However, this fact is usually of minor importance, as the faster update rate is rarely required.
- Low-power waveforms when [LCDLP] = 1, frame structure: “A-B-C-D-A-B-C-D”
  - The waveforms maintain a zero DC component over the period of two refresh cycles. It is possible to change the visibility of the LCD segments only at the end of every second refresh period. If visibility of segments is altered more often, the DC component of the drive waveforms ceases to be zero and long-term reliability of the LCD could be impacted. However, the lower frequencies contained in this waveform result in lower power consumption, an important parameter especially in battery-powered applications.

4 Test on board

Below are the hardware and software used in this application note:

- Hardware: FRDM-MCXA366
- Software: SDK_25_09_00_FRDM-MCXA366

4.1 Hardware setup

The FDRM-MCA366 board ships with an onboard debugger. Use a USB-C cable to connect to the board via J15 for downloading and debugging.

The SLCD used on FRDM-MCXA366 is 1/4 duty and 1/3 bias. The main information is as shown in Figure 7 and Table 4.

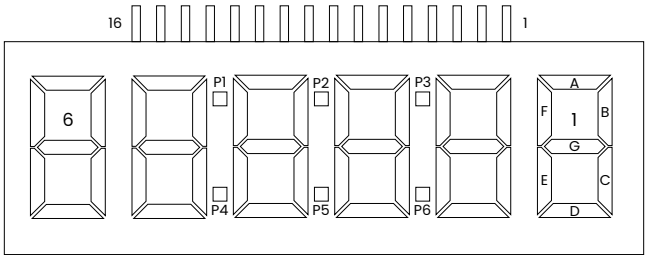

Figure 7. Onboard SCLD display mode

Table 4. Onboard SCLD pin connection

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
COM1	1A	P6	2A	P3	3A	P2	4A	P1	5A	P4	6A	P5	COM1			
COM2	1B	1F	2B	2F	3B	3F	4B	4F	5B	5F	6B	6F		COM2		
COM3	1C	1G	2C	2G	3C	3G	4C	4G	5C	5G	6C	6G			COM3	
COM4	1D	1E	2D	2E	3D	3E	4D	4E	5D	5E	6D	6E				COM4

Where:

- Pin 1 to 12 are front planes.
- Pin 13 to 16 are back planes (COM1 to COM4 correspond to BP0 to BP3).
- Each digit is divided into seven segments: ABCDEFG.
- Six points are assigned to different digits.
- From left to right, they are digits 6 to 1.

The seven-segment display is used to display numbers. It displays the numbers 0 to 9 by displaying different segments, as shown in Figure 8.

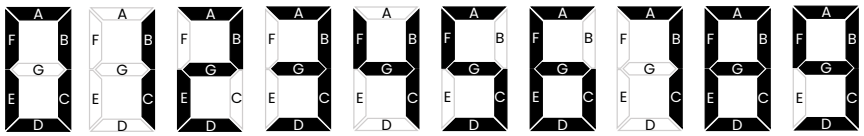

Figure 8. Numbers display

For the correspondence between each segment and each control bit, see Table 4. From low to high, the corresponding segments are ABCDPFGE, among which **P** (point) can be ignored because only the number display is considered here. Table 5 lists the HEX value corresponding to each segment:

Table 5. Segment control table

Segment	A	B	C	D	P	F	G	E
HEX	0x0001	0x0002	0x0004	0x0008	0x0100	0x0200	0x0400	0x0800

By combining the control bits (bitwise AND operation for all enable segments), different numbers can be displayed, as shown in Table 6.

Table 6. Number display table

Number	0	1	2	3	4	5	6	7	8	9
Segment	ABCDEF	BC	ABEDG	ABCDG	BCFG	ACDFG	ACDEFG	ABC	ABCDEFG	ABCDFG
HEX	0x0A0F	0x0006	0x0C0B	0x040F	0x0606	0x060D	0x0E0D	0x0007	0x0E0F	0x060F

Figure 9 and Table 7 show the connections of the MCU and SLCD pins.

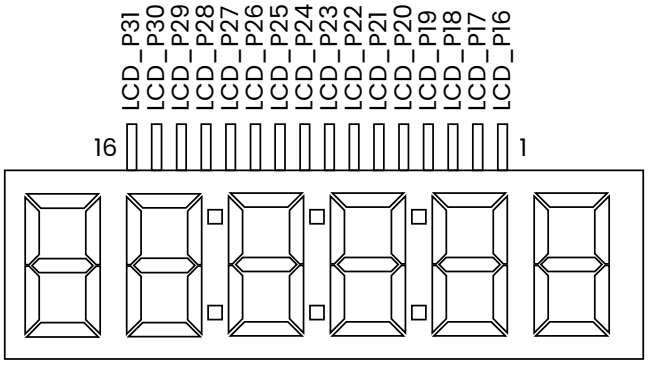

Figure 9. Pin connections

Table 7. Pin connection list

MCU pin	SLCD pin
P0_12 (LCD_P16)	1
P0_13 (LCD_P17)	2

Table 7. Pin connection list*...continued*

MCU pin	SLCD pin
P0_14 (LCD_P18)	3
P0_15 (LCD_P19)	4
P0_16 (LCD_P20)	5
P0_17 (LCD_P21)	6
P0_18 (LCD_P22)	7
P0_19 (LCD_P23)	8
P0_20 (LCD_P24)	9
P0_21 (LCD_P25)	10
P0_22 (LCD_P26)	11
P0_23 (LCD_P27)	12
P0_24 (LCD_P28)	13 (COM1)
P0_25 (LCD_P29)	14 (COM2)
P0_26 (LCD_P30)	15 (COM3)
P0_27 (LCD_P31)	16 (COM4)

4.2 Static display test

Below is the configuration step for showing “123456”:

1. Configure the corresponding pins as LCD functions.
   - P0_12 to P0_27
2. Enable FRO16K as SLCD clock.
3. Unlock clock configuration, enable SLCD peripheral clock, and release from reset.
4. Write 0b11 to [DUTY].
   - Set the duty cycle to ¼.
5. Write 1 to [PIN_16_EN]…[PIN_31_EN].
   - Enable the related LCD pins (set LCD_PEN0 = 0xFFFF0000).
6. Write 1 to [PIN_28_BPEN], [PIN_29_BPEN], [PIN_30_BPEN], [PIN_31_BPEN].
   - Set LCD_P28,29,30,31 as back planes (set LCD_BPEN0 = 0xF0000000).
7. Write 0x01, 0x02, 0x04, and 0x08 to [WF28], [WF29], [WF30], and [WF31] respectively.
   - LCD_P28,29,30,31 assigned to Phase A,B,C,D respectively (set LCD_WF31TO28 = 0x08040201).
8. Write value to [WF16] to [WF27] respectively (see Table 6).
   - Set LCD_WF19TO16 = 0x060D0E0D (display “56”).
   - Set LCD_WF23TO20 = 0x040F0606 (display “34”).
   - Set LCD_WF27TO24 = 0x00060C0B (display “12”).
9. Write 0 to [LCDLP].
   - Set standard waveforms.
10. Write 1 to [LCDEN].
    - Enable LCD waveform.

The core code shown as below (configure the LCD pins first):

```
/*!
 * void SLCD_display_static()
```

```
 * @brief SLCD display “123456”
 * @param NULL
 * @return NULL
 */
void SLCD_display_static()
{
  CLOCK_SetupFRO16KClocking(kCLKE_16K_COREMAIN); // Enable FRO16K for SCLD

  SYSCON -> CLKUNLOCK &= ~SYSCON_CLKUNLOCK_UNLOCK(1U); // Unlock clock configuration

  MRCC0 -> MRCC_GLB_CC1  |= MRCC_MRCC_GLB_CC1_SLCD0(1U); // Enable SLCD0 clock
  MRCC0 -> MRCC_GLB_RST1 |= MRCC_MRCC_GLB_RST1_SLCD0(1U); // Reset  SLCD0

  LCD0 -> GCR |= LCD_GCR_DUTY(3U); // 1/4 Duty cycle

  LCD0 -> PEN[0]  |= 0xFFFF0000; // Enable P31~P16
  LCD0 -> BPEN[0] |= 0xF0000000; // P31~P28 as back plane, P27~P16 as front plane

  LCD0 -> WF[7] = 0x08040201; // WF31~WF28, COM4~COM1 set to phase D~A

  LCD0 -> WF[4] = 0x060D0E0D; // display "56"
  LCD0 -> WF[5] = 0x040F0606; // display "34"
  LCD0 -> WF[6] = 0x00060C0B; // display "12"

  LCD0 -> GCR &= ~LCD_GCR_LCDLP(1U); // LCD driver drives standard waveforms

  LCD0 -> GCR |= LCD_GCR_LCDEN(1U); // LCD Driver Enable
}
```

4.3 Dynamic display test

SLCDs are commonly used in digital clocks, temperature displays, and other applications that require dynamic refresh. In this test, a stopwatch is created using the System Tick Timer (SysTick) and the SLCD module.

Below is the configuration step:

1. SLCD configuration step is similar to that listed in Section 4.2 (step 8 is not needed).
2. Configure the button to control the stopwatch.
   - Configure SW2 as a clear button.
   - Configure SW3 as a start/stop button.
3. Configure the SysTick and interrupt every 10 millisecond.
4. Configure the refresh logic of the SLCD.

For the whole runnable source code project, see AN14860SW.

When running the demo code:

- Press **SW3** to start/stop the stopwatch.
- Press **SW2** to clear the stopwatch.

4.4 SLCD waveform test

As mentioned in Section 3.2.5, there are two different waveform forms:

- Standard waveforms
- Low-power waveforms

To enable the low-power waveforms, write 1 to [LCDLP].

Figure 10 shows a standard waveform (BP0 to BP3) captured by an oscilloscope.

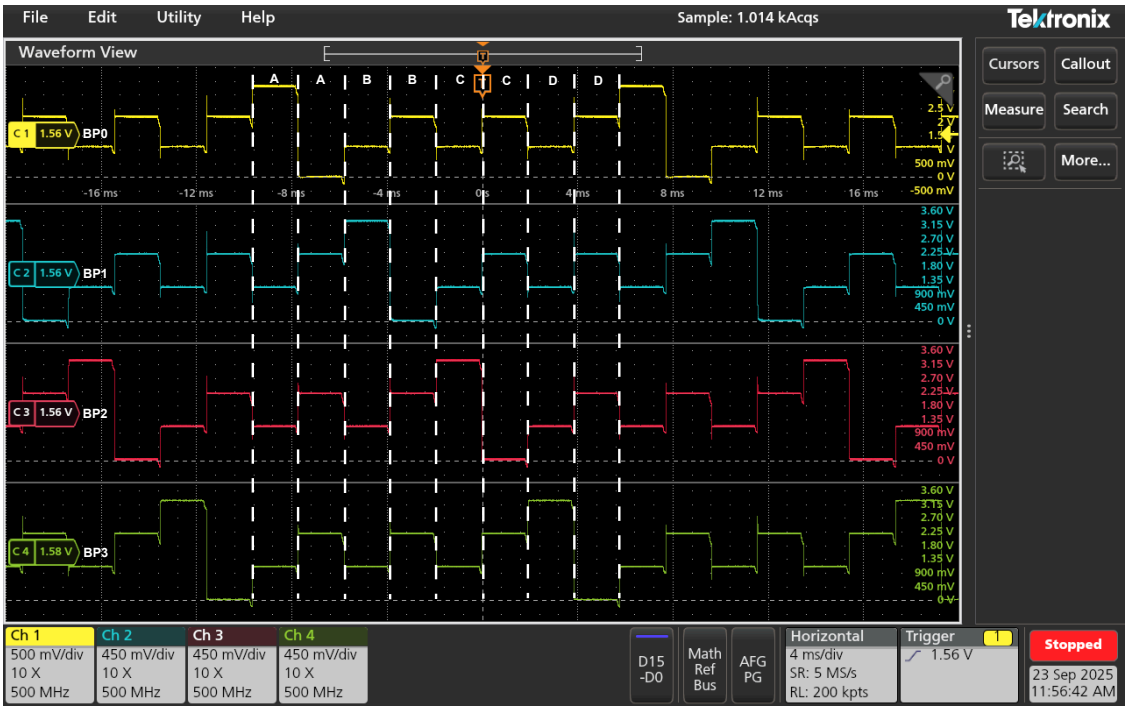

Figure 10. LCD standard waveforms

Figure 11 shows a low-power waveform (BP0 to BP3) captured by an oscilloscope.

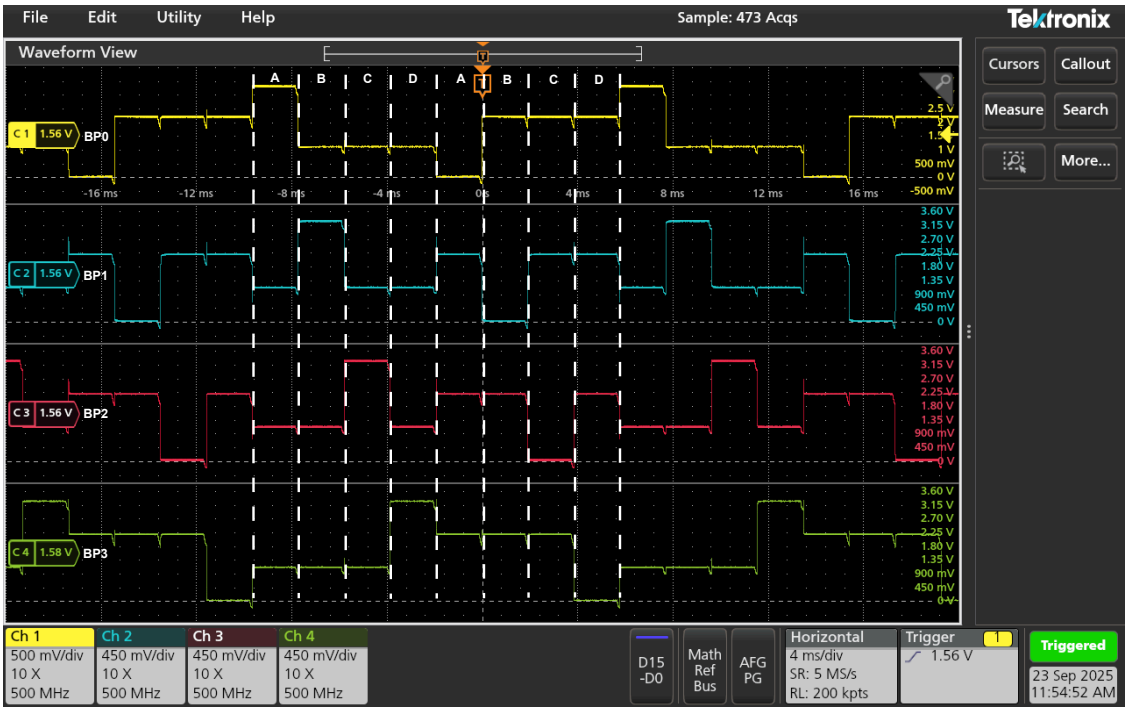

Figure 11. LCD low-power waveforms

5 Conclusion

This application note is for users to make better use of the SLCD module on MCX A series. The document provides the principle of SLCD and describes the basic usage of on-chip SLCD controller on MCX A366 MCU with the example projects based on the FRDM-MCXA366 board.

6 Reference

- MCX A365/366 data sheet
- MCX A365/366 Reference Manual
- *XGATE Library: TN/STN LCD Driver Driving Bare TN and STN LCDs Using GPIO Pins* (document AN3219)
- *Using Segment Liquid Crystal Displays (SLCD) Controller on MCX C444 MCU* (AN14321)

7 Note about the source code in the document

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8 Revision history

Table 8 summarizes the revisions to this document.

Table 8. Revision history

Document ID	Release date	Description
AN14860 v.1.0	08 January 2026	Initial public release

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