AN14709

Power Management Hardware for the KW47

Rev. 2.0 — 10 December 2025 Application note

Document information

Information	Content
Keywords	AN14709, power management, KW47, LDO, DC-DC
Abstract	This application note describes the usage of the different modules dedicated to power management in the KW47 microcontroller. The KW47 integrates a DC-DC buck converter, a couple of low-dropout regulators, and a programmable solid-state switch to turn on/off the KW47 power domains. Also, the KW47 integrates independent power domains for each group of hardware.

1 Introduction

This application note describes the usage of the different modules dedicated to power management in the KW47 microcontroller. The KW47 integrates a DC-DC buck converter, a couple of low-dropout regulators, and a programmable solid-state switch to turn on/off the KW47 power domains. Also, the KW47 integrates independent power domains for each group of hardware. For example, there is a dedicated power domain for the reset hardware, general-purpose input/output (GPIOs), and analog. The dedicated hardware for power management and the option to use different voltages for each power domain give flexibility. This helps to meet most of the application requirements in wireless applications.

2 KW47 dower domains

The KW47 microcontroller has independent power domains, which are grouped as follows:

- VDD_SWITCH: Represents the input voltage for the smart power switch (VBAT). This power domain supplies the voltage to the internal hardware associated with the VBAT.
- VDD_ANA: Drives the analog peripherals on this microcontroller, such as the analog-to-digital converter (ADC) and the VREF regulator.
- VDD_IO_ABC: Drives the voltage on the PTA, PTB, and PTC pins.
- VDD_IO_D/VDD_DCDC: Drives the voltage on the PTD pins, including the reset system. It is also shared with the inputs for the DC-DC Buck converter, and for the LDO_SYS regulator.
- VDD_SYS: Manages the power delivered to some peripherals on this chip. Table 1 shows the list of peripherals, which VDD_SYS domain supplies.
- VDD_CORE: The core-power domain supplies to the main core processor and some peripherals on this chip. This power domain is split into core main, core wake, and core radio domains for an independent power mode selection. The voltage on this power domain is associated with the maximum clocking frequency at which this device can operate. Table 1 shows the list of peripherals, which VDD_CORE domain supplies.
- VDD_RF: The RF power domain provides the voltage that drives the radio analog system in this chip and the 32 MHz-OSC oscillator.
- VDD_PA_2.4G: Drives the voltage for the radio power amplifier. The VDD_PA_2.4G voltage can be provided internally from the VDD_RF power domain.

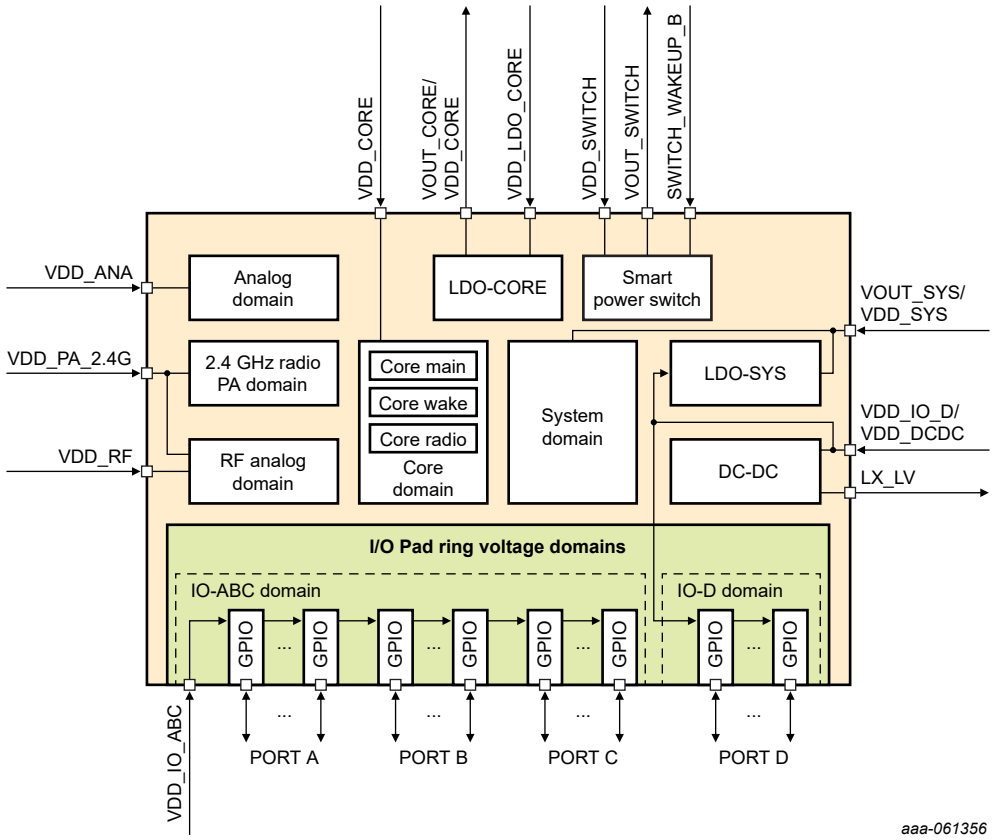

Figure 1. KW47 power domain block diagram

2.1 Peripherals supplied by each power domain

Table 1 shows the KW47 power domains and their associated on-chip peripherals, which these domains supply.

Table 1. Peripheral power domain assignments

Power domain	Voltage supply	Modules associated with the power domain
Analog domain	VDD_ANA and VSS_ANA	ADC0 and VREF0
Core main	VDD_CORE_MAIN (Tied internally to VDD_ CORE pin)	CM33, DSP, FPU, MPU, NVIC, SYSTICK, TZM, DAP, DWT, ITM, TPIU, AXBS0, eDMA0, MSCM, SMSCM, PRBRIGDE2, TRGMUX, MRCC, SFA0, CACHE-CODE, FLASH, ROM-BOOT, CRC0, EdgeLock Secure Enclave, TRDC0, LPIT0, TPM1, FlexCAN0, FlexCAN1, FlexIO0, LPI2C 1, I3C0, LPSPI 1, LPUART 1, GPIOB, GPIOC, SEMA42, PORTB, PORTC, ADC0, VREF0, and TCM- SYS
Core wake	VDD_CORE_WAKE (Tied internally to VDD_ CORE pin)	SWD, CMC0, EWM0, WDOG0, WDOG1, FRO-6M, MRCC, SCG0, TSTMR0, TPM0, LPI2C0, LPUART0, LPSPI0, GPIOA, PORTA, LPCMP0, and LPCMP1
Core radio	VDD_CORE_2.4G (Tied internally to VDD_ CORE pin)	RF-2.4G, NBU, RF-FMU, RF-FRO192M, TPM2, and LPUART2
IO-ABC	VDD_IO_ABC	PORTA, PORTB, PORTC, LPCMP0, and LPCMP1
IO-D	VDD_IO_D	LDO-SYS, DC-DC, and PORTD

Table 1. Peripheral power domain assignments*...continued*

Power domain	Voltage supply	Modules associated with the power domain
Smart power switch	VDD_SWITCH	Power switch, RAM LDO, FRO16K, and power switch controller
System	VDD_SYS	RFMC0, Bluetooth LE LL (from MBU), WUU0, FRO192M, LPTMR0/1, SPC0, OSC-RTC, FRO32K, REGFILE0/1 – RTC, TAMPER, RTC0, GPIOD, and PORTD
RF analog	VDD_RF	OSC-RF and RF-2.4G
2.4 GHz radio PA	VPA_2.4G	RF-PA-2.4G
VDD_DCDC	Direct current to direct current converter – Low voltage	DCDC-LV

The KW47 includes hardware dedicated to power management embedded in the chip. Table 2 shows a brief description of the regulators available on this MCU.

Table 2. On-chip regulator descriptor

On-chip regulator	Voltage supply	Description
DC-DC	VDD_DCDC	The DC-DC can be used to power the LDO-SYS, I/O ring, RF analog, and 2.4 GHz radio power amplifier. It also powers the external components. The user must consider that the total load current expected never exceeds the maximum DC-DC current capacity. The DC-DC current capacity depends on the DC-DC Drive mode.
LDO-CORE	VDD_LDO_CORE	The LDO-CORE can be used to power the VDD_CORE domain. It is not intended to supply external loads.
LDO-SYS	VDD_IO_D	The LDO-SYS can be used to power the VDD_SYS domain. It is not intended to supply external loads.

Table 3 shows the supported voltage options for each on-chip regulator.

Table 3. On-chip regulator voltages

On-chip regulator	Voltage options
DC-DC	1.25 V, 1.35 V, 1.5 V, 1.8 V, and 2.5 V
LDO-CORE	1.05 V, 1.1 V, and 1.15 V
LDO-SYS	1.8 V and 2.5 V[1]

[1] Do not enable the LDO-SYS 2.5 V option while the application is running. This option is intended only to program the eFuses.

2.2 Power domain rates

Table 4 shows the maximum and minimum DC voltage requirements for each power domain in the KW47 MCUs.

Table 4. Power domain rates

Power domain	Voltage supply	Minimum	Maximum	Unit
Core domain	VDD_CORE:			
	• Mid Drive (1.05 V)	1.0	1.1	V
	• Normal Drive (1.1 V)	1.04	1.21	V

Table 4. Power domain rates*...continued*

Power domain	Voltage supply	Minimum	Maximum	Unit
	• Safe-mode (1.15 V)	1.04	1.21	V
System domain	VDD_SYS:			
	• Normal mode	1.71	1.98	V
	• Fuse programming	2.25	2.75	V
IO-ABC domain	VDD_IO_ABC	1.71	3.6	V
IO-D domain	VDD_IO_D	1.86	3.6	V
Smart power switch	VDD_SWITCH	1.9	3.6	V
RF analog domain	VDD_RF	1.175	3.6	V
2.4 GHz radio PA	VPA_2.4G	0.9	2.4	V
Analog domain	VDD_ANA	1.71	3.6	V

3 KW47 power configurations

The KW47 microcontroller has independent power domains, allowing various power configurations. You can implement any power configuration depending on the voltage required on each power domain, according to the application requirement. For more information on DC voltage requirements for each power domain in KW47, see Section 2.2.

The purpose of this section is to show the most common power configurations, advantages, and considerations.

3.1 KW47 low-cost supply configuration

The following is the KW47 low-cost supply mode configuration:

- The KW47 low-cost supply mode disables the DC-DC and directly connects each power domain to a unique power supply.
- This configuration is the lowest-cost hardware implementation due to the small number of external components required.
- However, this configuration does not allow you to have independent voltages on each power domain, and therefore, has the highest power consumption.
- In this configuration, the following is recommended:
  - Disable the DC-DC
  - Clear the SPC -> CNTRL[DCDC_EN] = 0
  - Leave the DCDC_LX pin (DC-DC output pin) floating in the design

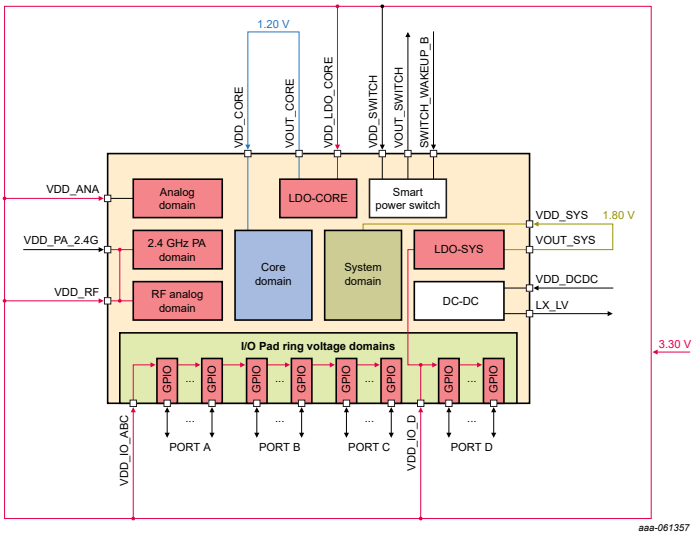

Figure 2. Low-cost schematic

3.2 KW47 power efficient mode configuration

The following is the KW47 DC-DC Buck mode configuration:

- The DC-DC Buck mode configuration provides the best balance in power consumption and cost. As a consequence, this mode is the most-used configuration.
- In DC-DC Buck mode, a single power supply is used to deliver power to many power domains including the DC-DC input.
- The DC-DC output can provide a different configurable voltage for the RF domain and LDO-CORE.
- The DC-DC output is targeted to deliver the voltage needed for the RF power domain to reach up to +10 dBm TX output power.
- It is also possible to decrease the DC-DC output voltage as a power-saving mechanism while the RF domain is idle.
- The DC-DC can be used to feed external circuitry.

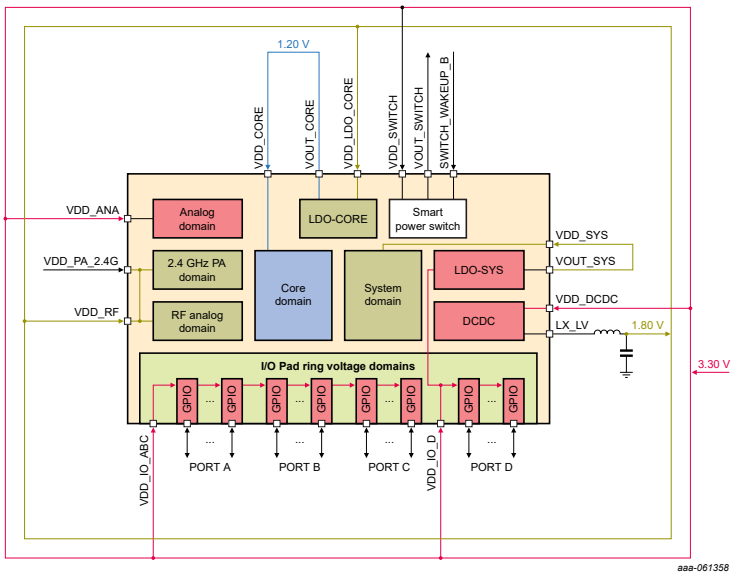

Figure 3. Power efficient schematic

3.3 KW47 DC-DC mode controlled with smart power switch

This section describes the KW47 DC-DC mode controlled with the smart power switch as follows:

- The smart power switch (VBAT) is a low-resistance solid-state switch that works with the power management system to implement the power-saving mechanisms.
- It provides two bandgap timers and an LDO voltage regulator dedicated to supply the retention SRAM while the rest of the MCU remains switched off.
- The smart power switch can be used to turn off all the MCUs or some specific power domains to obtain an optimized power consumption.
- The smart power switch can be used to switch on/off external circuitry with a low-dropout voltage.
- In this mode, the smart power switch domain (VDD_SWITCH) is the only voltage domain required to be powered permanently.
- The software can disable the smart power switch and enable it using any of the VBAT bandgap timers or a falling edge on the SWITCH_WAKEUP_B pin.

Figure 4 shows the configuration with the smart power switch as follows:

- The 3.3 V external power source supplies the power to the smart power switch.
- Its output is connected to the DC-DC, LDO-SYS, VDD_ANA, VDD_IO_D, and VDD_IO_ABC.
- The DC-DC output is connected to the LDO-CORE and VDD_RF.

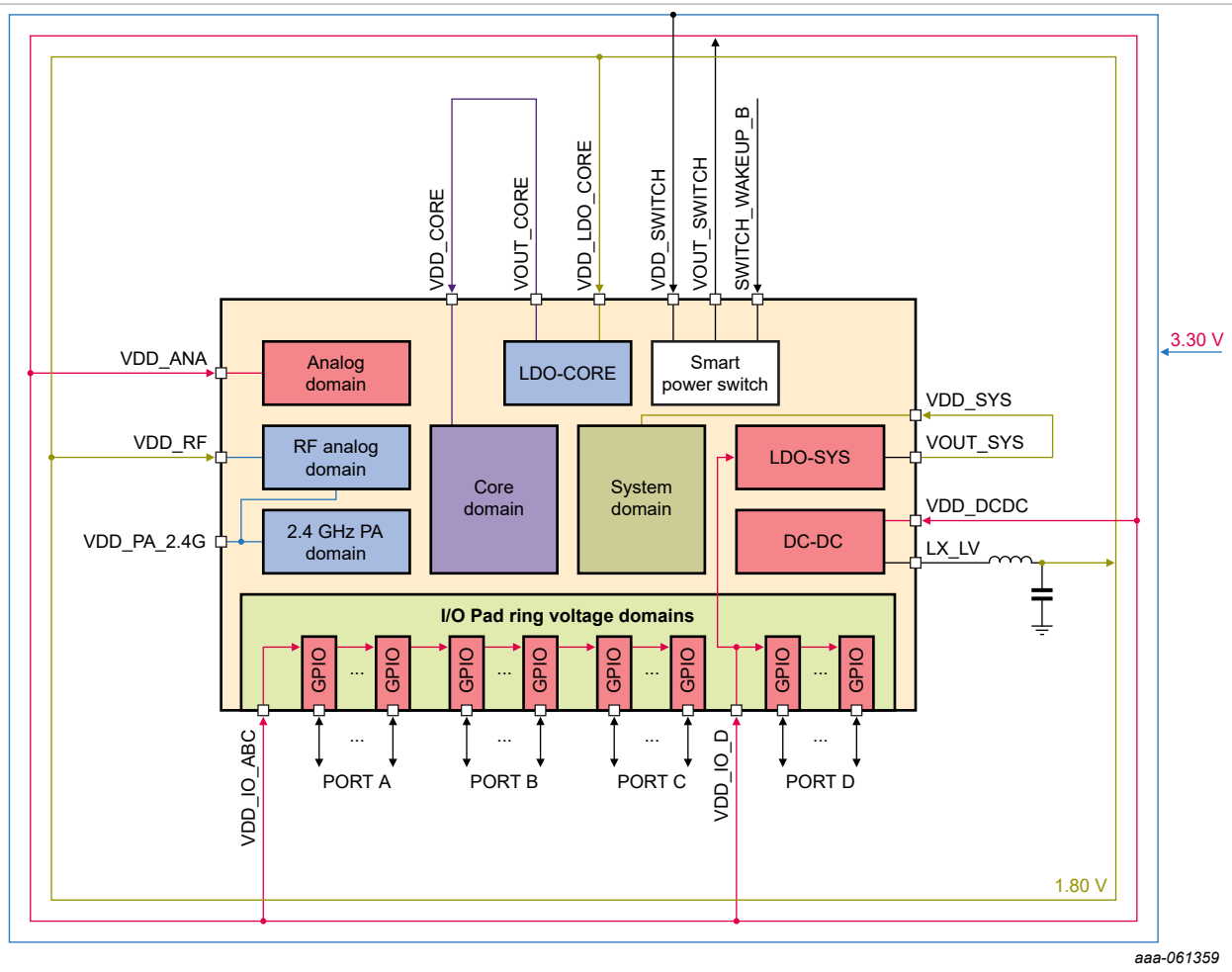

Figure 4. Power all supply

Figure 5 shows the configuration with the smart power switch as follows:

- The 3.3 V external power source supplies the power to the smart power switch and VDD_DCDC/VDD_IO_D.
- Its output is connected to the VDD_ANA and VDD_IO_ABC.
- The DC-DC output is connected to the LDO-CORE and VDD_RF.

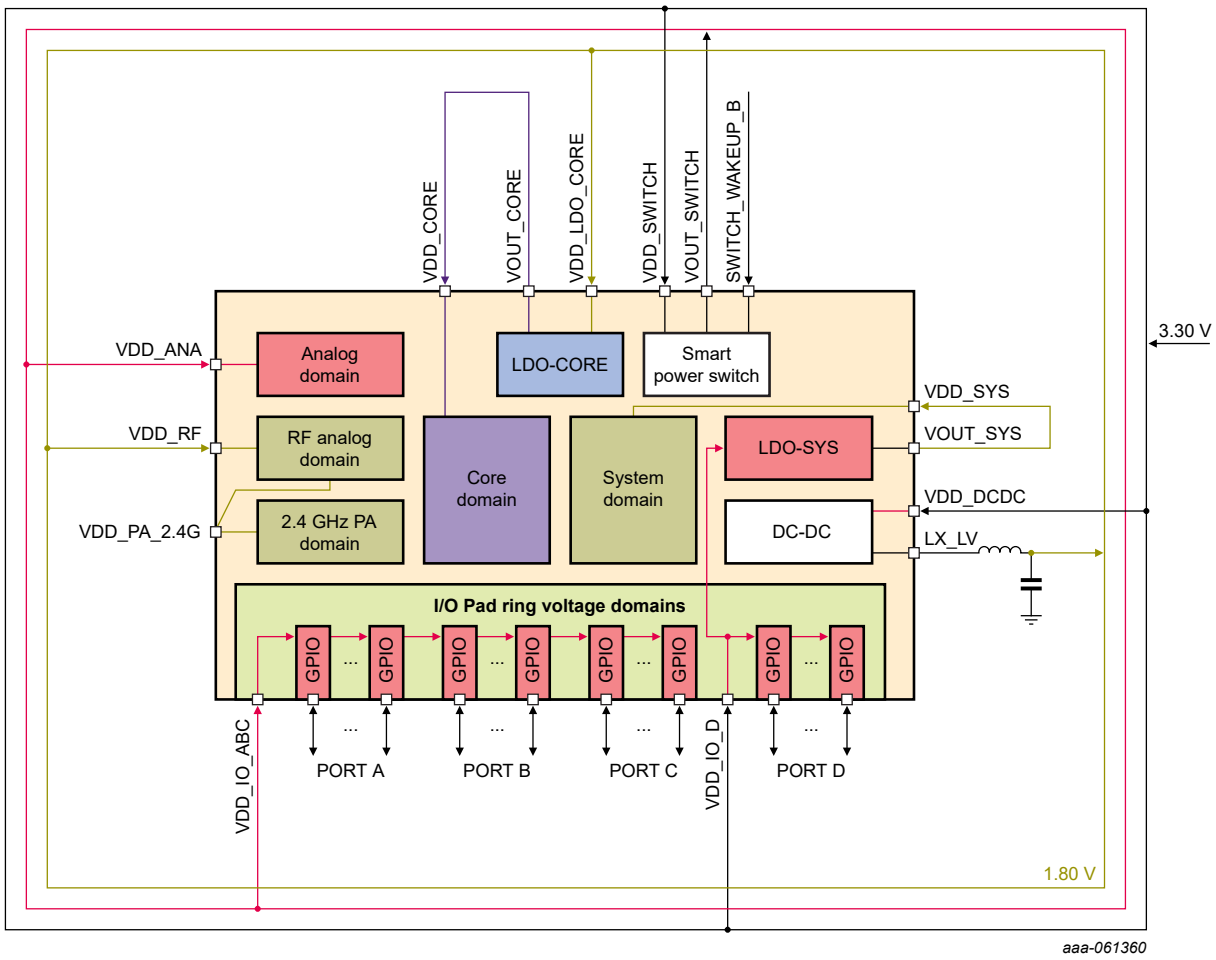

Figure 5. Power all supply except VDD_IO_D/VDD_DCDC

4 DC-DC buck converter

This section describes the characteristics, features, and operation of the DC-DC buck converter.

4.1 Enabling and disabling DC-DC buck converter

The DC-DC buck converter can be enabled and disabled according to the application configuration and requirements. The SPC regulator control register (CNTRL) can enable or disable the DC-DC on-chip converter by writing the SPC -> CNTRL[DCDC_EN] = 0. As a default setting, the DC-DC is enabled. However, if your design is bypassing the DC-DC, clear this bit to disable the DC-DC converter and prevent a leakage current.

4.1.1 DC-DC timing characteristics

Figure 6 shows the DC-DC startup time:

- The KW47 is connected in the DC-DC Buck mode and no external loads have been added.
- The DC-DC input and output voltages are DCDC_IN = 3.3 V and DCDC_OUT = 1.8 V.
- The DC-DC is configured in Normal drive strength mode.
- In Figure 6, the yellow curve represents the DCDC_OUT and the blue curve represents the DCDC_IN.

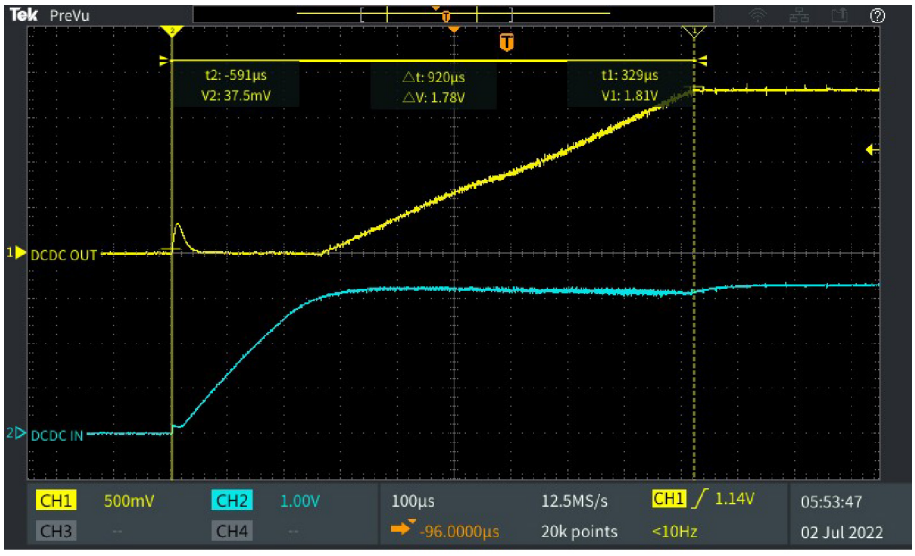

Figure 6. DC-DC startup time

Figure 7 shows the DC-DC shutdown time, considering the drop from 100 % to 10 % of the configured voltage:

- The KW47 is connected in the DC-DC Buck mode and no external loads have been added.
- The DC-DC input and output voltages are DCDC_IN = 3.3 V and DCDC_OUT = 1.8 V.
- The DC-DC is configured in the Normal drive strength mode.
- In Figure 7, the yellow curve represents the DCDC_OUT and the blue curve represents the DCDC_IN.

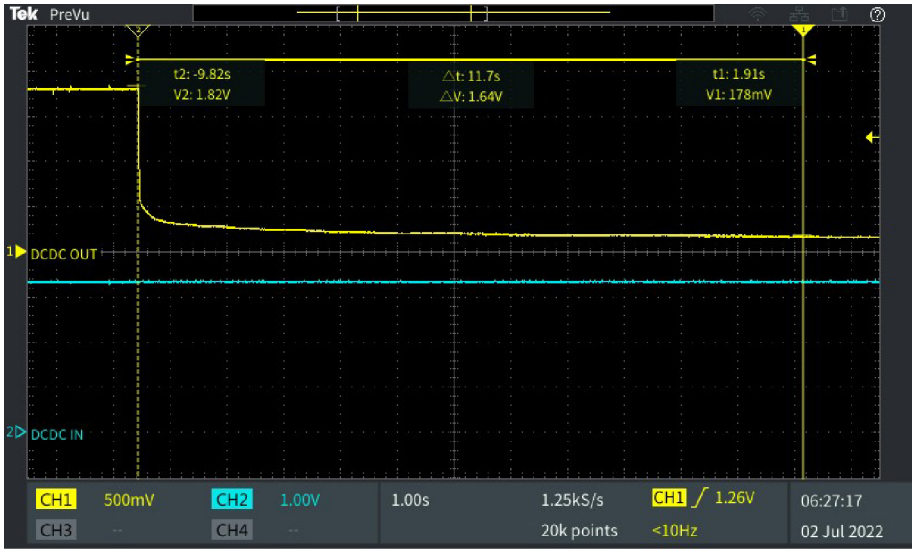

Figure 7. DC-DC shutdown time

4.2 DC-DC Drive strength modes

The DC-DC can operate in the following two different drive modes:

- Active mode
- Pulse refresh mode

Figure 8 depicts the DC-DC Drive Strength modes.

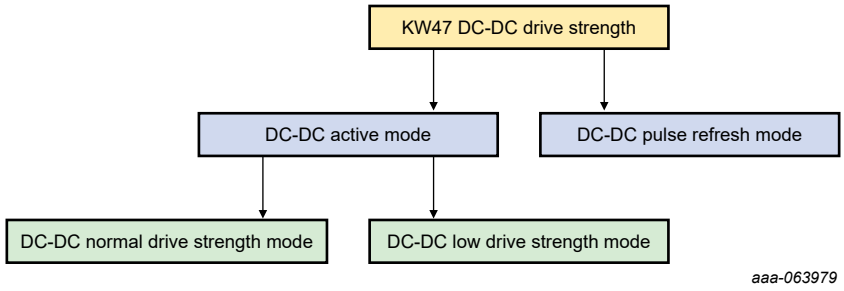

Figure 8. DC-DC drive strength modes

4.2.1 DC-DC Active mode

When operating in the Active mode, the DC-DC periodically issues a pulsed burst to maintain the output at the configured regulation voltage based on an internal analog-comparator monitoring system. This control mechanism ensures the regulation voltage always as long as the DC-DC load current is limited within the maximum specification. When the DC-DC is running in the Active mode, it can work in two different regulator drive strength modes: Normal drive strength and Low drive strength. Having different drive strength modes allow control over the quiescent current, which the DC-DC output driver manages. As a result, the DC-DC changes its maximum output current, the transient response, and efficiency as follows:

- **Normal drive strength mode**: The DC-DC provides the maximum output current capacity with the maximum DC-DC efficiency. This configuration provides the fastest transient response. However, the higher quiescent current at the operating point leads to a bigger DC-DC power consumption.
- **Low drive strength mode**: The DC-DC provides a limited output current capacity and less DC-DC efficiency. The transient response is slower than in Normal drive strength mode. However, this configuration decreases the overall power consumption of the DC-DC block due to a low quiescent current.

The selection of the Drive strength mode must account for the maximum current required by the application and the transient response requirements. If the DC-DC Drive mode operation is not critical in your application, or if the application behavior is hard to predict, keep these settings in the default configuration. It means using DC-DC Active mode with Normal drive strength mode. However, if your application requires optimizing the power consumption entering and exiting Low-power modes, consider setting the DC-DC Low drive strength mode.

Another option is to combine the DC-DC Normal drive strength in the MCU Active mode and DC-DC Low drive strength for Low-power modes.

4.2.2 DC-DC Pulse refresh mode

When the DC-DC is enabled and running in Pulse refresh mode, the DC-DC periodically issues a pulsed burst based on a programmed timer embedded on the system power control (SPC). In this mode, the analog-comparator monitoring system is disabled. Therefore, the DC-DC does not perform pulsed bursts to reload the output when the DC-DC output drops below the regulation voltage. Also, the SPC programmable timer period controls the DC-DC refresh burst entirely. In this mode, the DC-DC is turned off after completing the previous DC-DC burst. It turns on at the next timer timeout to reload the output.

The SPC -> DCDC_BURST_CFG [PULSE_REFRESH_COUNT] bit field controls how often the DC-DC is pulsed on and off based on the reference clock, which the CCM32K module (f_{CCM32K}) provides.

The SPC -> DCDC_BURST_CFG[PULSE_REFRESH_COUNT] bit field is a 16-bit counter value. It controls the frequency of the DC-DC refresh when DC-DC is configured in Pulse refresh mode.

The formula in Equation (1) is used to calculate the DC-DC refresh period (T_{DCDC_RFSH}) in Pulse refresh mode:

$$T_{DCDC\_RFSH} = \frac{1}{f_{CCM32K}} \times \left(PULSE\_REFRESH\_COUNT + 2\right) \quad (1)$$

4.2.2.1 Conditions to operate in the DC-DC Pulse refresh mode

The following conditions must be accomplished to operate the DC-DC in the Pulse refresh mode:

1. The software must configure the DC-DC Pulse refresh mode before the MCU goes to sleep. However, the DC- DC does not enter the Pulse refresh mode until:
   - All power domains have requested to enter the Low-power mode
   - The SPC has entered a low-power state
   - The MCU has successfully gone to sleep

   At wake-up, the DC-DC returns to the DC-DC Active mode.
2. The DC-DC Pulse refresh mode is not intended to supply external loads, but only the MCU itself. In DC-DC Pulse refresh mode, the DC-DC is enabled periodically to reload the DC-DC output capacitor based on the PULSE_REFRESH_CNT counter value. The rest of the time the DC-DC remains disabled. The application must configure the PULSE_REFRESH_CNT refresh rate to manage the voltage drop on the DC-DC capacitor and avoid a brownout condition. When the DC-DC is in Pulse refresh mode, an external load can cause the DC-DC output voltage to drop faster than the next DC-DC reload cycle. This condition brings the device to a brownout condition. Therefore, this mode is recommended when the MCU power domains are the only load connected on the DC-DC. For cases, when the DC-DC supplies the external loads while the MCU enters Deep power-down mode and a low DC-DC power consumption is desired, use the DC-DC in Low drive strength instead of DC-DC Pulse refresh mode.
3. The DC-DC Pulse refresh mode must enable the CCM32K clock output while the MCU enters low power to generate the periodic PWM bursts based on the PULSE_REFRESH_COUNT. The CCM32K peripheral can generate the clock output either from the external 32 kHz Xtal or from the internal FRO32K. If the application must disable the 32 kHz Xtal pins to enter the Sleep mode, and DC-DC is configured for Pulse refresh mode, perform the following:
   - Ensure that the FRO32K is enabled.
   - To generate the CCM32K clock before entering low-power mode, select FRO32K as the main source.

4.3 DC-DC frequency stabilization

The DC-DC frequency stabilization feature improves the switching frequency variations caused due to voltage transients in the DC-DC input, or dynamic loads at the DC-DC output. This feature can adjust the center switching frequency of the burst pulses. Therefore, you can consider it for applications sensitive to a particular frequency domain that can suffer interference from the DC-DC switching harmonics. Enabling the frequency stabilization feature causes a reduction of the DC-DC input reload current. However, there is a significant reduction of the maximum output current that the DC-DC can drive at its output.

If the DC-DC does not experience significant transients or drastic changes in the load, keep this feature disabled. As a default setting, the DC-DC frequency stabilization feature is disabled. You can try this feature considering that the DC-DC output current capability is going to get reduced, if:

- The application requires strict control over the DC-DC spectral content to avoid interference with other systems.

- If the application uses a coincell battery where the DC-DC current peaks impact directly on the battery lifetime.

To enable/disable the DC-DC frequency stabilization, write the SPC -> DCDC_CFG[FREQ_CNTRL_ON] bit field. When the frequency stabilization feature is enabled, the DC-DC switching frequency can be adjusted through the SPC -> DCDC_CFG[FREQ_CNTRL] 6-bit trimming value. The DC-DC frequency stabilization is only available for the DC-DC Active mode.

4.4 DC-DC burst synchronization

The application controls and monitors the DC-DC burst. Synchronizing with the quiet period between consecutive DC-DC bursts can be valuable for noise-sensitive applications, such as during a high-resolution ADC measurement. For this purpose, the DC-DC and the SPC provide the DCDC_BURST_TRIG_PULSE signal to synchronize the DC-DC burst activity with other peripherals in the device. This signal is asserted when the DC-DC burst completes and has entered the quiet period. This signal can trigger the ADC. To activate this signal, it is necessary to set SPC -> DCDC_BURST_CFG[EXT_BURST_EN] = 1. It is available as a trigger source in the TRGMUX peripheral and can be configured to trigger some on-chip peripherals. For more detail, see the *KW47 Reference Manual* (document KW47RM).

The application can request to initiate the DC-DC burst. For that purpose, the SPC -> DCDC_BURST_CFG[BURST_ACK] must be equal to '0' in the first instance. Then the software can set the SPC -> DCDC_BURST_CFG[BURST_REQ] = 1 to request a burst. The DC-DC and SPC hardware sets the SPC -> DCDC_BURST_CFG[BURST_ACK] = 1 when the burst has completed and the DC-DC has entered in the quiet period. Finally, the software writes '1' to the SPC -> DCDC_BURST_CFG[BURST_ACK] bit to clear the burst acknowledge flag.

For a high-resolution ADC conversion, you can configure the DCDC_BURST_TRIG_PULSE signal to trigger the ADC conversion and then the software initiates a DC-DC burst. At the completion of the current DC-DC burst, the ADC conversion is triggered in the DC-DC quiet period for an optimum ADC conversion result.

4.5 DC-DC voltage ramp-up control

The KW47 DC-DC integrates a voltage ramp-up control feature that inserts a delay in DC-DC voltage update when the DC-DC transitions to a higher voltage. This feature helps to control the DC-DC max transient current during the transition, decreasing the current peak due to DC-DC capacitor recharge. This feature is only available when:

- Switching the DC-DC voltage to a higher voltage level in the Active modes.
- The DC-DC drive strength is set to Normal and only supports the DC-DC voltage to 1.8 V maximum, does not support a transition to 2.5 V.

The following DC-DC voltage ramp is controlled on using the next registers:

- DCDC_CFG[RAMP_CNTRL_EN] provides an enable control of the feature.
- DCDC_CFG[RAMP_CNTRL] adjusts the ramp rate during the voltage transition.

4.6 DC-DC operation in power modes

The SPC peripheral has control over the DC-DC work modes. The SPC has the following three configuration registers:

- SPC Active power mode configuration register (ACTIVE_CFG)
- SPC Low-power mode configuration register (LP_CFG)
- SPC High-power mode configuration register (HP_CFG)

These registers are intended to have independent settings for the DC-DC when the KW47 transitions between the Active mode and Low-power mode or High-power request mode.

The ACTIVE_CFG, LP_CFG, and HP_CFG registers can configure the DC-DC voltage and Drive strength modes. Therefore, it is possible to configure the DC-DC in a different way automatically when the device moves to low power and exits it. Having independent configurations for the Active mode and Low-power mode allow the implementation of power-saving mechanisms by software. For example, it is possible to reduce the DC-DC voltage and set the DC-DC Low drive strength mode when the device goes to sleep, configuring the proper settings on the LP_CFG register. Then restore the DC-DC to a higher voltage and Normal drive mode at wake-up with the programmed settings in the ACTIVE_CFG. Even if the previous example is the expected operation for most of the applications, it is also possible to set the DC-DC to a higher voltage in the Low-power mode than in the Active mode if the application requires it.

In use cases where the radio must transmit at a high power (that is +10 dBm), it is required to increase the DC-DC output voltage. This request can be managed directly from the radio power domain (without the need to wake up the main power domain), using the RF_CMC. To request the High-power mode entry, the radio software configures the SPC_HP_CTRL[SPC_HP_MODE][3:0] to provide the target DC-DC output level. This parameter is one-hot encoded; possible DC-DC output values are: 1.35 V, 1.8 V, and 2.5 V while when setting the SPC_HP_MODE to 0x0, the DC-DC output remains unchanged.

Once the SPC_HP_MODE is configured, the radio software sets the SPC_HP_CTRL[SPC_HP_REQ] to initiate a request, and then waits for this request to be acknowledged. To acknowledge the request, the radio software reads the SPC_HP_STAT[SPC_HP_ACK]. Once acknowledged, the SPC has finalized the transition from the ACTIVE_CFG to HP_CFG.

Resetting the SPC_HP_CTRL[SPC_HP_REQ] triggers SPC to transition back from the HP_CFG to ACTIVE_CFG. You can monitor the end of this transition when polling the SPC_HP_ACK that returns to 0.

Table 5 describes the DC-DC operation modes allowed in each KW47 Power mode.

Table 5. DC-DC operation modes

Module	Active	Sleep	Deep Sleep	Power Down	Deep power-down mode
DC-DC buck converter	• SPC ACTIVE_CFG register controls the Normal or Low drive strength mode	SPC LP_CFG register controls the Normal or Low drive strength mode	• SPC LP_CFG controls the Normal, Low Drive Strength, Refresh mode	• SPC LP_CFG controls the Normal, Low Drive Strength, or Pulsed Refresh mode	Off
	• SPC HP_CFG controls the Normal drive strength mode when a high power request is active		• Off (Optional)	• Off (Optional)	

To configure the DC- DC in the Low drive strength mode when the MCU is in the Active mode, the application must set the same DC-DC output voltage on the ACTIVE_CFG and LP_CFG registers. It is mandatory to disable the HVD/LVD in the LP_CFG register before configuring the DC-DC in Pulsed refresh mode.

Any changes to the DC-DC drive strength or voltage level cause the SPC -> SC[BUSY] flag to assert to '1' logic level until SPC has completed changing its state to the new value. Therefore, software must check this status bit and wait until this bit clears to '0', to ensure that the SPC has completed the drive strength or voltage transition.

4.7 DC-DC main configuration registers

This section summarizes the main SPC registers involved in the configuration of the DC-DC buck converter in the KW47 MCU. Table 6 describes the SPC registers that configure the DC-DC behavior. For more details on the peripheral description, see the *KW47 Reference Manual* (document KW47RM).

SPC0 base address 4001_6000h

Table 6. DC-DC main configuration registers

Offset	Register	Width (bits)	Access	Reset value
14h	SPC regulator control register (CNTRL) This register controls the enablement of the SPC regulators.	32	WONCE	0000_0007h
60h	High power config control register (HP_CNFG_CNTRL) This register is used to enable the high power request feature.	32	RW	0000_0000h
100h	Active power mode configuration register (ACTIVE_CFG) This register controls the settings of the SPC regulators in the Active mode.	32	RW	3F10_0E15h
108h	Low-power mode configuration register (LP_CFG) This register controls the settings of the SPC regulators in the Low-power modes.	32	RW	0002_1104h
110h	High-Power mode configuration register (HP_CFG) This register controls the settings of the SPC regulators when in the Active mode and a high power request is active.	32	RW	3F10_0E15h
500h	DC-DC configuration register (DCDC_CFG) This register configures the frequency stabilization bit fields.	32	RW	0000_0000h
504h	DC-DC burst configuration register (DCDC_BURST_CFG) This register configures the DC-DC burst control bit fields.	32	RW	0140_0000h

4.7.1 SPC regulator control register (CNTRL)

CNTRL[DCDC_EN]: This bit field controls if the DC-DC is turned on (DCDC_EN = 1) or turned off (DCDC_EN = 0). As a default setting, the DC-DC is turned on. Ensure that the power domains, which this domain supplies can be disabled before disabling the DC-DC. If the DC-DC is bypassed, disable the DC-DC writing (DCDC_EN = 0).

4.7.2 High power config control register (HP_CNFG_CNTRL)

HP_CNFG_CNTRL[HP_REQ_EN]: This bit field controls the high power request HP_REQ_EN = 1 to enable or HP_REQ_EN = 0 to disable. Once this bit field is enabled, we need one of these two conditions to activate the high power request.

- HP_CNFG_CTRL[OVERRIDE_EN] = 0 and the secondary core domain asserts the external HP request.
- HP_CNFG_CTRL[OVERRIDE_EN] = 0 and HP_CNFG_CTRL[OVERRIDE_SEL] = 1.

HP_CNFG_CNTRL[OVERRIDE_EN]: This bit field overrides the high power request to a value, which the OVERRIDE_SEL sets. To enable OVERRIDE_EN = 1 and to disable OVERRIDE = 0.

HP_CNFG_CNTRL[OVERRIDE_SEL]: This bit field overrides the external high power request and forces the high power request to the OVERRIDE_SEL value.

4.7.3 Active power mode configuration register (ACTIVE_CFG)

- **ACTIVE_CFG[DCDC_VDD_LVL]**: This bit field controls the DC-DC output voltage when the SPC is in the Active mode. The DCDC_OUT = 2.5 V is only available for DC-DC Normal drive strength. To set the DCDC_OUT = 2.5 V, it is required to set the DCDC_CFG[VOUT2P5_SEL] = 1. For the rest of the voltage options, the VOUT2P5_SEL bit must be 0.

Table 7. DC-DC VDD regulator level

DCDC_VDD_LVL	VOUT2P5_SEL	DC-DC voltage
00b	0b	1.25 V
01b	0b	1.35 V
10b	0b	1.5 V
11b	0b	1.8 V
xxb	1b	2.5 V

- **ACTIVE_CFG[DCDC_VDD_DS]**: This bit field controls the DC-DC Drive strength mode when the SPC is in the Active mode. The valid Drive strength modes when the SPC is in the Active mode are DC-DC Normal and DC-DC Low drive strength. DC-DC Pulsed refresh mode is not available for SPC Active mode.

Table 8. DC-DC VDD regulator drive strength

DCDC_VDD_DS	DC-DC Drive mode
00b	Reserved
01b	Set to Low drive strength
10b	Set to Normal drive strength
11b	Reserved

4.7.4 Low-power mode configuration register (LP_CFG)

- **LP_CFG[DCDC_VDD_LVL]**: This bit field controls the DC-DC output voltage when the SPC is in the Low-power mode. The DCDC_OUT = 2.5 V is only available for DC-DC Normal drive strength. To set the DCDC_OUT = 2.5 V, it is required to set the DCDC_CFG[VOUT2P5_SEL] = 1. For the rest of the voltage options, the VOUT2P5_SEL bit must be 0.

Table 9. DC-DC VDD regulator level

DCDC_VDD_LVL	VOUT2P5_SEL	DC-DC voltage
00b	0b	1.25 V
01b	0b	1.35 V
10b	0b	1.5 V
11b	0b	1.8 V
xxb	1b	2.5 V

- **LP_CFG[DCDC_VDD_DS]**: This bit field controls the DC-DC Drive strength mode when the SPC is in the Low- power mode.

Table 10. DC-DC VDD regulator drive strength

DCDC_VDD_DS	DC-DC Drive mode
00b	Set to Pulse Refresh mode

Table 10. DC-DC VDD regulator drive strength...*continued*

DCDC_VDD_DS	DC-DC Drive mode
01b	Set to Low drive strength
10b	Set to Normal drive strength
11b	Reserved

4.7.5 High-Power mode configuration register (HP_CFG)

HP_CFG[DCDC_VDD_LVL]: This bit field controls the DC-DC output voltage when the SPC is in active configuration register when HP_CNFG_CTRL[HP_REQ_EN] = 1 and if any of the following conditions are true:

- HP_CNFG_CTRL[OVERRIDE_EN] = 0 and the secondary core domain asserts the external HP request.
- HP_CNFG_CTRL[OVERRIDE_EN] = 0 and HP_CNFG_CTRL[OVERRIDE_SEL] = 1.

The DCDC_OUT = 2.5 V is only available for DC-DC Normal drive strength mode. To set DCDC_OUT = 2.5 V, it is required to set DCDC_CFG[VOUT2P5_SEL] = 1. For the rest of the voltage options, the VOUT2P5_SEL bit must be 0.

The voltages in this register are only valid when SPC_HP_CTRL[SPC_HP_MODE] = 0.

Table 11. DC-DC VDD regulator level

DCDC_VDD_LVL	VOUT2P5_SEL	SPC_HP_CTRL[SPC_HP_MODE]	DC-DC voltage
00b	0b	0000b	1.25 V
01b	0b	0000b	1.35 V
10b	0b	0000b	1.5 V
11b	0b	0000b	1.8 V
xxb	1b	0000b	2.5 V

HP_CFG[DCDC_VDD_DS]: This bit field controls the DC-DC drive strength mode when the SPC is active is in active configuration register when HP_CNFG_CTRL[HP_REQ_EN] = 1 and if any of the following conditions are true:

- HP_CNFG_CTRL[OVERRIDE_EN] = 0 and the secondary core domain asserts the external HP request.
- HP_CNFG_CTRL[OVERRIDE_EN] = 0 and HP_CNFG_CTRL[OVERRIDE_SEL] = 1.

Table 12. DC-DC VDD regulator drive strength

DCDC_VDD_DS	DC-DC Drive mode
00b	Reserved
01b	Set to Low drive strength
10b	Set to Normal drive strength
11b	Reserved

4.7.6 DC-DC configuration register (DCDC_CFG)

- **DCDC_CFG[VOUT2P5_SEL]**: This bit field must remain enabled (VOUT2P5_SEL = 1) if the desired DC-DC output is 2.5 V (DCDC_VDD_LVL = 10b). Otherwise, this bit must remain disabled (VOUT2P5_SEL = 0). If VOUT2P5_SEL = 1 and DCDC_VDD_LVL is different than 10b (DC-DC output voltage selection is not 2.5 V), the DC-DC output voltage is not predictable. Therefore, you must enable this bit only if the output voltage is 2.5 V. If the output voltage must move from 2.5 V to another voltage level, this bit must be cleared (VOUT2P5_SEL = 0). The 2.5 V option is only available in DC-DC Normal drive strength mode. If the DC-DC

is operating at 2.5 V in DC-DC Normal drive strength mode and you must change the DC-DC drive strength mode, do the following:
  – Update the DC-DC output value to any other allowed value
  – Clear this bit
- **DCDC_CFG[FREQ_CNTRL_ON]**: This bit field enables/disables the frequency stabilization function in the DC-DC. Frequency stabilization is enabled with FREQ_CNTRL_ON = 1 and disabled with FREQ_CNTRL_ON = 0. When it is enabled, the DC-DC burst frequency can be adjusted with the FREQ_CNTRL bit field from the central frequency.
- **DCDC_CFG[FREQ_CNTRL]**: This bit field represents a 6-bit trimming value for the DC-DC burst frequency when the frequency stabilization feature is enabled, FREQ_CNTRL_ON = 1. When FREQ_CNTRL_ON = 0, FREQ_CNTRL trimming value is ignored.

4.7.7 DC-DC burst configuration register (DCDC_BURST_CFG)

- **DCDC_BURST_CFG[PULSE_REFRESH_CNT]**: This bit field is a 16-bit multiplier value that determines the DC-DC burst occurrence when the DC-DC is in Pulse refresh mode based on the CCM32K output frequency. See Section 4.2.2.
- **DCDC_BURST_CFG[BURST_ACK]**: This bit field is an indicator flag that sets to '1' when the previous DC-DC burst has completed successfully that the software has requested. This bit must be cleared each time at the completion of a burst, which the software requests when writing BURST_ACK = 1.
- **DCDC_BURST_CFG[EXT_BURST_EN]**: This bit enables/disables the internal DCDC_BURST_TRIG_PULSE signal that is used to trigger some peripherals with the TRGMUX when the DC-DC enters in the quiet period. The EXT_BURST_EN = 1 enables the trigger signal and the EXT_BURST_EN = 0 disables the trigger signal. This bit must be written only when the BURST_ACK = 0 and before writing the BURST_REQ = 1 to request a DC-DC burst.
- **DCDC_BURST_CFG[BURST_REQ]**: Write BURST_REQ = 1 to initiate a burst request. Do not initiate a new burst request until the previous one has been completed and acknowledged (clearing the BURST_ACK flag).

4.8 DC-DC main configuration registers

This section includes the DC-DC electrical characteristics.

4.8.1 DC-DC converter specifications

Table 13 summarizes the DC-DC converter specifications.

Table 13. DC-DC converter specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_DCDC_IN	DC-DC input voltage	1.71	-	3.6	V	1, 2
V_DCDC_OUT	DC-DC output voltage					1, 2
	1.25	1.1875	1.25	1.3125	V	
	1.35	1.2825	1.35	1.475	V	
	1.5	1.425	1.5	1.575	V	
	1.8	1.71	1.8	1.89	V	
	2.5	2.375	2.5	2.625	V	
V_DCDC_ RIPPLE	Ripple voltage at DC-DC output: • Normal drive strength mode • Low drive strength mode	 - -	 1 25	 - -	 % mV	 3 -

Table 13. DC-DC converter specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Notes
I_DCDC_LOAD	Load current at DC-DC output:					
	• Normal drive strength mode	-	-	105	mA	1, 4
	• Low drive strength mode	-	-	15	mA	1, 4
	• Frequency Stabilization on [FREQ_ CNTRL_ON = 1]	-	-	45	mA	1, 4
LX	DC-DC output inductor value	0.8	1	2.2	µH	5
ESR	DC-DC inductor equivalent series resistance	-	110	-	mΩ	6
COUT	DC-DC output capacitance	6	22	30	µF	7
F_Burst	DC-DC reload burst frequency	3	5	8	MHz	8
F_Burst_ Accuracy	DC-DC reload burst frequency accuracy	-	10	-	%	8

Note:

1. *The DC-DC converter generates 1.8 V at DCDC_LX by default. The DC-DC can be used to power VDD_RF, VDD_LDO_CORE, and external components as long as the maximum ILOAD is not exceeded.*
2. *The VDD_DCDC input supply to DC-DC must be at least 500 mV higher than the desired output at DCDC_LX.*
3. *The DC ripple is shown as a percentage in relation with the programmed DC-DC output voltage.*
4. *The maximum load current during boot-up must not exceed 60 mA.*
5. *The recommended inductor value is 1 µH to 1.5 µH. If the inductor is < 1 µH, the DC-DC efficiency is not guaranteed.*
6. *The maximum recommended ESR is 250 mΩ (not a hard limit).*
7. *The variation in capacitance of the capacitor at DCDC_LX due to aging, temperature, and voltage degradation must not exceed the min/max values.*
8. *FREQ_CNTRL_ON = 1.*

5 LDO core and LDO system regulators

This section describes the characteristics, features, and operation of the LDO core and LDO system regulators.

5.1 Enabling and disabling LDOs

Both the LDO core and LDO system can be enabled and disabled according to the application requirements. The SPC regulator Control register (CNTRL) can enable or disable the LDO CORE and LDO SYS. To enable or disable the LDO CORE and LDO SYS, write the SPC -> CNTRL[CORELDO_EN] = 0 and SPC -> CNTRL[SYSLDO_EN] = 0 respectively. As a default setting, both the LDOs are enabled. However, if your design is bypassing any of these regulators, you must disable such LDO to prevent a leakage current. The LDO outputs, VOUT_CORE and VOUT_SYS, are internally tied with VDD_CORE and VDD_SYS power domains respectively. Therefore, before disabling any of these regulators, ensure that such power domain is connected with an external power supply. Some power modes are allowed to turn off the VDD_CORE power domain.

Therefore, if no external voltage is connected on the VDD_SYS power domain, the LDO system regulator cannot be disabled. Disable the LDO core or LDO system as follows:

- To disable the high and low voltage detectors (SYS_HVDE, CORE_HVDE, SYS_LVDE, and CORE_LVDE), change the value to 0b in the corresponding bit fields in the SPC -> ACTIVE_CFG register

- Wait until the SPC -> SC[BUSY] = 0

To disable the LDO core regulator, clear the SPC -> CNTRL[CORELDO_EN] or SPC -> CNTRL[SYSLDO_EN] bit fields as it corresponds.

The LDO core and LDO system have a pulldown resistor that forces the LDO discharge when the software disables the regulator or, in the specific case of the LDO core, when the MCU enters in Deep power-down mode. This feature is enabled as a default setting. However, when the LDO core and LDO system are disabled to drive the VDD_CORE and VDD_SYS voltages from an external power supply, it is recommended to disable the pulldown resistors to prevent current leakage. To disable the pulldown resistors, write SPC -> CORELDO_CFG[DPDOWN_PULLDOWN_DISABLE] = 1 for the LDO CORE regulator and SPC ->SYSLDO_CFG[ISINKEN] = 0 for the LDO SYS regulator.

5.1.1 LDO timing characteristics

This section includes the timing characteristics of the LDO core and LDO system regulators.

5.1.1.1 LDO core timing characteristics

Figure 9 shows the LDO core startup time:

- The KW47 has been connected in the DC-DC Buck mode and no external loads have been added.
- In this configuration, the DC-DC output serves as the power supply for the LDO core.
- The DC-DC input voltage is DCDC_IN = 3.3 V.
- The LDO core input and output voltages are LDO_CORE_IN = DCDC_OUT = 1.8 V and LDO_CORE_OUT = 1.05 V.
- The DC-DC and LDO core are configured in Normal drive strength mode.
- In this capture, the red curve represents DCDC_IN, the blue curve represents LDO_CORE_IN/DCDC_OUT, and the yellow curve represents LDO_CORE_OUT.

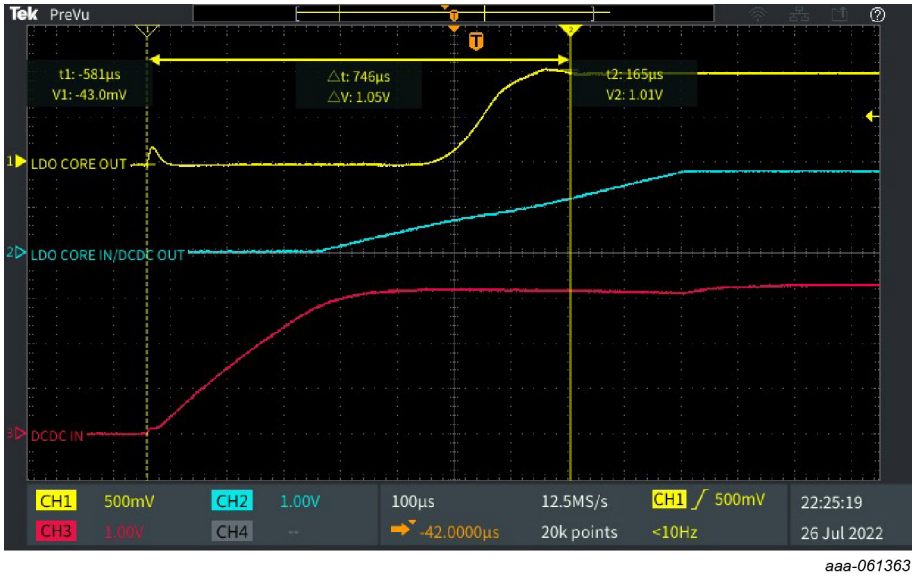

Figure 9. LDO core startup time

Figure 10 shows the LDO core shutdown time:

- The KW47 has been connected in the DC-DC Buck mode and no external loads have been added.
- The DC-DC input voltage is DCDC_IN = 3.3 V.

- The LDO core input and output voltages are LDO_CORE_IN/DCDC_OUT = 1.8 V and LDO_CORE_OUT = 1.05 V.
- The LDO core and DC-DC are configured in Normal drive strength mode.
- In Figure 10, the yellow curve represents LDO_CORE_OUT and the blue curve represents LDO_CORE_IN/DCDC_OUT.

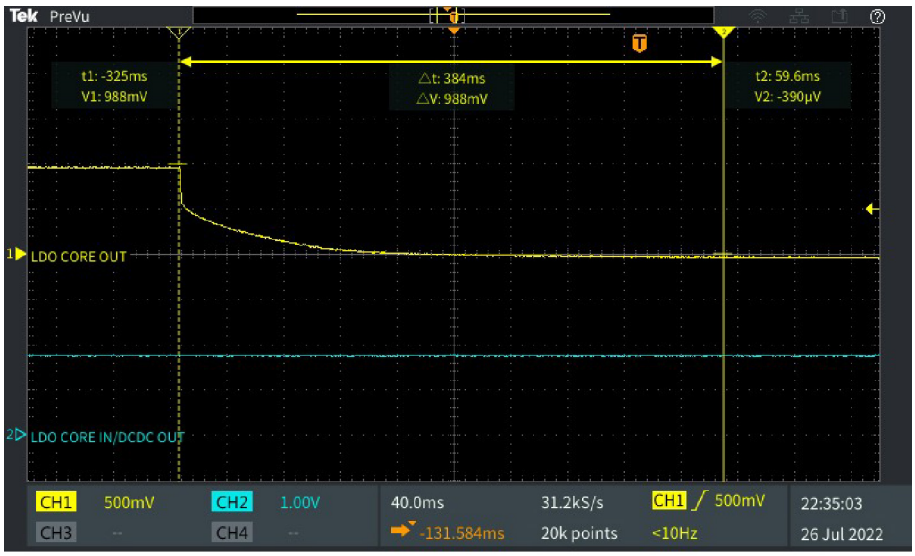

Figure 10. LDO core shutdown time

5.1.1.2 LDO system timing characteristics

Figure 11 shows the LDO system startup time:

- The KW47 has been connected in the DC-DC Buck mode and no external loads have been added.
- The LDO system input and output voltages are LDO_SYS_IN = 3.3 V and LDO_SYS_OUT = 1.8 V.
- The LDO SYS is configured in Normal drive strength mode.
- In Figure 11, the yellow curve represents LDO_SYS_OUT and the blue curve represents LDO_SYS_IN.

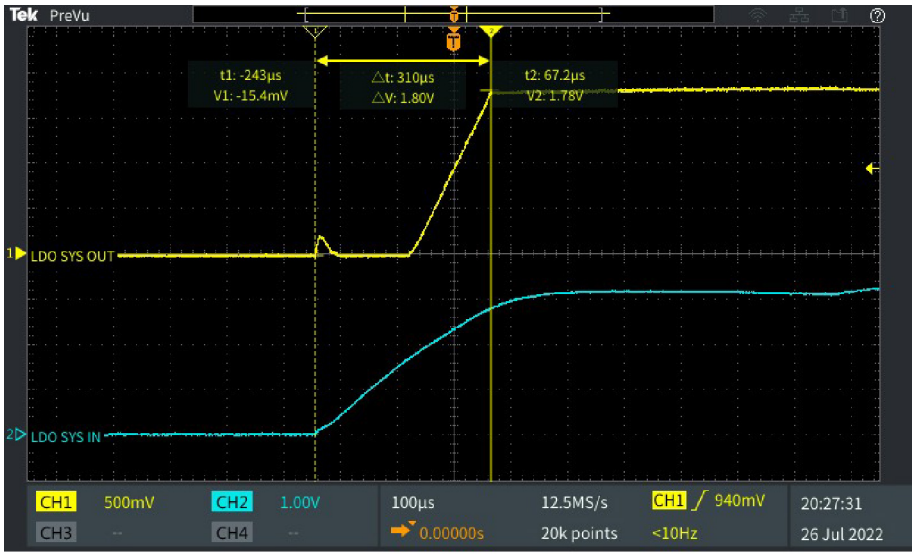

Figure 11. LDO system startup time

5.2 LDO drive strength modes

The LDO core and LDO system have the following two drive strength modes:

- Normal drive strength
- Low drive strength

In Normal drive strength mode, the LDO regulator provides the maximum output current capability. On the other hand, the Low drive strength LDO mode limits the output current. The LDO regulator supplies the core and power systems domains but does not supply the external loads. If the LDO drive strength mode selection is not critical in your application while the MCU runs in the Active mode, keep the default settings, that is, the LDO core and LDO system in Normal drive strength mode. If the application requires to enter low-power mode, configure the LDO in the Low drive strength to reduce power consumption. This approach considers that the power domains supplied through the LDO regulators do not exceed a few microamps and the LDO is not overstressed in this condition. Once the MCU wakes up, you can select the Normal drive strength mode for each LDO if required.

5.3 LDO operation in power modes

Similar to the DC-DC buck converter, the LDO core and LDO system regulators can be configured in an independent way in the Active and Low-power modes. The SPC registers, Active power mode configuration register (ACTIVE_CFG) when in high power request (HP_CFG), and SPC low-power mode configuration register (LP_CFG) provide the configuration alternatives for the corresponding mode.

Table 14 describes the LDO operation modes allowed in each KW47 power mode.

Table 14. LDO operation modes

Module	Active	Sleep	Deep Sleep	Power down	Deep power down
LDO core	• SPC ACTIVE_CFG controls the Normal or Low drive strength mode	SPC LP_CFG controls the Normal or Low drive strength mode	• SPC LP_CFG controls the Normal or Low drive strength mode	• SPC LP_CFG controls the Normal or Low drive strength mode	Off

Table 14. LDO operation modes...*continued*

Module	Active	Sleep	Deep Sleep	Power down	Deep power down
	• SPC HP_CFG controls the Normal drive strength mode		• Off (optional)	• Off (optional)	
LDO system	• SPC ACTIVE_CFG controls the Normal or Low drive strength mode	SPC LP_CFG controls the Normal or Low drive strength mode	SPC LP_CFG controls the Normal or Low drive strength mode	SPC LP_CFG controls the Normal or Low drive strength mode	SPC LP_CFG controls the Normal or Low drive strength mode
	• SPC HP_CFG controls the Normal drive strength mode				

When the application is running, the LDO system must be configured at 1.8 V. The LDO system 2.5 V output voltage alternative must be selected only when the MCU must program the eFuses. Therefore, this voltage option is only available when the MCU is running in the Active mode. When the LDO system is running at 2.5 V, the LDO is forced to operate in the Normal drive strength mode.

The LDO system Low drive strength mode is available only if the LDO is configured at 1.8 V. Before changing the LDO system drive strength to Low drive strength in the ACTIVE_CFG or LP_CFG, ensure to disable all the HVD/LVD in the corresponding configuration. Enabling any HVD/LVD while the LDO system is in the Low drive strength mode forces the LDO to operate in Normal drive strength mode.

Note: *Any changes to the DC-DC drive strength or voltage level cause the SPC -> SC[BUSY] flag to assert to '1' logic level until the SPC has completed changing its state to the new value. Therefore, the software must check the SPC -> SC[BUSY] status bit and wait until this bit clears to '0' to ensure that the SPC has completed the drive strength or voltage transition.*

5.4 LDO main configuration registers

This section summarizes the main SPC registers involved in the configuration of the LDO regulators in the KW47 MCU. Table 15 describes the SPC registers that configure the behavior of each LDO. For more details on the peripheral description, see the *KW47 Reference Manual* (document KW47RM).

SPC0 base address 4001_6000h

Table 15. SPC registers

Offset	Register	Width (bits)	Access	Reset value
14h	SPC regulator control register (CNTRL) This register controls the enablement of the SPC regulators.	32	WONCE	0000_0007h
100h	Active power mode configuration register (ACTIVE_CFG) This register controls the settings of the SPC regulators in the Active mode.	32	RW	3F10_0E15h
108h	Low-power mode configuration register (LP_CFG) This register controls the settings of the SPC regulators in the Low-power modes.	32	RW	0002_1104h
110h	High power mode configuration register (HP_CFG)	32	RW	3F10_0E15h

Table 15. SPC registers...*continued*

Offset	Register	Width (bits)	Access	Reset value
	This register controls the settings of the SPC regulators when in the Active mode and a high power request is active.			
300h	LDO_CORE configuration register (CORELDO_CFG)	32	RW	0000_0000h
400h	LDO_SYS configuration register (SYSLDO_CFG)	32	RW	0000_0101h

5.4.1 SPC regulator control register (CNTRL)

- **CNTRL[CORELDO_EN]**: This bit field controls whether the LDO core is turned on (CORELDO_EN = 1) or turned off (CORELDO_EN = 0). As a default setting, the LDO core is turned on. Ensure that the power domains, which this domain supplies can be disabled before disabling this LDO. If the LDO core is bypassed, to disable the LDO core write CORELDO_EN = 0.
- **CNTRL[SYSLDO_EN]**: This bit field controls whether the LDO system is turned on (SYSLDO_EN = 1) or turned off (SYSLDO_EN = 0). As a default setting, the LDO system is turned on. If the LDO system is bypassed, to disable the LDO system write SYSLDO_EN = 0.

5.4.2 Active power mode configuration register (ACTIVE_CFG)

- **ACTIVE_CFG[CORELDO_VDD_LVL]**: This bit field controls the LDO core output voltage when the SPC is in the Active mode.

Table 16. CORELDO_VDD_LVL and LDO voltage

CORELDO_VDD_LVL	LDO voltage
00b	Reserved
01b	1.05 V
10b	1.1 V
11b	1.15 V

- **ACTIVE_CFG[SYSLDO_VDD_LVL]**: This bit field controls the LDO system output voltage when the SPC is in the Active mode.

Table 17. SYSLDO_VDD_LVL and LDO voltage

SYSLDO_VDD_LVL	LDO voltage
0b	1.8 V
1b	2.5 V

- **ACTIVE_CFG[SYSLDO_VDD_DS]**: This bit field controls the LDO System drive strength mode when the SPC is in the Active mode.

Table 18. SYSLDO_VDD_DS and LDO Drive mode

SYSLDO_VDD_DS	LDO Drive mode
0b	Set to low drive strength
1b	Set to normal drive strength

5.4.3 Low-power mode configuration register (LP_CFG)

- **LP_CFG[CORELDO_VDD_LVL]**: This bit field controls the LDO core output voltage when the SPC is in the Low- power mode.

Table 19. CORELDO_VDD_LVL and LDO voltage

CORELDO_VDD_LVL	LDO voltage
00b	Reserved
01b	1.05 V
10b	1.1 V
11b	1.15 V

- **LP_CFG[CORELDO_VDD_DS]**: This bit field controls the LDO Core drive strength mode when the SPC is in the Low-power mode.

Table 20. CORELDO_VDD_DS and LDO Drive mode

CORELDO_VDD_DS	LDO Drive mode
0b	Set to low drive strength
1b	Set to normal drive strength

- **LP_CFG[SYSLDO_VDD_DS]**: This bit field controls the LDO System drive strength mode when the SPC is in Low-power mode.

Table 21. SYSLDO_VDD_DS and LDO Drive mode

SYSLDO_VDD_DS	LDO Drive mode
0b	Set to low drive strength
1b	Set to normal drive strength

5.4.4 High power mode configuration register (HP_CFG)

- **HP_CFG[CORELDO_VDD_LVL]**: This bit field controls the LDO core output voltage when the SPC is in the High power request mode.

Table 22. CORELDO_VDD_LVL and LDO voltage

CORELDO_VDD_LVL	LDO voltage
00b	Reserved
01b	1.05 V
10b	1.1 V
11b	1.15 V

- **HP_CFG[SYSLDO_VDD_LVL]**: This bit field controls the LDO system output voltage when the SPC is in the High power request mode.

Table 23. SYSLDO_VDD_LVL and LDO voltage

SYSLDO_VDD_LVL	LDO voltage
0b	1.8 V
1b	2.5 V

- **HP_CFG[SYSLDO_VDD_DS]**: This bit field controls the LDO System drive strength mode when the SPC is in the High power request mode.

Table 24. SYSLDO_VDD_DS and LDO Drive mode

SYSLDO_VDD_DS	LDO Drive mode
0b	Set to low drive strength
1b	Set to normal drive strength

5.4.5 LDO_CORE configuration register (CORELDO_CFG)

CORELDO_CFG[DPDOWN_PULLDOWN_DISABLE]: This configuration register is used to control whether the pull-down sink resistor is enabled or disabled in the LDO core. It is used to discharge the LDO output voltage fast when this regulator is shut down in Deep power-down mode. This resistor is enabled by default and it is recommended not to change this setting.

5.4.6 LDO_SYS configuration register (SYSLDO_CFG)

SYSLDO_CFG[ISINKEN]: This configuration register is used to control whether the pull-down sink resistor is enabled or disabled in the LDO system. It is used to discharge the LDO output voltage fast when this regulator is shut down. This resistor is enabled by default and it is recommended not to change this setting.

5.5 LDO electrical characteristics

This section includes the electrical characteristics of the LDO core and LDO system regulators.

5.5.1 LDO core electrical characteristics

Table 25 summarizes the LDO core regulator specifications.

Table 25. LDO core regulator specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_LDO_CORE_IN	LDO core input voltage	1.25	-	3.6	V	1, 2
V_LDO_CORE_OUT	LDO core output voltage:					
	• Normal drive strength mode	1.05	-	1.15	V	
	• Low drive strength mode	1.05	-	1.15	V	
I_LDO_CORE_LOAD	LDO core max load current at LDO output:					
	• Normal drive strength: 0.20 V < VDROP_OUT < 0.4 V	-	-	40	mA	
	• Normal drive strength: VDROP_OUT > 0.4 V	-	-	60	mA	
	• Low drive strength: 0.20 V < VDROP_OUT < 0.4 V	-	-	18	mA	
	• Low drive strength: VDROP_OUT > 0.4 V	-	-	28	mA	
Iinrush	LDO core inrush current	-	-	500	mA	
COUT	LDO core external output capacitor	3.7	4.7	10	µF	
Cdec	LDO core external decoupling capacitor	-	0.1	-	µF	

Table 25. LDO core regulator specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Notes
ESR	External output capacitor equivalent series resistance	-	10	-	mΩ	

Note:

1. *To bypass the LDO_CORE, tie VDD_LDO_CORE to VDD_CORE.*
2. *The VDD_LDO_CORE input supply must be set to 200 mV higher than the VOUT_CORE in the mid-voltage regulation option (1.05 V). For the rest of the supported voltage regulation options, it must be set to 250 mV higher than the VOUT_CORE.*

5.5.2 LDO system electrical characteristics

Table 26 summarizes the LDO system regulator specifications.

Table 26. LDO system regulator specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_LDO_SYS_IN	LDO system input voltage:					
	• LDO_SYS input supply voltage in Regulation mode	1.86	-	3.6	V	1
	• LDO_SYS input supply voltage in Bypass mode	1.8	-	1.98	V	1
	• LDO_SYS input in Fuse programming mode	2.75	-	3.6	V	1
V_LDO_SYS_OUT	LDO system output voltage:					
	• Normal drive strength mode	1.71	1.8	1.98	V	2, 3, 4, 5
	• Fuse Programming mode	2.25	2.5	2.75	V	2, 3, 4, 5
I_LDO_SYS_LOAD	LDO system max load current at LDO output:					
	• Normal drive strength mode	-	-	50	mA	
	• Low drive strength mode	-	-	2	mA	
	• Fuse programming mode	-	-	40	mA	
I_LDO_SYS_IN	LDO system input current consumption:					
	• Normal drive strength mode	-	100	-	µA	6
	• Low drive strength mode	-	70	-	nA	6
Iinrush	LDO core inrush current	-	-	120	mA	
COUT	LDO core external output capacitor	-	1.5	10	µF	
Cdec	LDO core external decoupling capacitor	-	0.1	-	µF	
ESR	External output capacitor equivalent series resistance	-	30	-	mΩ	

Note:

1. *The regulator automatically switches to pass through, that is the driver of the regulator is fully on, with the supply below 1.95 V.*

2. *The LDO_SYS converter generates 1.8 V by default at the VOUT_SYS. The VOUT_SYS can be used to power the VDD_SYS, VDD_RF, VDD_IO_X, and VDD_ANA, as long as the max ILOAD is not exceeded.*
3. *The VOUT_SYS and VDD_SYS are connected.*
4. *The VDD_IO_D must be at least 150 mV higher than the desired VOUT_SYS.*
5. *The LDO_SYS can be used to program efuse and in this configuration the output voltage can range between 2.25 V and 2.75 V.*
6. *In Normal drive strength, the LDO_SYS draws ~100 µA for every 20 mA of load current. For an external output capacitor, the value is 1.5 µF. If the capacitor has a 10 µF value, this value must be 300 mA instead.*

6 Smart power switch - VBAT

VBAT is a smart power and low-resistance switch that works with the power management system to implement the power-saving mechanisms. It can be used to switch off all or some power domains to obtain the lowest power consumption possible.

However, if the KW47 is running on a battery with limited peak current, do not use the smart power switch constantly. The DC-DC introduces a high inrush current during the DC-DC startup, which can shorten the lifespan of the battery. Therefore, for battery-powered applications, it is recommended to use the smart power switch carefully when the system is powered off for an extended period. This switch can also be used for power distribution control of external loads on the board as load and voltage requirements are within the VBAT specifications. For some typical configurations for the smart power switch, see Section 3.3.

Figure 12 shows the smart power switch architecture in the KW47 MCU.

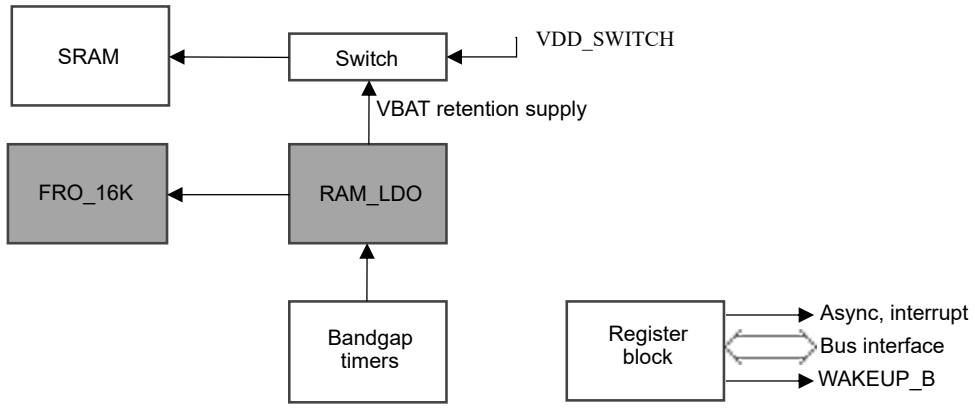

Figure 12. Smart power switch (VBAT) block diagram

6.1 Smart power switch hardware

The smart power switch can switch on/off a load but also includes hardware embedded on it, which the independent power domain VDD-SWITCH supplies. This hardware offers extra features to fulfill many application requirements for the KW47 MCU.

The following sections describe the smart power switch hardware and its capabilities.

6.1.1 VBAT FRO16K and bandgap timers

The smart power switch has an internal 16.384 kHz oscillator, which the VDD- SWITCH power domain known as the VBAT FRO16K oscillator supplies. The FRO16K can remain active in all Low-power modes. The

FRO16K is used by the VBAT. However, some other peripherals in the KW47 can also use it. For more details, see the *KW47 Reference Manual* (document KW47RM).

In addition to the FRO16K oscillator, the smart power switch has the following two bandgap timers:

- Bandgap timer 0
- Bandgap timer 1

Both the bandgap timers use FRO16K as a reference clock to determine its counter value and are supplied with the VDD-SWITCH power domain. The bandgap timers can turn on the smart power switch when the timer count expires. The bandgap timers can also program the VBAT to switch off the system for a determined period. In the KW47 MCU, the bandgap timers can be configured as follows:

- The bandgap timer 0 timeout can be configured in the range of 7.8125 ms to 1 s
- The bandgap timer 1 timeout ranges from 1 s to 65535 s

Before starting any bandgap timer, turn on the FRO16K (VBAT -> FROCTLA[FRO_EN] = 1) and enable the LDO RAM bandgap bit (VBAT -> LDOCTLA[BG_EN] = 1).

6.1.2 VBAT LDO RAM retention and SRAM retention array

When the smart power switch controls all power domains, the application running on the device resets the execution when the VBAT switches off and on. As a result, the application context is lost due to the loss of power on the system. To manage this use case, the smart power switch includes an LDO that can supply an 8 kB SRAM array dedicated to retain the application data when the VBAT is turned off. This feature enables quick recovery after the POR sequence of the device when the smart power switch turns on again.

In general, the LDO RAM retention regulator can be used to keep the power of the SRAM retention at any time or through any Low-power mode in which the application data is lost. However, all access to the SRAM retention address range is not allowed while the LDO RAM is powering this memory. Otherwise, any attempt to access the memory triggers a fault condition. The 8 kB SRAM retention array address range is from 0x2001_A000 to 0x2001_BFFF, which corresponds to the STCM5 in the KW47 device. The STCM5 supports the ECC in the KW47 devices.

6.1.2.1 VBAT LDO RAM enable sequence

To enable the VBAT LDO RAM retention regulator, perform the following steps:

1. Enable the VBAT FRO16K oscillator: VBAT -> FROCTLA[FRO_EN] = 1.
2. Enable the LDO RAM bandgap bit: VBAT -> LDOCTLA[BG_EN] = 1.
3. To achieve the lowest power consumption, set the LDO RAM in Low-power refresh mode by enabling the following bit: VBAT -> LDOCTLA[REFRESH_EN] = 1.
4. Enable the LDO RAM regulator: VBAT -> LDOCTLA[LDO_EN] = 1.
5. Wait until the LDO_RDY flag is set, polling the VBAT -> STATUSA[LDO_RDY] bit.

6.1.2.2 Powering the SRAM retention memory with VBAT LDO RAM regulator

As a default setting, the VDD_CORE domain powers the SRAM retention memory. Therefore, if the application requires the use of a memory retention feature, the software must configure the proper registers to move the SRAM power supply from the VDD_CORE domain to the VBAT LDO RAM regulator. As explained in Section 6.1.2, any attempt to read or write the SRAM retention memory while it is supplied with the LDO RAM regulator results in a fault. Therefore, the application data must be saved in the SRAM address range before switching the memory power supply.

To configure the VBAT LDO RAM regulator to supply the SRAM retention memory, perform the following steps:

1. Enable the VBAT LDO RAM. For more details, see Section 6.1.2.1.

2. Configure VBAT -> LDORAMC[ISO] = 1.
3. Configure VBAT -> LDORAMC[SWI] = 1.

Once the VBAT turns on, the software must reverse these steps to switch the SRAM memory power to the VDD_CORE domain and be able to access the SRAM retention memory and load the application context.

1. Configure VBAT -> LDORAMC[SWI] = 0.
2. Configure VBAT -> LDORAMC[ISO] = 0.

6.1.3 VBAT on/off control

Any of the four following methods can turn on the smart power switch:

1. After a VBAT power-on reset (POR), the internal wake-up logic turns on the smart power switch automatically. The VBAT POR occurs on a power cycle on the VDD_SWITCH. The VBAT POR resets the register of the smart power switch to the original state. It is the only way that the hardware can reset these values. After a VBAT POR, the smart power switch output is on by default. The VBAT POR is independent from the device POR.
2. The software can turn on the VBAT after a falling edge on the external SWITCH_WAKEUP_B pin, which is available in the KW47. The SWITCH_WAKEUP_B pin is pulled up internally.
3. To wake up the VBAT after programmed time, the software can program any of the two VBAT bandgap timers before shutting down the smart power switch. The VBAT bandgap timers are embedded in the smart power switch.
4. The SPC can activate the switch through SPC -> CFG MCU active settings when the smart power switch controls the activation of external loads on the board. The software writing the corresponding settings in the SPC -> CFG register deactivates the smart power switch. The SPC registers configure independent settings for the smart power switch on/off control when the KW47 is in the following mode:
   a. KW47 MCU Active mode settings (MCU running and executing code):
      The SPC -> CFG active settings can enable/disable the smart power switch to drive external loads on the circuit. The SPC -> CFG register active settings must not be used to enable/disable the smart power switch when it controls the KW47 power supply.
   b. KW47 MCU Low-power mode settings:
      The SPC -> CFG low power settings provide configuration bits to deactivate the smart power switch automatically when the device enters in the Low-power mode. Once the MCU recovers from the Low-power mode, the smart power switch SWITCH_WAKEUP_B or internal VBAT bandgap timers can activate the smart power switch again.
      The smart power switch low power settings are used to control the KW47 power supply. Therefore, to disable the switch, the application software must configure the smart power switch low power settings first, then execute the sequence to enter Low-power mode.

The following are the SPC -> CFG register enable/disable settings in the Active and Low-power modes:

1. SPC->CFG[INTG_PWSWTCH_WKUP_ACTIVE_EN]: VBAT enable bit in Active mode
   Writing 1 to this bit enables the smart power switch when the MCU is in the Active mode. Modifying this bit to '1' or '0' when the MCU is in the Active mode and VBAT is already enabled, does not affect. It is used to control the external loads.
2. SPC->CFG[INTG_PWSWTCH_SLEEP_ACTIVE_EN]: VBAT disable bit in Active mode
   Writing 1 to this bit disables the smart power switch when the MCU is in the Active mode. Modifying this bit either to '1' or '0' when the MCU is in the Active mode and VBAT is already disabled, does not affect. It is used to control the external loads.
3. SPC->CFG[INTG_PWSWTCH_WKUP_EN]: VBAT enable bit in Low-power mode
   Writing 1 to this bit enables the smart power switch when the MCU exits from any Low-power mode. It is used to enable the main power supply of the device through the smart power switch exiting from a Low-power mode.

4. SPC->CFG[INTG_PWSWTCH_SLEEP_EN]: VBAT disable bit in Low-power mode
   Writing 1 to this bit disables the smart power switch when the MCU enters to any Low-power mode. It is used to disable the main power supply of the device through the smart power switch entering in a Low-power mode.

The application software must not enable the "INTG_PWSWTCH_WKUP_ACTIVE_EN" and "INTG_PWSWTCH_SLEEP_ACTIVE_EN" at the same time, as it causes an invalid condition.
To turn on the smart power switch while the MCU operates in the Active mode, set the INTG_PWSWTCH_WKUP_ACTIVE_EN = 1 and INTG_PWSWTCH_SLEEP_ACTIVE_EN = 0.
On the other hand, to turn off the VBAT, set INTG_PWSWTCH_WKUP_ACTIVE_EN = 0 and INTG_PWSWTCH_SLEEP_ACTIVE_EN = 1 simultaneously. If the application does not use the smart power switch in the MCU Active mode, do not write these bits.

For VBAT low-power operation, the software can enable the INTG_PWSWTCH_WKUP_EN and INTG_PWSWTCH_SLEEP_EN simultaneously to switch off the VBAT while the KW47 is in the Low-Power mode and turn it on again when the device exits from low power. It is possible to enable any of the VBAT control bits individually for the Low-Power modes depending on application requirements and the expected operation. If the application does not use the smart power switch in the MCU Low-power modes, do not write these bits.

If the software configures the smart power switch to wake up through the SWITCH_WAKEUP_B external pin or from any of the programmable bandgap timers, the software must clear the corresponding status flag.

Then set the INTG_PWSWTCH_WKUP_ACTIVE_EN = 1 and INTG_PWSWTCH_SLEEP_ACTIVE_EN = 0 to complete the smart power switch activation and prepare the hardware for the next smart power switch shutdown sequence in advance.

6.2 Smart power switch main configuration registers

This section summarizes the SPC and VBAT main registers involved in the configuration of the smart power switch in the KW47 MCU.

This section shows the SPC registers that configure the DC-DC behavior. For more details, see the *KW47 Reference Manual* (document KW47RM).

SPC0 base address 4001_6000h

Table 27. SPC register

Offset	Register	Width (bits)	Access	Reset value
20h	SPC configuration register (CFG) This register controls the smart power switch on and off states in MCU Active and LP modes.	32	RW	0000_0000h

Table 28 shows the VBAT registers that configure the DC-DC behavior.

VBAT0 base address 4002_B000h

Table 28. VBAT registers

Offset	Register	Width (bits)	Access	Reset value
10h	Status A (STATUSA) This register contains the status flags related with the VBAT turn-on events.	32	W1C	0000_0001h
20h	Wakeup enable A (WAKENA) This register enables/disables the smart power switch to turn-on source options.	32	RW	0000_0001h
200h	FRO16K control A (FROCTLA)	32	RW	0000_0001h

Table 28. VBAT registers*...continued*

Offset	Register	Width (bits)	Access	Reset value
	This register contains the enable/disable option for the internal 16 kHz VBAT oscillator.			
300h	LDO RAM control A (LDOCTLA) This register contains the enablement options for the LDO RAM retention regulator.	32	RW	0000_0000h
320h	RAM control (LDORAMC) This register configures the power supply settings for the SRAM retention memory.	32	RW	0000_0000h
330h	Bandgap timer 0 (LDOTIMER0) This register contains the enable and timeout settings for the bandgap timer 0.	32	RW	0000_0000h
338h	Bandgap timer 1 (LDOTIMER1) This register contains the enable and timeout settings for the bandgap timer 1.	32	RW	0000_0000h

6.2.1 SPC configuration register (CFG)

- **CFG[INTG_PWSWTCH_WKUP_ACTIVE_EN]**: VBAT enable bit in Active mode

Writing 1 to this bit enables the smart power switch when the MCU is in Active mode. Changing this bit to any other value when the MCU is in Active mode and VBAT is enabled, does not affect it. Do not enable this bit to 1 when INTG_PWSWTCH_SLEEP_ACTIVE_EN = 1. It is used to control external loads.

- **CFG[INTG_PWSWTCH_SLEEP_ACTIVE_EN]**: VBAT disable bit in Active mode

Writing 1 to this bit disables the smart power switch when the MCU is in Active mode. Changing this bit to any other value when the MCU is in Active mode and VBAT is turned on, does not affect it. Do not enable this bit to 1 when INTG_PWSWTCH_WKUP_ACTIVE_EN = 1. It is used to control external loads.

- **CFG[INTG_PWSWTCH_WKUP_EN]**: VBAT enable bit in Low-power mode

Writing 1 to this bit enables the smart power switch when the MCU exits any Low-power mode. It is used to enable the main power supply of the device through the smart power switch exiting a Low-power mode.

- **CFG[INTG_PWSWTCH_SLEEP_EN]**: VBAT disable bit in Low-power mode

Writing 1 to this bit disables the smart power switch when the MCU enters any Low-power mode. It is used to disable the main power supply of the device through the smart power switch entering a Low-power mode.

6.2.2 Status A (STATUSA)

- **STATUSA[LDO_RDY]**: Read-only status bit
  To determine if the LDO RAM retention regulator is enabled and steady, check this bit. This bit is set to 1 when the LDO RAM is enabled.
- **STATUSA[TIMER1_FLAG]**: Status bit for the bandgap timer 1
  This bit is set to 1 to indicate that the bandgap timer 1 timeout has expired. To clear this bit after the timeout event, the software writes 1 to this bit.
- **STATUSA[TIMER0_FLAG]**: Status bit for the bandgap timer 0
  This bit is set to 1 to indicate that the bandgap timer 0 timeout has expired. To clear this bit after the timeout event, the software writes 1 to this bit.
- **STATUSA[WAKEUP_FLAG]**: Status bit for the external SWITCH_WAKEUP_B pin on the device

This bit is set to 1 to indicate that the external wake-up pin has been pulled down. To check and clear this bit after a wake-up button press event, the software writes 1 to this bit.

- **STATUSA[POR_DET]**: Status bit for the VBAT power-on reset detection event
  This bit is set to 1 after a VBAT POR. To clear this bit after the VBAT POR event, the software writes 1 to this bit.

6.2.3 Wakeup enable A (WAKENA)

- **WAKENA [TIMER1_FLAG]**: To enable this bit, write 1 to this field to switch on the smart power switch when the bandgap timer 1 timeout has been reached. Writing 0 to this bit disables this feature.
- **WAKENA [TIMER0_FLAG]**: To enable this bit, write 1 to this field to switch on the smart power switch when the bandgap timer 0 timeout has been reached. Writing 0 to this bit disables this feature.
- **WAKENA [WAKEUP_FLAG]**: To enable this bit, write 1 to this field to switch on the smart power switch when the external SWITCH_WAKEUP_B signal is pulled down. Writing 0 to this bit disables this feature.

6.2.4 FRO16K control A (FROCTLA)

- **FROCTLA[FRO_EN]**: Writing 1 to this bit enables the VBAT FRO16K oscillator. This oscillator is enabled by default. Ensure that the FRO16K oscillator is enabled before using the bandgap timers or the LDO RAM retention regulator.

6.2.5 LDO RAM control A (LDOCTLA)

- **LDOCTLA[REFRESH_EN]**: This bit enables the LDO RAM Refresh mode, which decreases the LDO power consumption. The LDO RAM sets this bit to 1 to enter Refresh mode.
- **LDOCTLA[LDO_EN]**: This bit activates the LDO RAM. Before setting this bit to 1 to enable the LDO RAM regulator, it is required to follow the sequence described in Section 6.1.2.1.
- **LDOCTLA[BG_EN]**: This bit enables the LDO RAM bandgap required as part of the LDO RAM enable sequence. Writing 1 to this bit enables the LDO RAM bandgap.

6.2.6 RAM control (LDORAMC)

- **LDORAMC[SWI]**: This bit is used to select the SRAM retention memory power supply between the VDD_CORE domain and the VBAT LDO RAM. To select the LDO RAM, it is required to set SWI = 1. To select the VDD_CORE, SWI must be 0. Before selecting the VBAT LDO RAM as the power supply for the SRAM retention memory, it is required to set the LDORAMC[ISO] = 1.
- **LDORAMC[ISO]**: Set this bit to 1, to:
  – Isolate the SRAM memory power supply from the rest of the memory
  – Place the array in Low-power Retention mode before switching the SRAM supply to the VBAT LDO RAM

6.2.7 Bandgap timer 0 (LDOTIMER0)

- **LDOTIMER0[TIMEN]**: To enable the bandgap timer 0, write 1 to this bit. The timer starts counting immediately after writing this bit. Therefore, this bit must be written lastly as a part of the bandgap timer enable sequence. Before updating the VBAT timeout, ensure that this bit is disabled, TIMEN = 0.
- **LDOTIMER0[TIMCFG]**: This 3-bit field configures the bandgap timer 0 timeout value.

Table 29 shows the timeout options.

Table 29. Bandgap timer 0

LDOTIMER0[TIMCFG]	Bandgap timer 0 timeout
000b	1 s

Table 29. Bandgap timer 0*...continued*

LDOTIMER0[TIMCFG]	Bandgap timer 0 timeout
001b	500 ms
010b	250 ms
011b	125 ms
100b	62.5 ms
101b	31.25 ms
110b	15.625 ms
111b	7.8125 ms

6.2.8 Bandgap timer 1 (LDOTIMER1)

- **LDOTIMER1[TIMEN]**: To enable the bandgap timer 1, write 1 to this bit. The timer starts counting immediately after writing this bit. Therefore, this bit must be written lastly as a part of the bandgap timer enable sequence. Before updating the VBAT timeout, ensure that this bit is disabled, TIMEN = 0.
- **LDOTIMER1[TIMCFG]**: This 24-bit field configures the bandgap timer 1 timeout value. It can be configured in the range from 1 s to 65535 s with a resolution of 1 s per increment in the TIMCFG value.

6.3 Smart power switch electrical characteristics

Table 30 summarizes the smart power switch core specifications. The SWITCH_WAKEUP_B pad is internally pulled up to the switch input through a resistor. It can be pulled down to wake up the smart power switch.

To generate an internal wake-up signal, the maximum value of the SWITCH_WAKEUP_B pulldown voltage is 0.7 V and duration time must be larger than 1 µs.

Table 30. Smart power switch core specifications

Symbol	Description	Min	Typ	Max	Unit
V_SWITCH_IN	VDD_SWITCH input voltage	1.9	-	3.6	V
I_SWITCH_OUT	Smart power switch output load current	-	-	40	mA
Ron	Switch series resistance at the on state	-	-	3	Ω
I_leakage1	Typical leakage current when V_SWITCH_IN = 2.7 V at 25 °C	-	4	-	µA
I_leakage2	Maximum leakage current when V_SWITCH_IN = 3.3 V at 25 °C	-	-	1	µA

7 Acronyms

Table 31 lists the acronyms used in this document.

Table 31. Acronyms

Acronym	Description
ADC	Analog-to-digital converter
CMC	Clock monitor control
CRC	Cyclic redundancy check
DAP	Debug access port
DC	Direct current
DSP	Digital signal processing
DWT	Data watchpoint and trace
eDMA	Enhanced direct memory access
EWM	External watchdog monitor
FlexCAN	Flexible controller area network
FlexIO	Flexible input/output
FMU	Frequency management unit
FPU	Floating point unit
FRO	Free running oscillator
GPIO	General purpose input/output
I3C	Improved inter-integrated circuit instance
ITM	Instrumentation trace macrocell
LDO	Low dropout regulator
LP	Low power
LPCMP	Low-power comparator
LPI2C	Low-power inter-integrated circuit
LPIT	Low-power interrupt timer
LPSPI	Low-power serial peripheral interface
LPTMR	Low-power timer
LPUART	Low-power universal asynchronous receiver/transmitter
MCU	Microcontroller unit
MPU	Memory protection unit
MRCC	Main reset control circuit
MSCM	Multi-core system control module
NBU	Narrowband unit
NVIC	Nested vectored interrupt controller
OSC-RTC	Oscillator for real-time clock
POR	Power-on reset

Table 31. Acronyms...*continued*

Acronym	Description
PRBRIGDE	Peripheral bridge
RAM	Random-access memory
RF	Radio frequency
RFMC	Rf management controller
RTC	Real-time clock
SCG	System clock generator
SFA	Secure flash access
SMSCM	Secure multi-core system control module
SPC	System power controller
SRAM	Static random-access memory
SWD	Serial wire debug
SYSTICK	System tick timer
TAMPER	Tamper detection
TCM	Tightly coupled memory
TPM	Timer/pwm module
TRDC	Trusted resource domain controller
TRGMUX	Trigger multiplexer
TZM	Trustzone module
VBAT	Voltage battery
WDOG	Watchdog
WUU	Wake-up unit

8 References

Table 32 lists the references used to supplement this document.

Table 32. Related documentation/resources

Document	Link/how to access
KW47 Reference Manual (document KW47RM)	KW47RM

9 Revision history

Table 33 summarizes the revisions to this document.

Table 33. Revision history

Document ID	Release date	Description
AN14709 v.2.0	10 December 2025	Initial public release
AN14709 v.1.0	03 July 2025	Initial NDA release

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