AN14685

PF9453 QFN schematic and layout guidelines

Rev. 1.0 — 9 June 2025 Application note

Document information

Information	Content
Keywords	PF9453, QFN, PMIC
Abstract	This application note provides guidelines for schematic and good layout practices for PF9453 QFN PMIC

1 Introduction

This application note outlines schematic and PCB layout design guidelines for the PF9453 QFN Power Management IC (PMIC). While applicable to all PF9453 QFN variants (MPF9453AXMXXHN), the term PF9453HN is used throughout for simplicity.

The PF9453HN is a highly integrated PMIC designed to deliver a complete power management solution for NXP's i.MX91/93 processor families, as well as other industrial and IoT platforms with similar power requirements.

2 Packaging

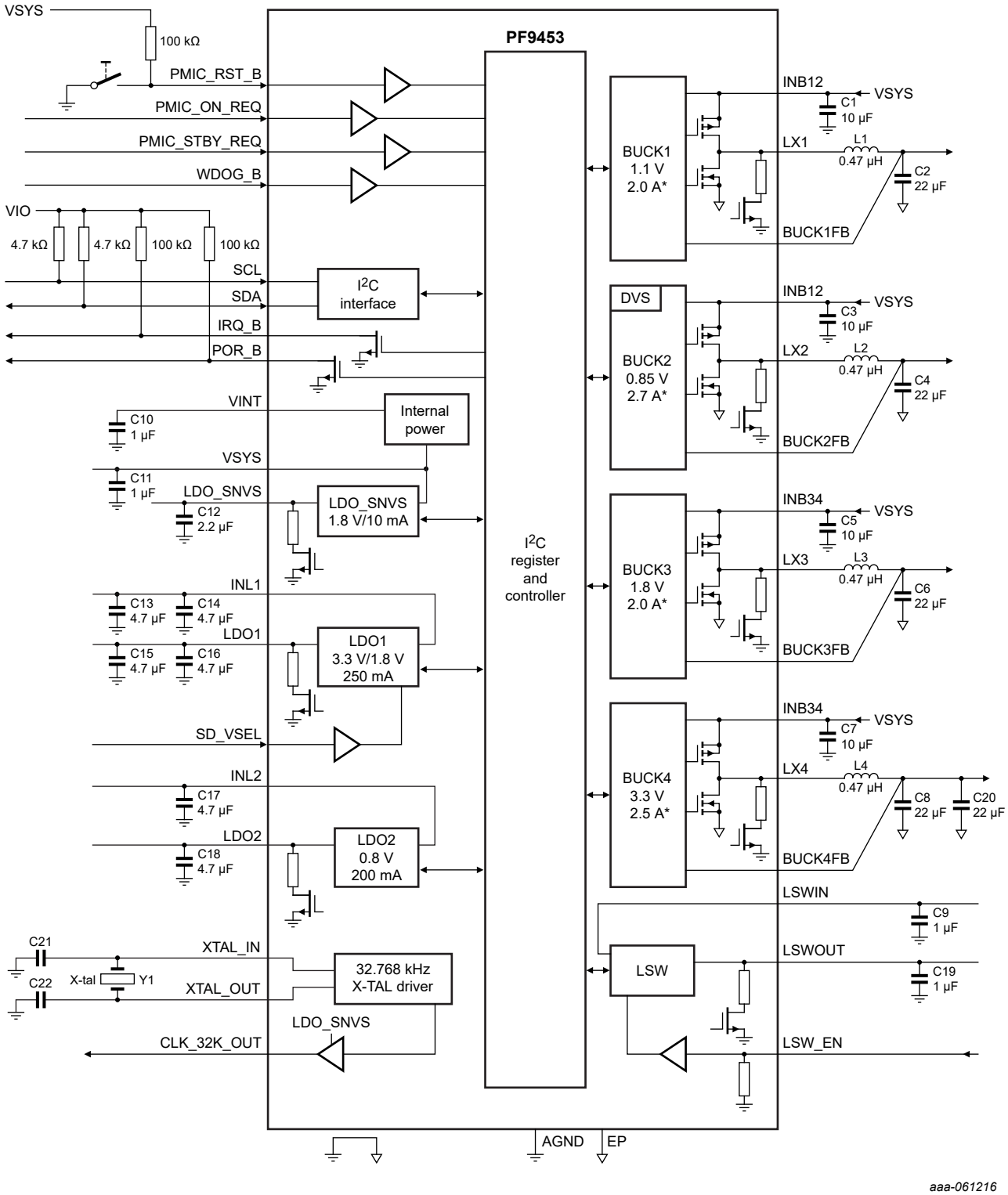
The PF9453HN is designed for both consumer and industrial applications and is available in a 40-pin HVQFN package with a 5 mm × 5 mm body size and 0.4 mm pitch. Refer to Table 1 for the package drawing information.

Table 1. Package drawing information

Package	Description	Package outline drawing number
HVQFN40	40-pin QFN, 5.0 mm x 5.0 mm with exposed pad, 0.4 mm pitch	SOT2231-1

3 PF9453HN reference schematic

PF9453HN reference schematic with i.MX 91 processor is illustrated in Figure 1.



Note*: Output current of PF9453 regulators changes depending on the part number; refer to Table 1 in the PF9453DS

Figure 1. PF9453HN (OTP configuration A1) application schematic

The schematic and design reference for PF9453HN can be found at the following link:

- https://www.nxp.com/PF9453AHN-EVB

4 Schematic design guidelines

This section describes the guidelines related to the schematic design process.

4.1 Pin connection guidelines

Table 2 provides the recommended pin connections for the PF9453HN. These guidelines help ensure that the PF9453HN operates correctly.

Note: *VIN refers to* ***Input Voltage*** *of the PMIC.*

Table 2. PF9453HN pin connection guidelines

Pin Symbol	Pin	Pin Type	Pin Function	Recommended Connection	Recommended connection when not used
LDO2	1	Power	LDO2 output	Bypass with a 4.7µF/6.3V to GND	Leave floating
INL2	2	Power	LDO2 input	Bypass with a 4.7µF/6.3V to GND	Connect to VIN
BUCK2FB	3	Analog input	BUCK 2 feedback	Connect to the BUCK 2 output rail close to the load	Connect to INB12
LX2	4, 5	Power	BUCK 2 switching node	Connect to a 0.47µH inductor	Leave floating
INB12	6, 7	Power	BUCK 1 and BUCK 2 inputs	Bypass with two 10µF/6.3V ceramic capacitors	Connect to VIN
LX1	8, 9	Power	BUCK 1 switching node	Connect to a 0.47µH inductor	Leave floating
BUCK1FB	10	Analog input	BUCK 1 feedback	Connect to the BUCK 1 output rail close to the load	Connect to INB12
POR_B	11	Digital output	Power On reset output	Place a pull-up resistor from 20kΩ to 220kΩ to a system I/O supply rail	Leave floating
SCL	12	Digital input	I^2C serial clock	Place a 4.7 kΩ pull-up resistor to a system I/O supply rail	Place a 4.7 kΩ pull-up resistor to a system I/O supply rail
SDA	13	Digital input / output	I^2C serial data	Place a 4.7 kΩ pull-up resistor to a system I/O supply rail	Place a 4.7 kΩ pull-up resistor to a system I/O supply rail
CLK_32K_OUT	14	Digital output	32.768kHz clock CMOS output with LDO_SNVS power rail	Connect to the clock input signal of the processor or other peripheral	Leave floating
PMIC_ON_REQ	15	Digital input	PMIC ON input from application processor. When it is asserted high, the device starts power on sequence	Connect to PMIC_ON_REQ pin from the processor. Pull-up via 8 kΩ - 100 kΩ to LDO_SNVS if required	Place a 100k pull-up resistor to LDO_SNVS rail
XTAL_IN	16	Analog input	32.768kHz crystal oscillator input	Connect to crystal oscillator and bypass with a capacitor to GND (18pF typically)	Connect to GND
XTAL_OUT	17	Analog output	32.768kHz crystal oscillator output	Connect to crystal oscillator and bypass with a capacitor to GND (18pF typically)	Leave floating

Table 2. PF9453HN pin connection guidelines*...continued*

Pin Symbol	Pin	Pin Type	Pin Function	Recommended Connection	Recommended connection when not used
PMIC_RST_B	18	Digital input	PMIC reset input pin. Once it is asserted low, PMIC performs cold reset	Connect to reset signal from processor	Connect to VIN
IRQ_B	19	Digital output	PMIC interrupt pin, open drain output requiring external pull up resistor	Place a pull-up resistor from 20kΩ to 220kΩ to a system I/O supply rail	Leave floating
WDOG_B	20	Digital input	Watchdog reset input from application processor	Connect to watchdog reset signal from processor	Connect to VIN
BUCK4FB	21	Analog input	BUCK 4 feedback	Connect to the BUCK 4 output rail close to the load.	Connect to INB34
LX4	22, 23	Power	BUCK 4 switching node	Connect to a 0.47µH inductor	Leave floating
INB34	24, 25, 26	Power	BUCK 3 and BUCK 4 inputs	Bypass with two typical 10µF/6.3V ceramic capacitors	Connect to VIN
LX3	27, 28	Power	BUCK 3 switching node	Connect to a 0.47µH inductor	Leave floating
BUCK3FB	29	Analog input	BUCK 3 feedback	Connect to the BUCK 3 output rail close to the load.	Connect to INB34
LSW_EN	30	Digital input	Load switch enable input. It has internal 1.5MΩ pull down resistor	Connect to processor I/O pin for load switch enable input	Leave floating
PMIC_STBY_REQ	31	Digital input	Standby mode input from application processor. When it is asserted high, device enters STANDBY mode.	Connect to PMIC_STBY_REQ signal from processor	Connect to GND
LSWIN	32	Power	Load Switch input	Bypass with a 1µF/16V to GND	Connect to GND
LSWOUT	33	Power	Load Switch output	Bypass with a 1µF/16V to GND	Leave floating
AGND	34	GND	Analog GND	It should be connected to GND plane through a via. Do not short directly to EPAD on top layer.	N/A
SD_VSEL	35	Digital input	LDO1 voltage selection input.	Connect to processor I/O pin	Connect to GND
VINT	36	Power	Internal power supply output	Bypass with 1µF/16V to GND	N/A
VSYS	37	Power	Internal power input	Bypass with a 1 µF/16V to GND, connect to VIN	N/A
LDO_SNVS	38	Power	LDO_SNVS output	Bypass with a 2.2µF/16V to GND	Leave floating
LDO1	39	Power	LDO1 output	Bypass with 2 x 4.7µF/6.3V to GND	Leave floating
INL1	40	Power	LDO1 input	Bypass with 2 x 4.7µF/6.3V to GND	Connect to VIN
EPAD	41	GND	Exposed pad	Connect this pad to the inner and external GND planes through	N/A

Table 2. PF9453HN pin connection guidelines...*continued*

Pin Symbol	Pin	Pin Type	Pin Function	Recommended Connection	Recommended connection when not used
				multiple vias to allow effective thermal dissipation.	

4.2 BUCK converter guidelines

This section describes guidelines for selecting passive components for each BUCK converter of the PF9453HN.

4.2.1 Inductor selection for BUCK converters

Each BUCK converter in the **PF9453HN** typically uses a **0.47 µH inductor**, which must be appropriately rated for both **DC resistance (DCR)** and **saturation current**. The inductor's DCR directly impacts the converter's efficiency—therefore, selecting an inductor with **low DCR** is essential for achieving high efficiency.

The table below lists inductors with low DCR suitable for this application.

In addition to DCR, **AC losses**—which depend on the inductor's material and construction—can also significantly affect efficiency. For accurate assessment of AC losses in a specific use case, it is recommended to consult the inductor manufacturer.

Below are the equations needed to calculate the **peak-to-peak inductor ripple current** (ΔI_L) and **maximum inductor current** (I_{L_max}), and how to choose a good inductor for a specific use case.

4.2.1.1 Inductor current calculations

To select a suitable inductor, it's important to calculate both the peak-to-peak ripple current and the maximum inductor current. The process begins with determining the duty cycle (D) of the BUCK converter, taking into account conduction losses.

Equation 1 shows how to do this calculation.

$$D = \frac{Vout\left[1+\frac{R_{ec}}{R}\right]}{Vin\_max} \quad (1)$$

Where:

- D = duty cycle
- $Vout$ = BUCK output voltage (V)
- Vin_max = Maximum BUCK Input voltage (V)
- R = Output load (Ω)
- R_{ec} = Equivalent resistance in conduction mode (Ω)

As can be seen from the above equation, NXP recommends calculating the duty cycle (D) considering the **equivalent resistance in conduction mode** (R_{ec}) to obtain an accurate result, Equation 2 shows how to calculate (R_{ec}).

$$R_{ec} = R_L + (D)(HS\_R_{DSON}) + (1-D)(LS\_R_{DSON}) \quad (2)$$

Where:

- D = duty cycle

- R_L = Inductor series resistance (Ω).
- HS_R_{DSON} = High Side P-FET Drain to Source Resistance during ON state (Ω).
- LS_R_{DSON} = Low Side N-FET Drain to Source Resistance during ON state (Ω).

In addition to Equation 2, there is a simplified alternative in which the D value is replaced with an ideal value, output voltage (Vout) divided by input voltage (Vin), substituting in the previous Equation 3 is obtained.

$$R_{ec} \approx R_L + \frac{Vout}{Vin\_max} x\ HS\_R_{DSON} + \left(1 - \frac{Vout}{Vin\_max}\right) x\ LS\_R_{DSON} \quad (3)$$

Where:

- R_L = Inductor series resistance (Ω).
- HS_R_{DSON} = High Side P-FET Drain to Source Resistance during ON (Ω).
- LS_R_{DSON} = Low Side N-FET Drain to Source Resistance during ON (Ω).
- $Vout$ = BUCK output voltage (V).
- Vin_max = Maximum BUCK Input voltage (V).

With the results obtained in the equations above the ***peak-to-peak inductor ripple current*** can be calculated with the Equation 4. Finally, by adding the maximum DC current expected in the specific use case, the Equation 5 calculates the ***maximum inductor current***.

$$\Delta I_L = \frac{(Vin\_max - Vout)\, D}{L\ x\ f} \quad (4)$$

$$I_{L\_max} = I_{out\_max} + \frac{\Delta I_L}{2} \quad (5)$$

Where:

- f = Switching frequency (Hz)
- L = Inductance (H)
- ΔI_L = peak-to-peak inductor ripple current (A)
- I_{L_max} = Maximum inductor current (A)
- I_{out_max} = Maximum output DC current (A)

The saturation current of the inductor must be rated higher than the ***maximum inductor current*** as calculated with Equation 5. This is needed because during a heavy load transient the inductor current raises above the calculated value.

A conservative approach is to select the inductor current rating for the calculated maximum switching current (I_{out_max}).

4.2.1.2 Recommended inductors for PF9453HN

Table 3 shows possible inductor list for each BUCK converter on PF9453HN.

Table 3. Tested inductor list

BUCK	Vendor	Part Number	Inductance (µH)	Size (mm)	DCR (mΩ)	Isat (A)	Inom (A)
BUCK1, BUCK2,	Murata	DFE252010P-R47M=P2	0.47	2.50 mm x 2.00 mm	35	5.0	3.5

Table 3. Tested inductor list*...continued*

BUCK	Vendor	Part Number	Inductance (µH)	Size (mm)	DCR (mΩ)	Isat (A)	Inom (A)
BUCK3, BUCK4.	Murata	DFE21CCNR47MELL	0.47	2.00 mm x 1.2 mm	29	4.8	4.1

4.2.2 Output capacitor selection for BUCK converters

The fast-response adaptive constant ON-time control scheme of the BUCK converters implemented in the PF9453HN allows the use of small ceramic capacitors—typically 22 µF—without causing significant output voltage undershoot or overshoot during heavy load transients. Ceramic capacitors with low ESR (Equivalent Series Resistance) values help minimize output voltage ripple. The table below shows the recommended capacitors for a typical use case.

When ceramic output capacitors are used, their RMS ripple current rating generally meets the application requirements. For completeness, the RMS ripple current is calculated using Equation 6.

$$I_{RMS\_COUT} = \Delta I_L \, x \frac{1}{2\sqrt{3}} \tag{6}$$

Where:

- I_{RMS_COUT} = Output capacitor RMS ripple current (A)
- ΔI_L = Peak-to-peak inductor ripple current (A)

At high load currents—where the nominal load current exceeds half of the ripple current (ΔI_L)—the inductor operates in Continuous Conduction Mode (CCM), and the PF9453HN switches to Pulse Width Modulation (PWM) mode. In this mode, the total output voltage ripple is the sum of:

1. The peak voltage caused by the output capacitor's ESR, and
2. The voltage ripple caused by the capacitor's charging and discharging.

Equation 7 provides a good approximation of the output voltage ripple:

$$\Delta Vout \approx \Delta I_L \, x \left(\frac{1}{8 \, x \, Cout \, x \, f} + ESR \right) \tag{7}$$

Where:

- $\Delta Vout$ = BUCK output ripple voltage (V)
- $Cout$ = Output capacitance (F)
- ESR = Equivalent Series Resistance (Ω)
- ΔI_L = Peak to peak inductor ripple current (A)
- f = Switching frequency (Hz)

Table 4. Recommended output capacitors

Ref	Block	Pin	Part number	Impedance |z| (Ω) at 2Mhz.	Size [mm]	Value
C2	BUCK	BUCK1 Output	GRM158C80G226ME	6.0mΩ	1005	22 µF
C4	BUCK	BUCK2 Output	GRM158C80G226ME	6.0mΩ	1005	22 µF
C6	BUCK	BUCK3 Output	GRM158C80G226ME	6.0mΩ	1005	22 µF
C8, C20	BUCK	BUCK4 Output	GRM158C80G226ME	6.0mΩ	1005	22 µF x 2

The highest output voltage ripple occurs at the highest input voltage (V_{IN}).

At low load currents—where the nominal current is less than half of the ripple current—the PF9453HN operates in Pulse Frequency Modulation (PFM) mode. In this mode, the output voltage ripple depends primarily on the output capacitance. For more details on ripple behavior in this mode, refer to the section Expected ripple in DCM mode.

4.2.3 Expected ripple in DCM mode

When the BUCK converter operates in Discontinuous Conduction Mode (DCM), the expected output voltage ripple can be estimated using Equation 8.

$$\Delta Vout \approx \frac{1}{Cout \times 2} \times \left(\frac{Vin\_max - Vout}{L} \times \frac{Vout}{Vin\_max \times f} - ILoad \right) \times \left(\frac{1}{f} - \frac{Iload \times L}{Vin\_max - Vout} - \frac{Iload \times L}{Vout} \right) + ESR \left(\frac{Vin\_max - Vout}{L} \times \frac{Vout}{Vin\_max \times f} \right) \quad (8)$$

Where:

- Cout = Output capacitance (F).
- Vout = BUCK output voltage (V).
- Vin_max = Maximum BUCK Input voltage (V).
- ESR = Equivalent Series Resistance (Ω).
- L = Inductance (H).
- ILoad = Nominal output current (A)
- f = Switching frequency (Hz).

Note: *The largest ripple occurs when the nominal output current approaches zero and the input voltage approaches its maximum value.*

4.2.4 Input capacitor selection for BUCK converters.

A low-ESR input capacitor is highly recommended for optimal input voltage filtering and to minimize interference with other circuits caused by high input voltage spikes—an inherent characteristic of BUCK converters. Each DC-DC converter requires a 10 µF ceramic input capacitor on its input pins. The input capacitance can be increased without limitation to further improve input voltage filtering.

See Table 5 for recommended input capacitors.

Table 5. Recommended input capacitors

Ref	Block	Pin	Part number	Size [mm]	Value
C1, C3	BUCK1 and BUCK2	INB12	GRM188R60J106ME	1608	10 µF x 2
C5, C7	BUCK3 and BUCK4	INB34	GRM188R60J106ME	1608	10 µF x 2

4.3 Recommended capacitors for PF9453HN internal power and load switch pins

To ensure stable operation and minimize noise, the internal power input (VSYS), internal power supply output (VINT), and load switch pins (LSWIN and LSWOUT) must each be bypassed with low-ESR ceramic capacitors. The table below lists the recommended capacitor values and part numbers for these critical pins:

Table 6. Recommended capacitors for internal power and load switch pins

Ref	Block	Pin	Part number	Size [mm]	Value
C10	VINT	VINT	GRM155R61C105KA	1005	1 µF
C11	VSYS	VSYS	GRM155R61C105KA	1005	1 µF

Table 6. Recommended capacitors for internal power and load switch pins...*continued*

Ref	Block	Pin	Part number	Size [mm]	Value
C9	LSW	LSWIN	GRM155R61C105KA	1005	1 µF
C17	LSW	LSWOUT	GRM155R61C105KA	1005	1 µF

Each of these capacitors should be placed as close as possible to the corresponding pin to maximize effectiveness

4.4 Recommended capacitors for LDO input and output pins

All input and output pins of the LDOs must be bypassed with low-ESR ceramic capacitors to ensure stable voltage regulation and minimize output noise. Table 7 lists the recommended capacitor values and part numbers for each LDO pin.

Table 7. Recommended LDO capacitors

Ref	Block	Pin	Part number	Size [mm]	Value
C13, C14	LDO1 input	INL1	GRM155R60J475ME	1005	4.7 µF x 2
C15, C16	LDO1 output	LDO1	GRM155R60J475ME	1005	4.7 µF x 2
C17	LDO2 input	INL2	GRM155R60J475ME	1005	4.7 µF
C18	LDO2 output	LDO2	GRM155R60J475ME	1005	4.7 µF
C12	LDO_SNVS output	LDO_SNVS	GRM155R61C225KE	1005	2.2 µF

4.5 Crystal driver components selection

The crystal oscillator circuit (see Figure 2) uses two load capacitors, CL1 and CL2, which, together with the crystal's internal inductance, provide the necessary 180° phase shift for the feedback loop.

From the crystal's perspective, these capacitors are effectively in series through ground. Therefore, when using two identical capacitors, each must have a value that is twice the required load capacitance of the crystal. It's also important to account for PCB parasitic capacitance when calculating the appropriate capacitor values, as shown in Equation 9.

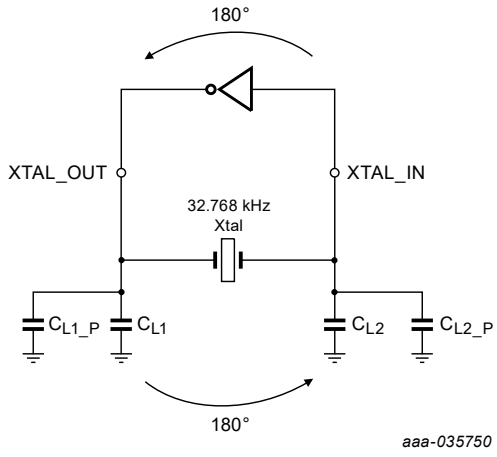


Figure 2. Crystal oscillator circuit

$$C_{Load} = \frac{C'_{L1} \, x \, C'_{L2}}{C'_{L1} + C'_{L2}} \quad (9)$$

Where:

1. $C'_{L1} = C_{L1} + C_{L1\_P}$ *where* CL1_P is PCB parasitic capacitance.
2. $C'_{L2} = C_{L2} + C_{L2\_P}$ *where* CL2_P is PCB parasitic capacitance.

When using equal capacitors for C_{L1} and C_{L2} and a symmetric layout with equal parasitic capacitance on both crystal pins, the effective load capacitance is shown in Equation 10.

$$C_{Load} = \frac{C_{L1} + C_{L1_P}}{2} \quad (10)$$

Example:

If the crystal requires a 12.5 pF load and the estimated parasitic capacitance is 7 pF per pin, the required capacitor value can be calculated accordingly:

$$C_{L1} = 2\,x\,C_{Load} - C_{L1\_P} = \left(2\,x\,12.5pf\right) - 7pf = 18pf$$

$$C_{L2} = C_{L1} = 18pf$$

Table 8 lists the recommended components for the crystal driver circuit.

Table 8. Recommended components for crystal

Ref	Block	Pin	Part number	Size [mm]	Value
C18	XTAL	XTAL_IN	GCM1555C1H180JA16	1005	18 pF
C19	XTAL	XTAL_OUT	GCM1555C1H180JA16	1005	18 pF
Y1	XTAL	XTAL_IN and XTAL_OUT	ABS07-32.768KHZ-T	3.2 mm x 1.5 mm	32.768 kHz

5 Layout design guidelines

5.1 Placement

All power stage components should be placed as close as possible to the PMIC, with particular emphasis on input and output decoupling capacitors. To ensure optimal performance and minimal noise, follow this placement priority:

1. INB12 and INB34 vias – Position these directly adjacent to the PMIC for efficient power delivery.
2. Input capacitors for the BUCK regulators – Place as close as possible to the corresponding input pins.
3. Switching regulator inductors – Locate next to the BUCK outputs to minimize loop area.
4. VSYS and VINT capacitors – Position near their respective output pins.
5. LDO_SNVS, LDO1, and LDO2 capacitors – Place close to their associated LDO outputs.
6. Crystal and associated passive components – Mount near the PMIC's crystal pins with short, symmetrical traces.
7. Load switch capacitors – Place near the output of the load switches.

Refer to Figure 3 for detailed guidance.

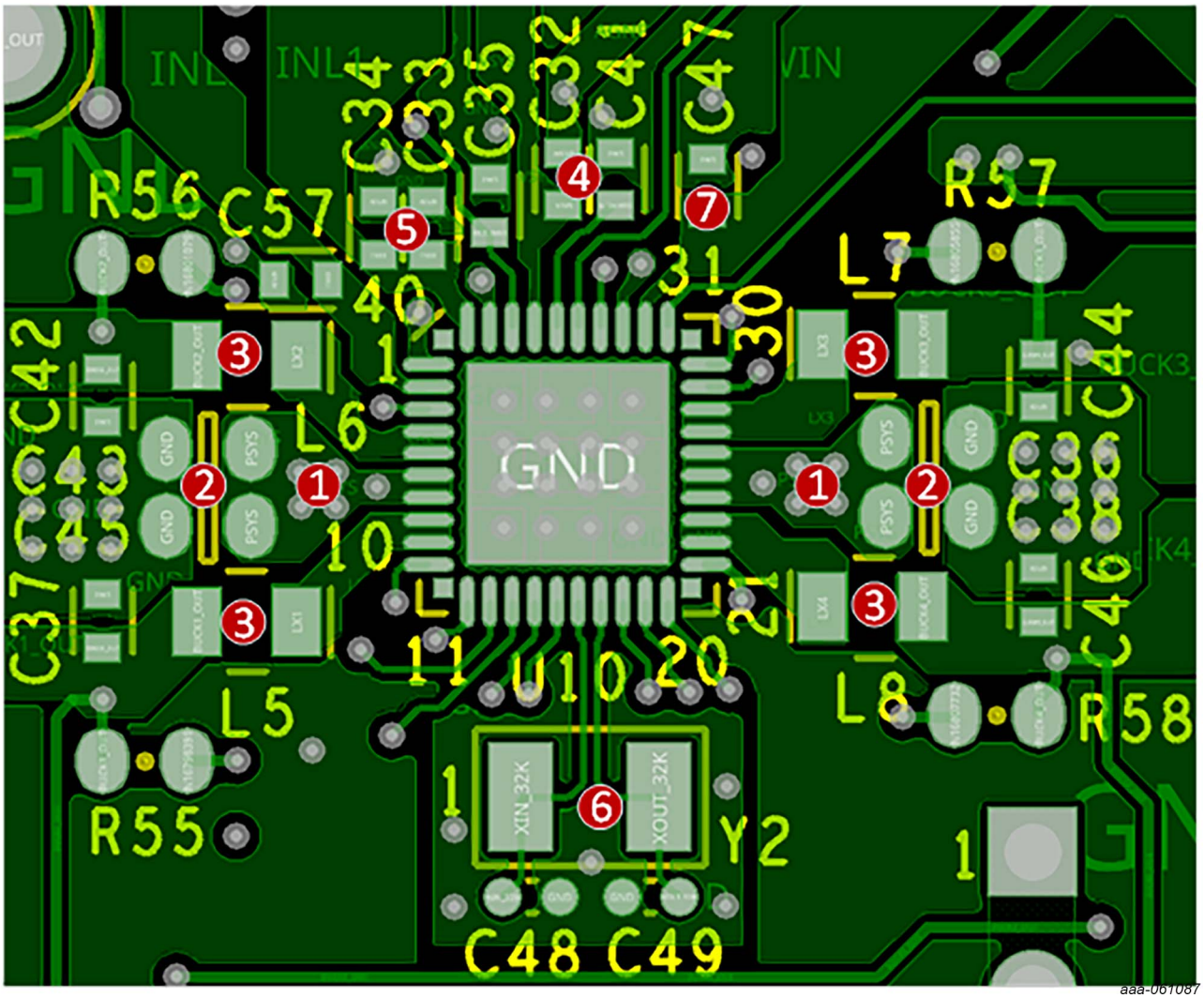


Figure 3. PF9453HN PCB layout example

5.2 General routing guidelines

The recommended PCB stack-up for this PMIC consists of four layers:

1. Top signal/power layer
2. Ground plane
3. Power layer
4. Bottom signal layer

Grounding:

- Use a star grounding approach for the AGND signal, which serves as the return path for the VSYS network. Refer to Section 5.5 for more information.
- The exposed pad (EP) on the PF9455 QFN package is the main high-current ground return for all BUCK regulators. Place multiple vias directly under the EP to connect to the ground plane, ensuring low impedance and adequate copper area.

High-speed and high-current nodes:

- INBxx and LXx nodes carry high current and have high dI/dt characteristics, making them potential sources of EMI. Keep these traces short and wide to reduce inductance and radiated noise.
- Minimize and isolate high dv/dt LXx node areas to reduce EMI emissions.

Feedback and control:

- The control loop regulates the output voltage at the point where the feedback trace connects to the output rail. For optimal load regulation, connect the feedback trace close to the load and route it away from noisy signals or layers to avoid interference.

Power routing:

- Place all power components on the same side of the board, and route their power traces on the same layer to minimize voltage drops.
- If routing power traces between layers is necessary, do so only in low di/dt paths and use multiple vias to reduce impedance and noise coupling.

5.3 I2C, crystal and IO signals

To prevent interference from nearby high-power or high-frequency signals, it is recommended to shield critical signal traces using ground planes placed on adjacent PCB layers. Ensure that the ground plane remains continuous and uniform along the entire length of the signal trace.

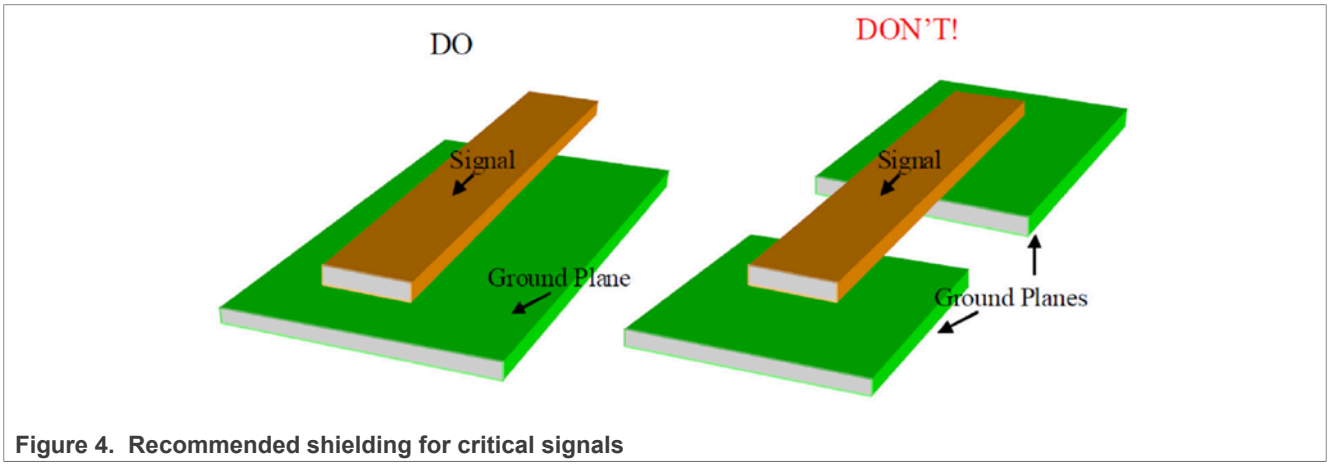


Figure 4. Recommended shielding for critical signals

5.4 BUCK regulators

In a BUCK converter configuration, the length of the critical traces must be kept to a minimum. Critical traces refer to current paths with high dI/dt.

Figure 5 illustrates the current paths in a BUCK converter during the ON and OFF periods of the switching cycle. These critical traces are those that conduct only during either the ON or the OFF period, as highlighted in red.

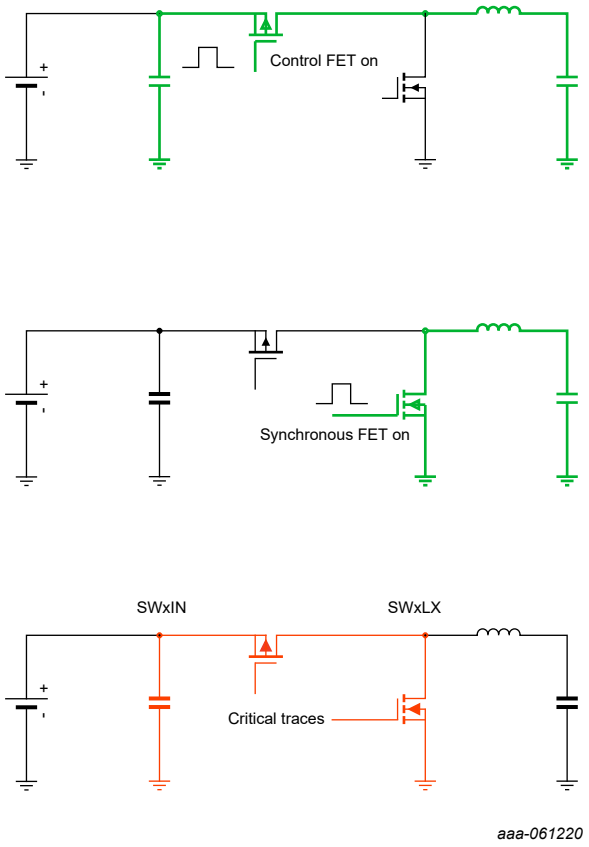


Figure 5. BUCK converter critical traces

In the PF9453HN BUCK regulators, both the high-side and low-side MOSFETs are integrated within the package. Therefore, it is crucial to place the input capacitor as close as possible to the INBxx input pin and the ground.

Figure 6 provides an example schematic of the BUCK regulator configuration.

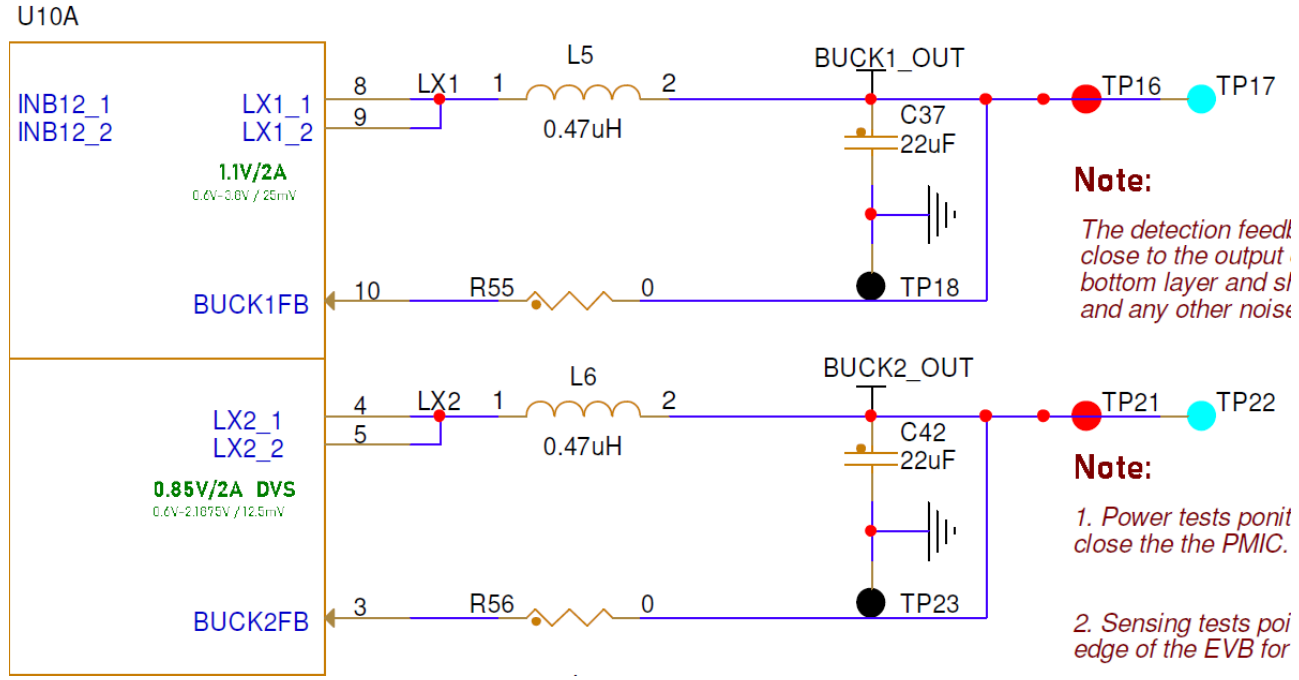


Figure 6. PF9453HN QFN BUCK1 and BUCK2 schematic

Figure 7 shows an example of layout for the BUCK regulators.

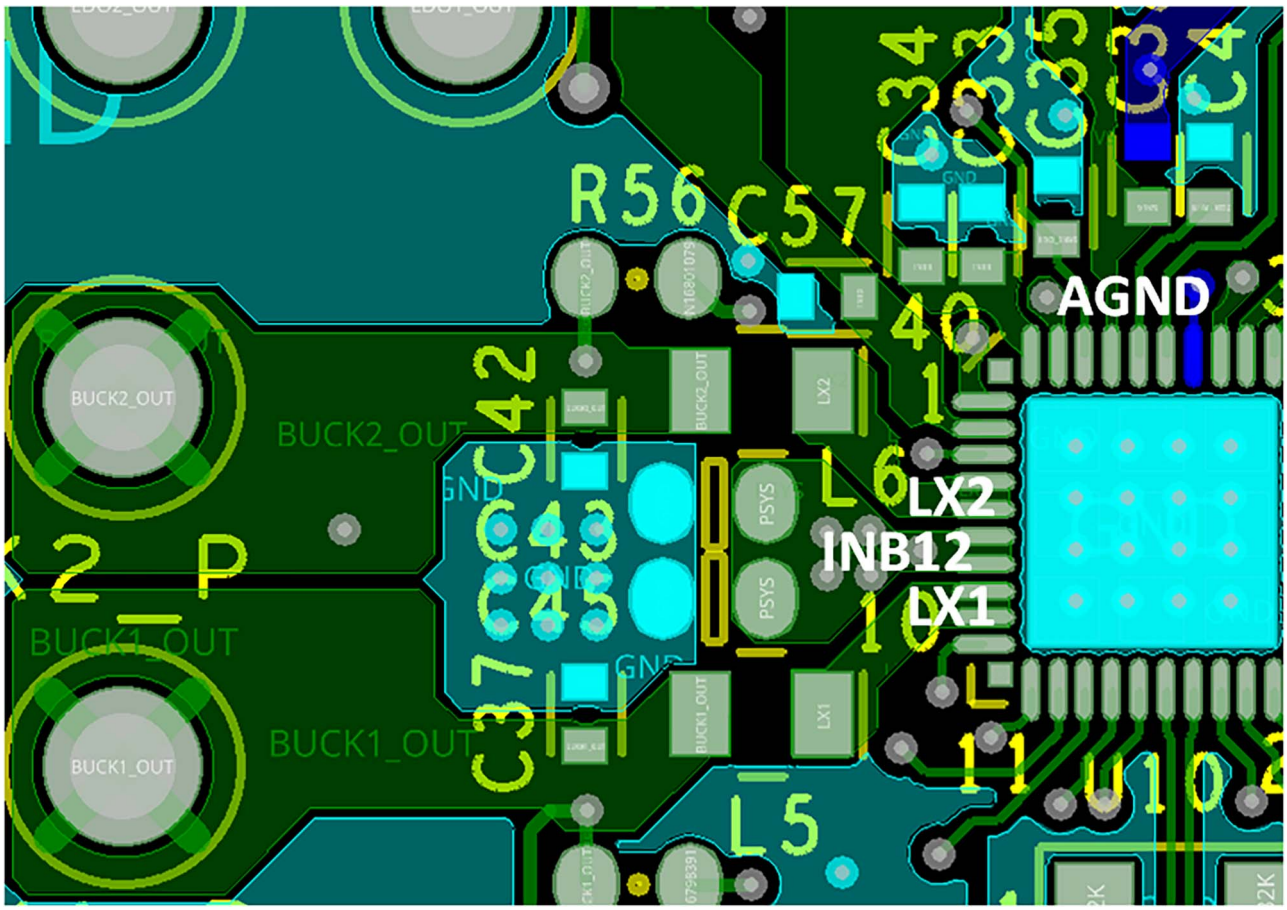


Figure 7. PF9453HN BUCK1 and BUCK2 layout top layer

5.5 Effective grounding

For optimal performance of the PF9453HN, the use of star grounding is essential.

The exposed pad (EP) serves as the ground return (PGND) for all switching regulators and should be connected to the ground plane using multiple vias to ensure a low-impedance path. (See Figure 8 and Figure 9.)

Pin 34 (AGND) is the signal ground and must be routed carefully to avoid coupling with high-current return paths. The following examples illustrate two effective star grounding implementations:

- Example 1:
  The AGND net (shown in dark blue) is completely isolated from the ground plane on the second layer. It connects directly to the ground pins of the input connector capacitors, maintaining a clean signal ground path.
- Example 2:
  The AGND pin is connected to the ground plane on the second layer through a dedicated via. It is not connected through the EP, which helps prevent noise coupling from the switching regulator return currents that flow through the EP.

Refer to Figure 8 and Figure 9 for visual reference.

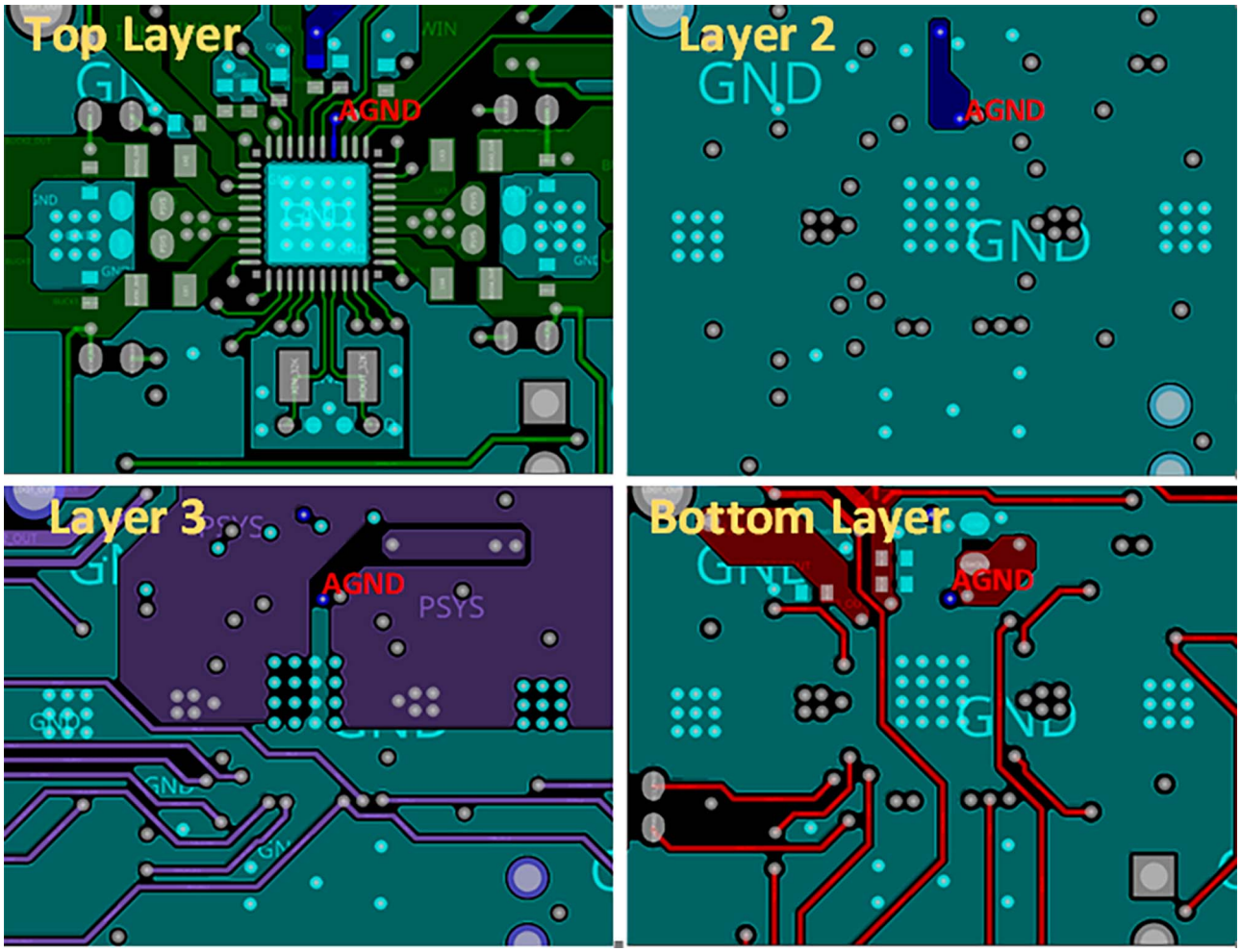


Figure 8. PF9453HN layout example 1

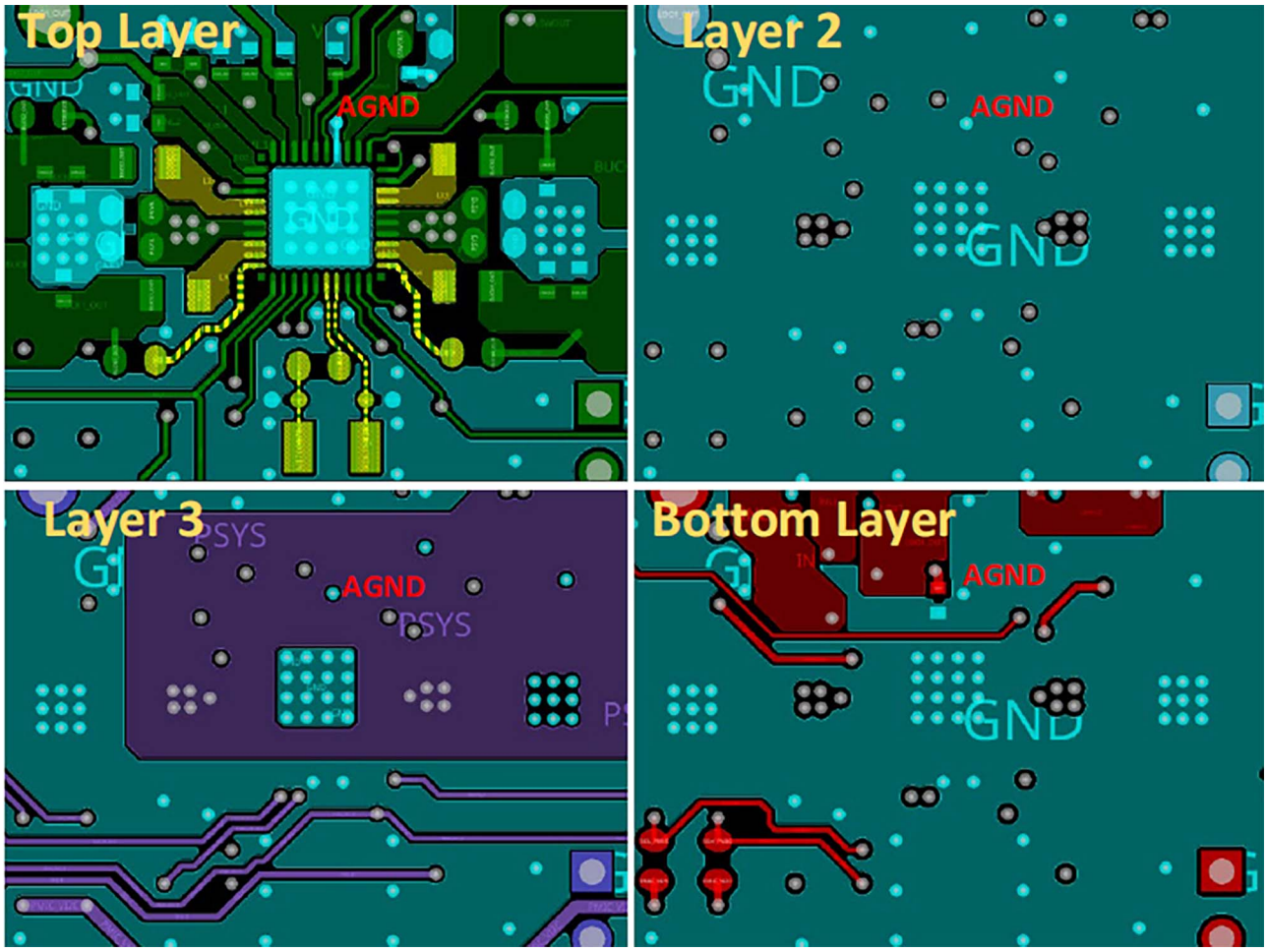


Figure 9. PF9453HN layout example 2

6 Revision history

Table 9. Revision history

Document ID	Release date	Description
AN14685 v.1.0	9 June 2025	• Initial version

Legal information

Definitions

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