AN14684

Features, Usage, and Capabilities of Smart Power Switch on the KW47 Microcontroller

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Document information

Information	Content
Keywords	AN14684, KW47 microcontrollers, KW47-EVK smart power switch, fast wake-up from smart power switch
Abstract	This application note describes the use of the smart power switch in the KW47 microcontroller.

1 Introduction

This application note describes the use of the smart power switch in the KW47 microcontroller. The KW47 integrates a programmable solid-state switch that turns connected components on or off, including KW47 power domains.

The switch enables ultralow power consumption applications on KW47 when it directly controls the KW47 power domain supply.

The smart power switch also includes embedded hardware powered by an independent power domain VDD_SWITCH. This hardware provides enhanced features that meet diverse KW47 MCU application requirements.

2 KW47 power domains

The KW47 microcontroller has independent power domains, grouped as follows:

- VDD-SWITCH: Represents the input voltage for the smart power switch (VBAT). This power domain supplies the voltage to the internal hardware associated with the VBAT.
- VDD-ANA: Drives the analog peripherals on this microcontroller, including the Analog-to-Digital Converter (ADC) and the VREF regulator.
- VDD-IO-ABC: Supplies the voltage on the PTA, PTB, and PTC pins.
- VDD-IO-D or VDD-DCDC: Provides the voltage to the PTD pins, including the reset system. It also serves as the input for the DC-DC Buck converter and the input for the Low Dropout Regulator (LDO)-SYS regulator.
- VDD-SYS: Manages the power delivery to some peripherals on this chip. Refer to Table 1 for the list of peripherals supplied by this domain.
- VDD-CORE: Supplies power to the main core processor and some peripherals on this chip. This power domain is divided into core main, core wake, and core radio domains for an independent power mode selection. The voltage of this power domain is associated with the maximum clocking frequency at which the device can operate. Refer to Table 1 for the list of peripherals supplied by this domain.
- VDD-RF: Provides the voltage that drives the radio analog system on this chip, and the 32 MHz oscillator (OSC).
- VDPA-2P4GHZ: Drives voltage for the radio power amplifier. The VDD-RF power domain can provide the VDPA-2P4GHZ voltage internally.

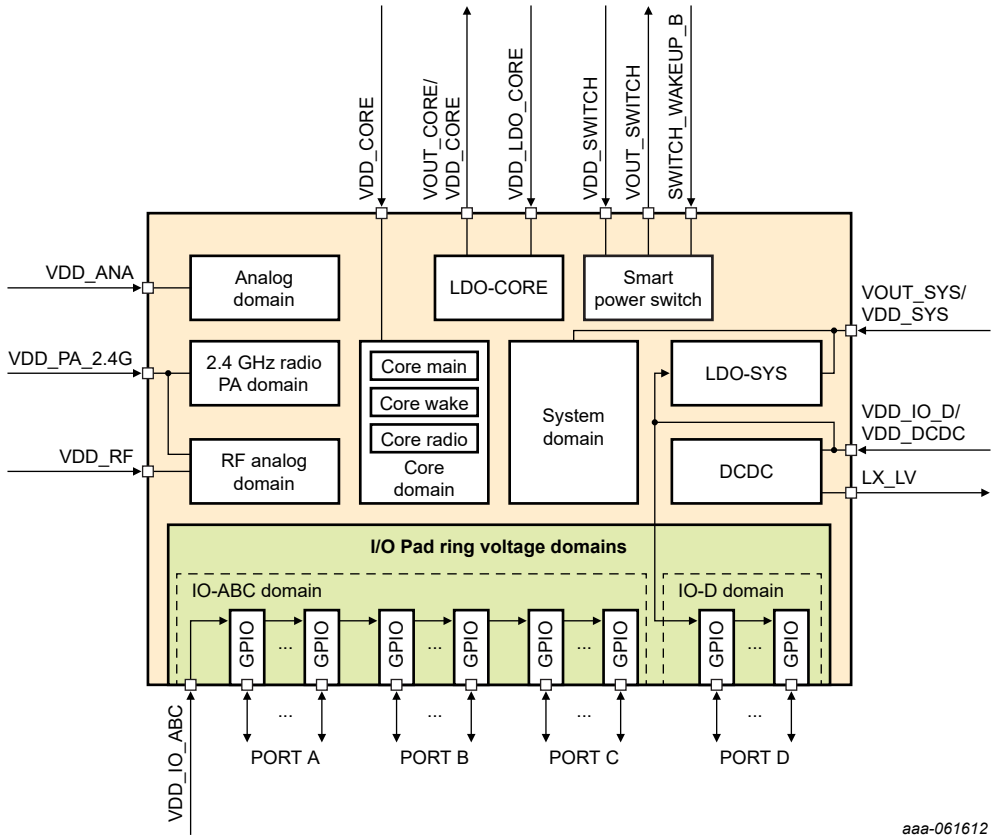


Figure 1. KW47 power domain block diagram

2.1 Peripherals supplied by each power domain

The KW47 power domains supply their associated on-chip peripherals as listed in Table 1.

Table 1. Peripheral power domain assignments

Power domain	Voltage supply	Modules associated with the power domain
Analog domain	VDD_ANA VSS_ANA	ADC0 VREF0
Core main	VDD_CORE_MAIN (Tied internally to VDD_CORE pin)	CM33, DSP, FPU, MPU, NVIC, SYSTICK, TZM, DAP, DWT, ITM, TPIU, AXBS0, eDMA0, MSCM, SMSCM, PRBRIGDE2, TRGMUX, MRCC, SFA0, CACHE-CODE, FLASH, ROM, BOOT, CRC0, EdgeLock Secure Enclave, TRDC0, LPIT0, TPM1, FlexCAN0, FlexIO0, LPI2C 1, I3C0, LPSPI 1, LPUART 1, GPIOB/C, SEMA42, PORTB/C, ADC0, VREF0, and TCM-SYS
Core wake	VDD_CORE_WAKE (Tied internally to VDD_CORE pin)	SWD, CMC0, EWM0, WDOG0/1, FRO-6M, MRCC, SCG0, TSTMR0, TPM0, LPI2C0, LPUART0, LPSPI0, GPIOA, PORTA, and LPCMP0/1
Core radio	VVD_CORE_2.4G (Tied internally to	RF-2.4G, NBU, RF-FMU, RF-FRO192M, TPM2, LPUART2

Table 1. Peripheral power domain assignments*...continued*

Power domain	Voltage supply	Modules associated with the power domain
	VDD_CORE pin)	
IO-ABC	VDD_IO_ABC	PORTA, PORTB, PORTC, LPCMP0/1
IO-D	VDD_IO_D	LDO-SYS, DC-DC, PORTD
Smart power switch	VDD_SWITCH	Power switch, RAM LDO, FRO16K, power switch controller
System	VDD_SYS	RFMC0, Bluetooth LE LL (from NBU), WUU0, FRO192M, LPTMR0/1, SPC0, OSC-RTC, FRO32K, REGFILE0/1 – RTC, TAMPER, RTC0, GPIOD, PORTD
RF analog	VDD_RF	OSC-RF, RF-2.4G
2.4 GHz Radio PA	VPA_2.4G	RF-PA-2.4G

2.2 Power domain rates

Table 2 shows the maximum and minimum Direct Current (DC) voltage requirements for each power domain in KW47 MCUs.

Table 2. Power domain rates

Power domain	Voltage supply	Minimum	Maximum	Unit
Core domain	VDD_CORE Mid Drive (1.05 V) Normal Drive (1.1 V) Safe-Mode (1.15 V)	1.0 1.04 1.04	1.1 1.21 1.21	V V V
System domain	VDD_SYS - Normal mode - Fuse programming	1.8 2.25	1.98 2.75	V V
IO-ABC domain	VDD_IO_ABC	1.71	3.6	V
IO-D domain	VDD_IO_D	1.86	3.6	V
Smart power switch	VDD_SWITCH	1.9	3.6	V
RF analog domain	VDD_RF	1.175	3.6	V
2.4 GHz Radio PA	VPA_2.4G	0.9	2.4	V
Analog domain	VDD_ANA	1.71	3.6	V

3 KW47 power configurations

The KW47 microcontroller supports independent power domains, allowing multiple power configuration options. Any power configuration can be implemented by setting the required voltage on each power domain according to the application requirement. Ensure that the chosen power configuration complies with the requirements described in Section 2.2.

The subsections that follow present common power configurations, their advantages, and considerations.

3.1 KW47 LDO mode configuration

In LDO mode, the KW47 disables the DC-DC converter and directly connects each power domain to a unique power supply. This configuration uses the low-cost hardware implementation due to the small number of external components required.

However, this configuration prevents independent voltage levels for each power domain. Therefore, it leads to the highest power consumption.

In this configuration, it is recommended to:

- Disable the DC-DC by clearing the CNTRL[DCDC_EN] bit in the SPC module (set it to 0).
- Tie the DC-DC output to GND through a 10 kΩ resistor.

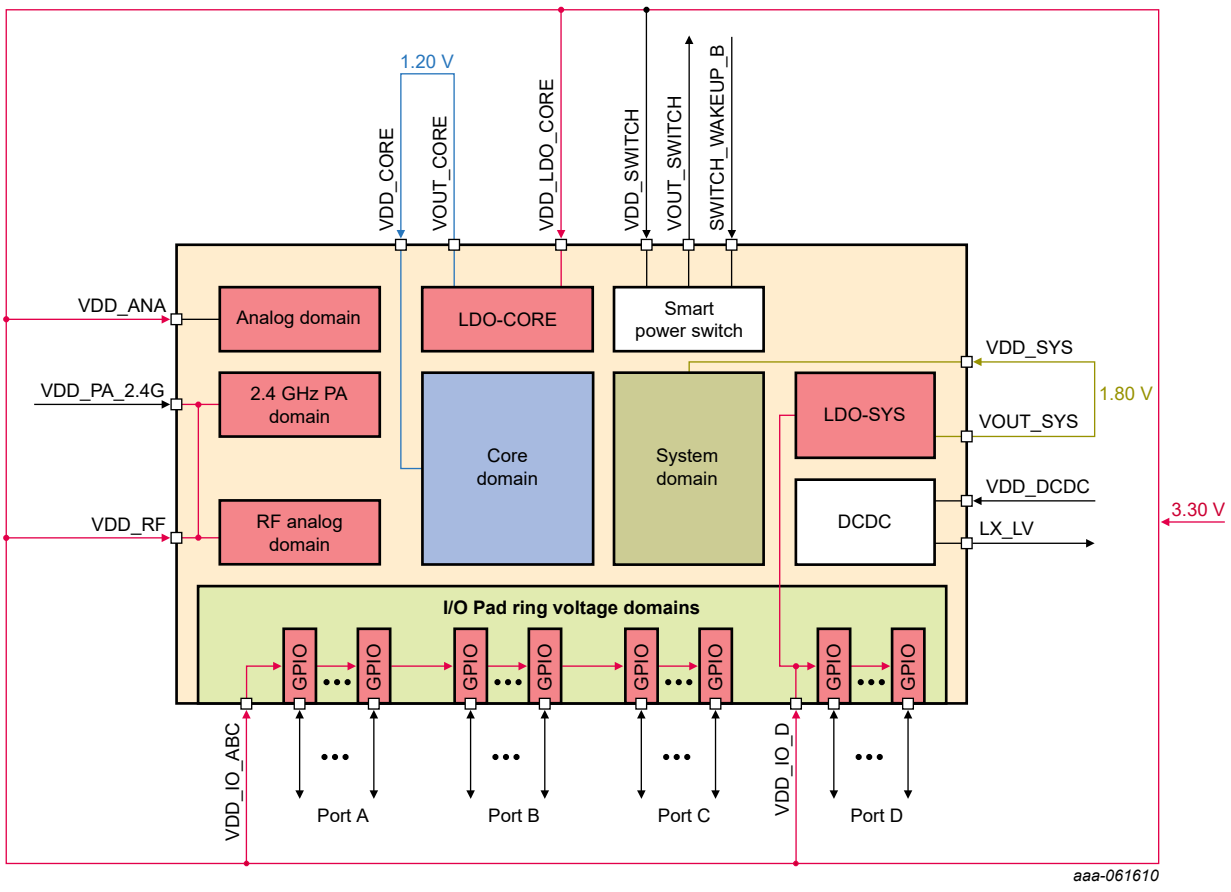


Figure 2. KW47 LDO mode configuration

3.2 KW47 DC-DC Buck configuration

The DC-DC Buck mode configuration balances power consumption and cost optimally, making it a common configuration.

A single power supply in the DC-DC Buck mode powers multiple domains, including the DC-DC input. The DC-DC output supplies configurable voltage to the Radio Frequency (RF) domain and LDO-CORE. The DC-DC output delivers voltage to the RF power domain for achieving up to +10 dBm TX output power. Decreasing the DC-DC output voltage saves power when the RF domain remains idle. The DC-DC can also be used to feed external circuitry.

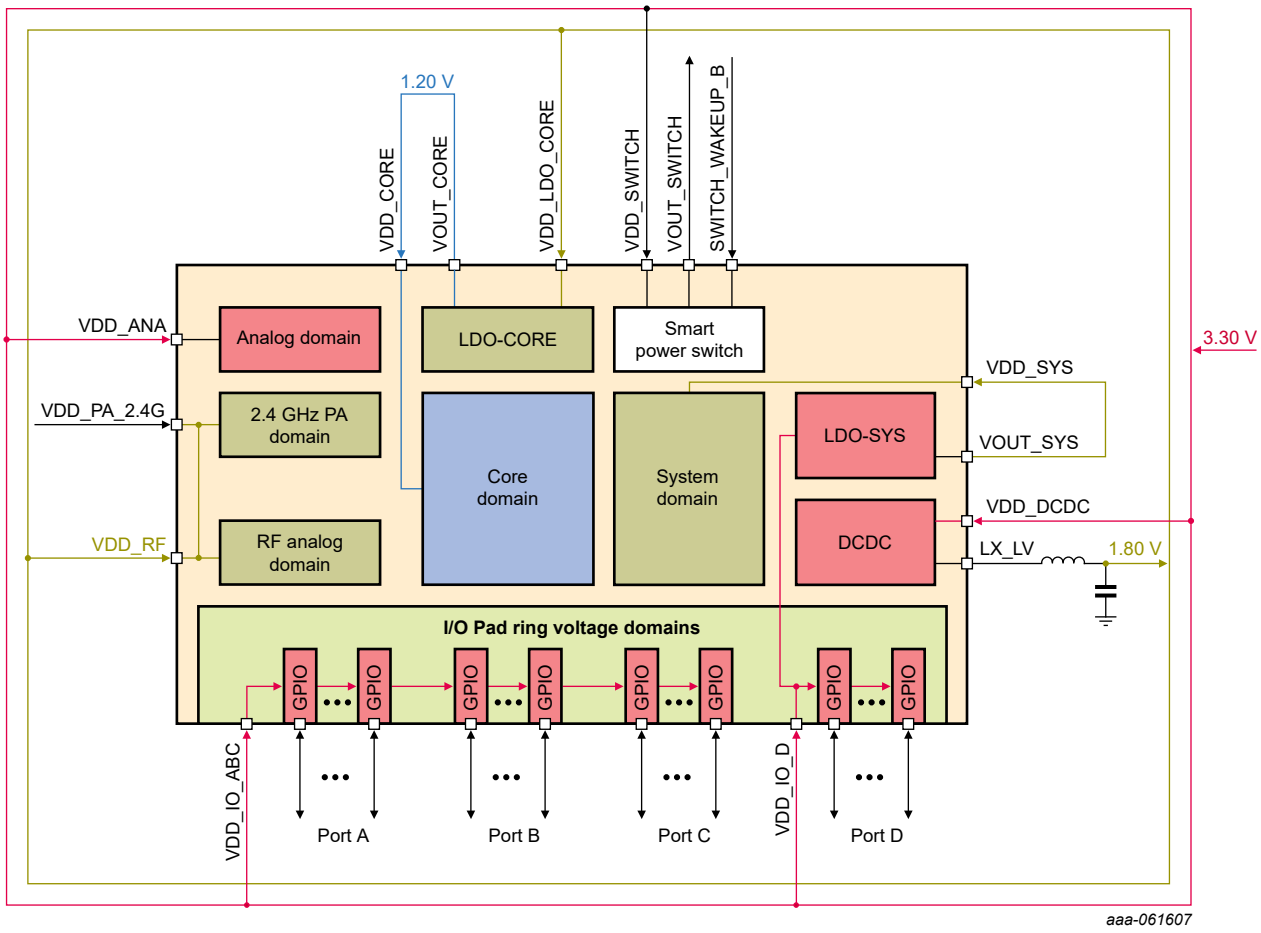


Figure 3. KW47 DC-DC Buck mode configuration

3.3 KW47 smart power switch configurations

The smart power switch (VBAT) is a low-resistance solid-state switch. It works with the power management system to implement power-saving mechanisms. It also provides two band gap timers and an LDO voltage regulator dedicated to supply the retention Static Random Access Memory (SRAM) while the rest of the MCU remains switched off.

The smart power switch can turn off all MCUs or selected power domains with the smart power switch to optimize power consumption. The smart power switch provides two band gap timers and an LDO voltage regulator. This regulator supplies the retention SRAM while the rest of the MCU remains off. SRAM retention during the switch-off state is configurable. The software can disable the smart power switch and enable it by using either the VBAT band gap timers or a falling edge on the SWITCH_WAKEUP_B pin.

Figure 4, Figure 5, and Figure 6 show typical smart power switch configurations.

- The external 3.3 V power source supplies the smart power switch. Its output is connected to the DC-DC, LDO-SYS, VDD_ANA, VDD_IO_D, and VDD_IO_ABC. The DC-DC output is connected to the LDO-CORE and VDD_RF.

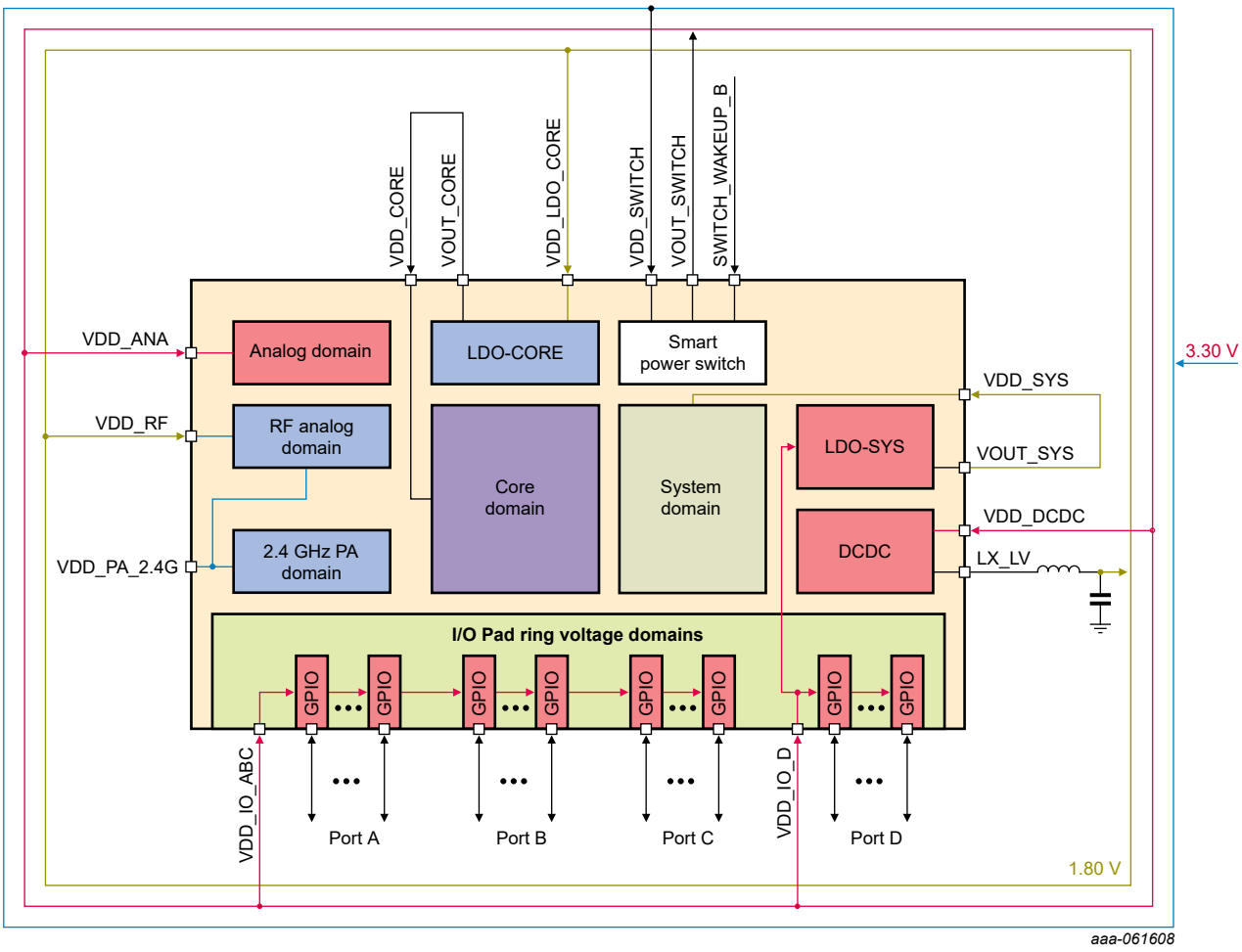


Figure 4. KW47 DC-DC mode, power all domains with smart power switch

- The external 3.3 V power source supplies the smart power switch and VDD_DCDC or VDD_IO_D. The smart power switch output is connected to VDD_ANA and VDD_IO_ABC. The DC-DC output is connected to the LDO-CORE and VDD_RF.

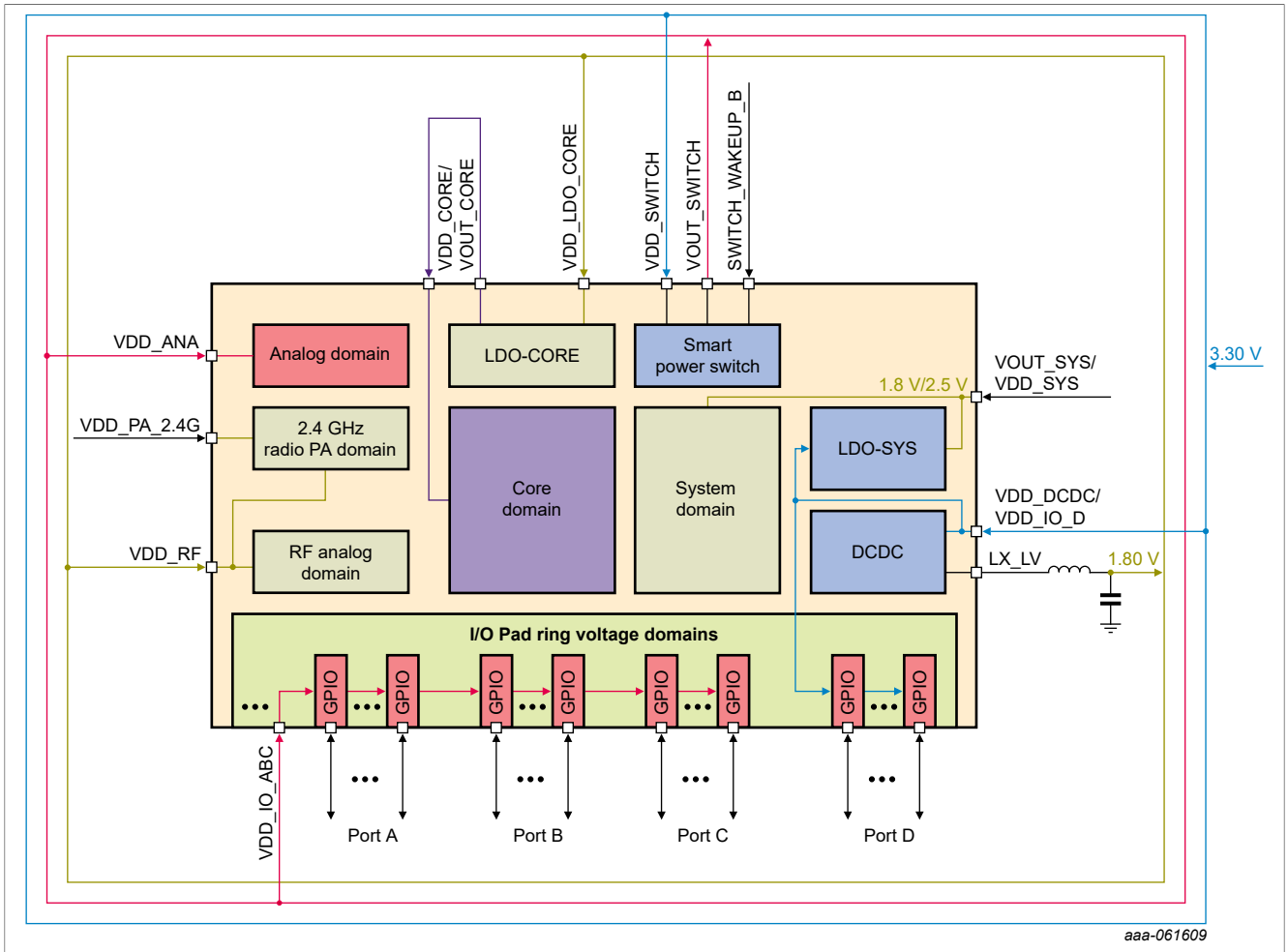


Figure 5. KW47 DC-DC mode, power all domains with smart power switch except VDD_IO_D and VDD_DCDC

- The external 3.3 V power source supplies the smart power switch. Its output is connected to the DC-DC, LDO-SYS, VDD_ANA, VDD_IO_D, LDO-CORE, and VDD_IO_ABC. In this configuration, it is recommended to disable the DC-DC.

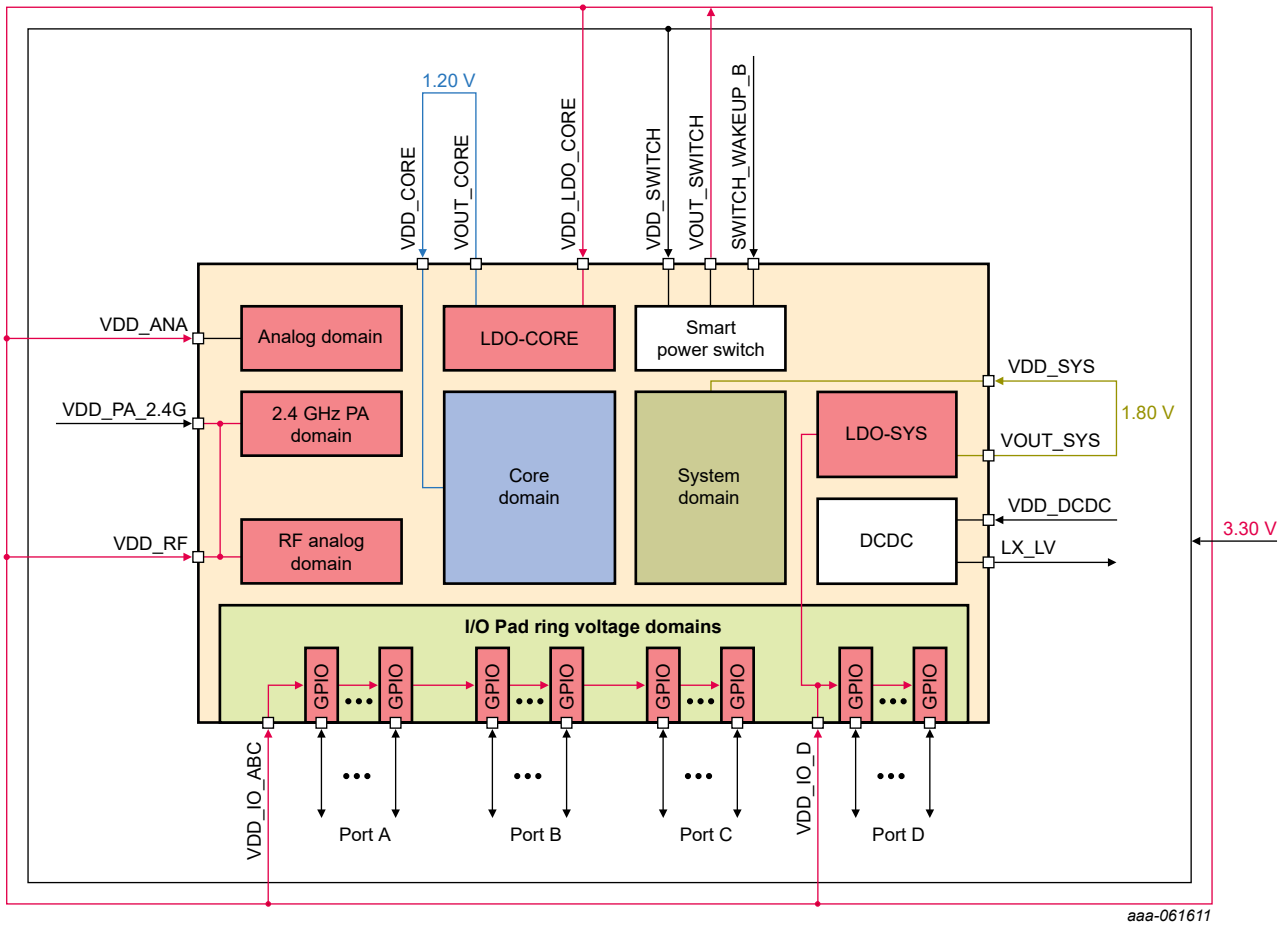


Figure 6. KW47 LDO mode, power all domains with smart power switch

4 Smart power switch

The smart power switch (VBAT) is a low-resistance switch. It works with the power management system to implement power-saving mechanisms. It switches off all or specific power domains to achieve ultralow power consumption.

However, avoid using the smart power switch continuously when the KW47 runs from a battery with peak current limitation requirements. The DC-DC converter creates a high inrush current during startup, which can shorten battery life. NXP recommends using the smart power switch for use cases in which the system is expected to remain powered off for extended periods of time.

The smart power switch is able to control power distribution to external board loads. This is true as long as load and voltages meet specifications. Refer to the Section 3 for typical smart power switch configurations.

Figure 7 shows the smart power switch architecture in the KW47 MCU.

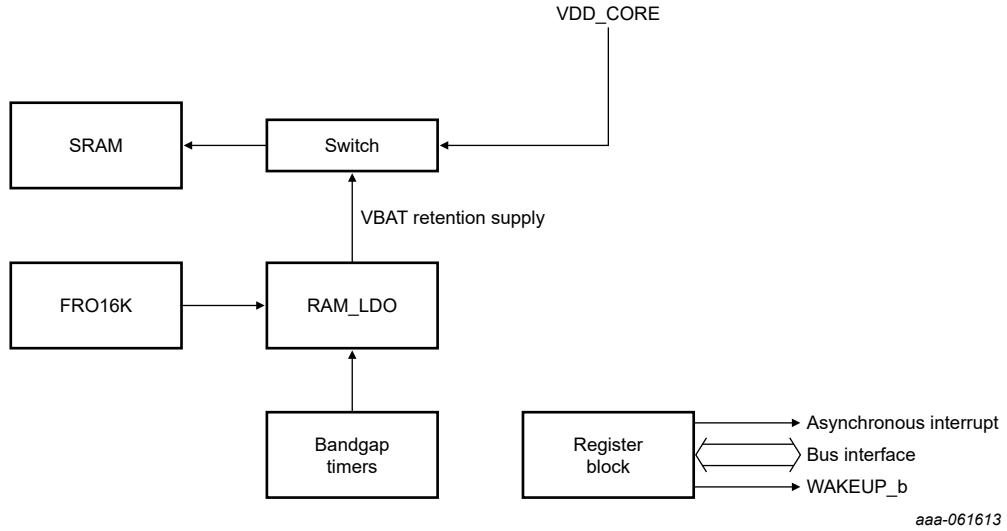


Figure 7. Smart power switch block diagram

4.1 Smart power switch hardware

The smart power switch performs the primary function of switching loads on or off. The switch also incorporates embedded hardware. The independent power domain VDD_SWITCH powers this hardware. This setup provides features that meet KW47 MCU application requirements.

The subsections that follow detail the smart power switch hardware and the available capabilities.

4.1.1 VBAT FRO16K and band gap timers

The smart power switch includes an internal 16.384 kHz oscillator, supplied by the VDD_SWITCH power domain, known as the VBAT FRO16K oscillator. This oscillator can remain active in all low-power modes. Although FRO16K is primarily used by the VBAT, some other peripherals in KW47 can also use it. For more information on this feature, refer to the *KW47 Reference Manual* (document KW47RM).

In addition to the FRO16K oscillator, the smart power switch includes two band gap timers:

- Band gap timer 0
- Band gap timer 1

Both timers use the FRO16K as their reference clock to determine their counter value and are also powered by the VDD_SWITCH power domain. These timers can be used to turn on the smart power switch when their countdown expires. This functionality allows the system to be programmed to power off for a specified duration and automatically power back on after the timer expires.

In the KW47 MCU, the timer configuration ranges:

- Band gap Timer 0: Timeout ranges from 7.8125 ms to 1 second
- Band gap Timer 1: Timeout ranges from 1 second to 16,777,216 seconds

Prerequisites for timer operation:

1. Enable the FRO16K oscillator by setting FROCTLA[FRO_EN] to 1 in the VBAT domain.
2. Enable the LDO Random Access Memory (RAM) band gap bit by setting LDOCTLA[BG_EN] to 1 in the VBAT domain.

It is important to note that writing bit LDOCTLA[BG_EN] to 1 in the VBAT domain, which is required for band gap timers, also enables LDO RAM and sets the STATUSA[LDO_RDY] bit in VBAT. If LDO_RAM is not

supplying the System Tightly Coupled Memory 8 (STCM8) SRAM array, this can lead to increased power consumption. Therefore, it is recommended to use band gap timers to control the power on functionality only when the STCM8 SRAM content retention feature is enabled.

For more information on SRAM retention feature, refer to the Section 4.1.2.

4.1.2 VBAT LDO RAM retention and SRAM retention array

When the smart power switch controls all power domains, it is expected that the application running on the device resets the execution when the smart power switch turns off and on. This interruption can possibly result in the loss of application context due to the loss of power on the system. To address this use case, the smart power switch includes an LDO RAM that can supply an 8 kB SRAM array dedicated to retain the application data when the VBAT is turned off. This feature enables the system to recover the data quickly after the Power-on Reset (POR) sequence when the smart power switch powers the system back on.

In general, the LDO RAM retention regulator can be used to maintain power to the SRAM retention at any time, including during low-power modes, to preserve application data. However, all access to the SRAM retention address range is not allowed while the LDO RAM is powering this memory. Any attempt to access this memory during that time triggers a fault condition. The 8 kB SRAM retention array is mapped to the address range from 0x2003_8000 – 0x2003_9FFF, which corresponds to the STCM8 in KW47 device. The STCM8 supports Error Correction Code (ECC) in KW47 devices.

4.1.2.1 VBAT LDO RAM enable sequence

To enable the VBAT LDO RAM retention regulator, follow the steps below:

1. Enable the VBAT FRO16K oscillator by setting FROCTLA[FRO_EN] to 1 in the VBAT domain.
2. Enable the LDO RAM band gap bit by setting LDOCTLA[BG_EN] to 1 in the VBAT domain.
3. For the lowest power consumption, set the LDO RAM in low-power refresh mode by enabling the following bit: LDOCTLA[LDO_EN] to 1 in the VBAT domain.
4. Enable the LDO RAM regulator by setting LDOCTLA[LDO_EN] to 1 in the VBAT domain.
5. Wait until the LDO_RDY flag is set by polling the STATUSA[LDO_RDY] bit in the VBAT domain.

4.1.2.2 Powering the SRAM retention memory with VBAT LDO RAM regulator

By default, the SRAM retention memory is powered by the VDD_CORE domain. Therefore, if the application requires the use of the memory retention feature, the software must configure the necessary registers to move the SRAM power supply source from the VDD_CORE domain to the VBAT LDO RAM regulator. As explained in Section 4.1.2, any attempt to read or write to the SRAM retention memory while it is supplied by the LDO RAM regulator results in a fault. To avoid this, the application data must be saved in the SRAM address range before switching the memory power supply.

The following steps describe how to configure the VBAT LDO RAM regulator to supply the SRAM retention memory:

1. Enable the VBAT LDO RAM regulator by following the steps described in Section 4.1.2.1.
2. Configure LDORAMC[ISO] = 1 in the VBAT domain.
3. Configure LDORAMC[SWI] = 1 in the VBAT domain.

After the smart power switch turns on, the software must reverse these steps to switch the SRAM memory supply back to the VDD_CORE domain. This allows access to the SRAM retention memory and loads the application context.

1. Configure LDORAMC[SWI] = 0 in the VBAT domain.
2. Configure LDORAMC[ISO] = 0 in the VBAT domain.

4.1.3 Fast wake-up from smart power switch

The KW47 MCU supports fast wake-up after being powered off and back on by the smart power switch. Before the smart power switch turns off, the software can store the application context in a retained 8 kB STCM8 SRAM array. The SRAM address 0x2003_9FF8 is expected to hold a CRC value computed with the first 48 bytes of the application image as input. The address 0x2003_9FFC is expected to hold the application wake-up entry address.

When the smart power switch turns on, the KW47 ROM bootloader switches the SRAM power supply to VDD_CORE, and verifies computed CRC. If the CRC check is successful, the MCU core fetches the value stored in the wake-up entry address (0x2003_9FFC) and uses it as an application entry point. For more information on the KW47 ROM bootloader, refer to the *KW47 Reference Manual* (document KW47RM).

This feature is useful in a scenario where the device must restore its context after all power domains have been shut down. Typically, the wake-up entry address points to a wake-up routine that recovers the device from low-power mode, reinitializes application-required peripherals. It then restores the application context to the state that it was in before the power-down.

Although this is the most common use case, the wake-up entry can point to any arbitrary application image programmed into the device flash memory. This is valid as long as the image is correctly formatted.

For more information on Cortex-M33 application image format, refer to Arm documentation.

4.1.4 Smart power switch on or off control

The smart power switch can be turned on using any of the following four methods:

- POR: After a POR of the smart power switch, the internal wake-up logic automatically enables the smart power switch. The smart power switch POR occurs during a power cycle on the VDD_SWITCH. The POR resets the smart power switch registers to their default state, which is the only way the hardware can reset these values. After the smart power switch POR, by default, the switch output is enabled.
  Note: *The POR of the smart power switch operates independently from the device POR.*
- External wake-up pin: Software can enable the switch to be turned on after a falling edge on the external SWITCH_WAKEUP_B pin (available in KW47). This pin is pulled up internally.
- Programmable timers: Software can configure either of the two band gap timers embedded in the smart power switch. This configuration is done before shutting down the switch to wake up after the programmed time.
- System Power Controller (SPC) register (SPC -> CFG): Sometimes, the SPC can turn on the switch by writing to the SPC -> CFG register. This is applicable only when the smart power switch is not actively controlling the power domains required by the MCU to run in active mode. This allows to turn on or off the switch without shutting down the SPC.

For example, Figure 5 shows a use case where the SPC controls the smart power switch, managing only the VDD_ANA and VDD_IO_ABC power domains. Similarly, the SPC can activate the switch when it is used to control external onboard loads.

Software can only turn off the smart power switch by writing to the corresponding SPC -> CFG register.

The SPC registers can configure independent settings of the smart power switch depending on whether the KW47 is in active mode or enters one of the available low-power modes. Following this principle, it is possible to turn on or off the smart switch when the MCU is running in active mode. Also, it is possible to configure the smart power switch to turn off automatically when the MCU enters a low-power mode, and turn on the smart power switch again when the MCU exits from low-power mode.

The SPC -> CFG register can configure the VBAT enable or disable operation in active and low-power mode as follows:

- SPC -> CFG[INTG_PWSWTCH_WKUP_ACTIVE_EN]: Writing this bit to '1' turns on the smart power switch when the MCU is in active mode. Modifying this bit to '1' or '0' when the MCU is in active mode and the switch is already turned on has no effect.
- SP -> CFG[INTG_PWSWTCH_SLEEP_ACTIVE_EN]: Writing this bit to '1' turns off the smart power switch when the MCU is in active mode. Modifying this bit to '1' or '0' when the MCU is in active mode and the switch is already turned off has no effect.
- SPC -> CFG[INTG_PWSWTCH_WKUP_EN]: Writing this bit to '1' turns on the smart power switch when the MCU exits from any low-power mode.
- SPC -> CFG[INTG_PWSWTCH_SLEEP_EN]: Writing this bit to '1' turns off the smart power switch when the MCU enters to any low-power mode.

Configuration guidelines:

- The application software must not enable both INTG_PWSWTCH_WKUP_ACTIVE_EN and INTG_PWSWTCH_SLEEP_ACTIVE_EN at the same time, as this causes an invalid condition.
- To turn on the smart power switch while the MCU operates in active mode, set INTG_PWSWTCH_WKUP_ACTIVE_EN = 1 and INTG_PWSWTCH_SLEEP_ACTIVE_EN = 0.
- To turn off the smart power switch, set INTG_PWSWTCH_WKUP_ACTIVE_EN = 0 and INTG_PWSWTCH_SLEEP_ACTIVE_EN = 1 simultaneously.
- If the application does not use the smart power switch in MCU active mode, it is recommended not to write these bits.

If software configures the smart power switch to wake up either through the SWITCH_WAKEUP_B external pin or from any of the programmable band gap timers, the software must clear the corresponding status flag. Then, it is recommended to set INTG_PWSWTCH_WKUP_ACTIVE_EN = 1 and INTG_PWSWTCH_SLEEP_ACTIVE_EN = 0 to complete the smart power switch activation and prepare the hardware in advance for the next smart power switch shutdown sequence.

It is also recommended to use both INTG_PWSWTCH_WKUP_EN and INTG_PWSWTCH_SLEEP_EN bits when the smart power switch is actively controlling the power domains required by the MCU to run in active mode. This ensures proper MCU synchronization with device low-power entry or exit with smart power switch activation or deactivation.

4.2 Smart power switch main configuration registers

The smart power switch operation is managed through a set of control registers located in the SPC and VBAT memory-mapped regions. SPC registers configure switch behavior in both active and low-power modes.

Table 3. SPC register (SPC0 base address: 4001_6000h)

Offset	Register	Width (bits)	Access	Reset value
20 h	SPC configuration register (CFG) Controls the smart power switch on and off states in MCU Active and Low-power modes.	32	RW	0000_0000h

Table 4. VBAT register (VBAT0 base address: 4002_B000h)

Offset	Register	Width (bits)	Access	Reset value
10 h	Status A (STATUSA) Contains the status flags related to the VBAT turn-on events.	32	W1C	0000_0001h
20 h	Wake-up Enable A (WAKENA)	32	RW	0000_0001h

Table 4. VBAT register (VBAT0 base address: 4002_B000h) *...continued*

Offset	Register	Width (bits)	Access	Reset value
	Enables or disables the smart power switch turn-on source options.			
200 h	FRO16K Control A (FROCTLA) Contains the enable or disable option for the internal 16 kHz VBAT oscillator.	32	RW	0000_0001h
300 h	LDO_RAM Control A (LDOCTLA) Contains the enable options for the LDO RAM retention regulator.	32	RW	0000_0000h
320 h	RAM Control (LDORAMC) Configures the power supply settings for the SRAM retention memory.	32	RW	0000_0000h
330 h	Band gap timer 0 (LDOTIMER0) Contains the enable and timeout settings for the band gap timer 0.	32	RW	0000_0000h
338 h	Band gap timer 1 (LDOTIMER1) Contains the enable and timeout settings for the band gap timer 1.	32	RW	0000_0000h

4.2.1 SPC configuration register

The SPC configuration register (CFG) manages smart power switch behavior in active and low-power modes by setting specific control bits. The following are the descriptions and usage recommendations for each configurable bit:

- CFG[INTG_PWSWTCH_WKUP_ACTIVE_EN]: Writing this bit to '1' turns on the smart power switch when the MCU is in active mode. Changing this bit to any value when the MCU is in active mode and the switch is already turned on has no effect.
  Note: *Do not set this bit to '1' when INTG_PWSWTCH_SLEEP_ACTIVE_EN = 1.*
- CFG[INTG_PWSWTCH_SLEEP_ACTIVE_EN]: Writing this bit to '1' turns off the smart power switch when the MCU is in active mode. Changing this bit to any value when the MCU is in active mode and the switch is already turned on has no effect.
  Note: *Do not set this bit to '1' when INTG_PWSWTCH_WKUP_ACTIVE_EN = 1.*
- CFG[INTG_PWSWTCH_WKUP_EN]: Writing this bit to '1' configures the smart power switch to the on state when the MCU exits from any low-power mode.
- CFG[INTG_PWSWTCH_SLEEP_EN]: Writing this bit to '1' configures the smart power switch to the off state when the MCU enters any low-power mode.

4.2.2 Status A (STATUSA)

The STATUSA register provides read-only status bits related to smart power switch events, such as wake-up triggers, timer expirations, and POR.

- STATUSA[LDO_RDY]: Indicates whether the LDO RAM retention regulator is enabled and stable. This bit is read-only and set to '1' when the LDO RAM is enabled.
- STATUSA[TIMER1_FLAG]: Status bit for the band gap timer 1. This bit is set to '1' to indicate that the band gap timer 1 timeout has expired. Software must clear this bit after the timeout event by writing a '1' to this bit.

- STATUSA[TIMER0_FLAG]: Status bit for the band gap timer 0. This bit is set to '1' to indicate that the band gap timer 0 timeout has expired. Software must clear this bit after the timeout event by writing a '1' to this bit.
- STATUSA[WAKEUP_FLAG]: Status bit for the external SWITCH_WAKEUP_B pin on the device. This bit is set to '1' to indicate that the external wake-up pin has been pulled down. Software must check and clear this bit after a wake-up button press event by writing a '1' to this bit.
- STATUSA[POR_DET]: Status bit for the VBAT POR detection event. This bit is set to '1' after a VBAT POR. Software must clear this bit after the smart power switch POR event by writing a '1' to this bit.

4.2.3 Wake-up enable A (WAKENA)

The WAKENA register enables specific wake-up sources that can automatically activate the smart power switch.

- WAKENA [TIMER1_FLAG]: Set this bit to '1' to turn on the smart power switch when the band gap timer 1 timeout has been reached. Writing this bit to '0' disables this feature.
- WAKENA [TIMER0_FLAG]: Set this bit to '1' to turn on the smart power switch when the band gap timer 0 timeout has been reached. Writing this bit to '0' disables this feature.
- WAKENA [WAKEUP_FLAG]: Set this bit to '1' to turn on the smart power switch when the external SWITCH_WAKEUP_B signal is pulled down. Writing this bit to '0' disables this feature.

4.2.4 FRO16K control A (FROCTLA)

The FROCTLA register allows control of the internal VBAT FRO16K oscillator.

- FROCTLA[FRO_EN]: Writing this bit to '1' enables the VBAT FRO16K oscillator.
  This oscillator is enabled by default. Ensure that the FRO16K oscillator is enabled before using any feature that depends on it, such as the band gap timers or the LDO RAM retention regulator.

4.2.5 LDO RAM control A (LDOCTLA)

The LDOCTLA register manages the enablement and operation modes of the LDO RAM regulator.

- LDOCTLA[REFRESH_EN]: Enables the LDO RAM refresh mode, which decreases the LDO power consumption. LDO RAM enters refresh mode by setting this bit in '1'.
- LDOCTLA[LDO_EN]: Activates the LDO RAM regulator. Before setting this bit to '1' to enable the LDO RAM regulator, ensure that the initilization sequence described in Section 4.1.2.1 has been followed.
- LDOCTLA[BG_EN]: Enables the LDO RAM band gap required as part of the LDO RAM enable sequence. Writing this bit to '1' enables the LDO RAM band gap.

4.2.6 RAM control (LDORAMC)

The LDORAMC register is used to configure the SRAM retention memory power supply between different domains.

- LDORAMC[SWI]: Selects the SRAM retention memory power supply between the VDD_CORE domain and the VBAT LDO RAM.
  - To select the LDO RAM, set SWI = 1.
  - To select the VDD_CORE, set SWI = 0.
  - Before selecting the VBAT LDO RAM as the power supply for the SRAM retention memory, set LDORAMC[ISO] = 1.
- LDORAMC[ISO]: Set this bit to '1' to isolate the SRAM memory power supply from the rest of memory and place the array in low-power retention mode before switching the SRAM supply to the VBAT LDO RAM.

4.2.7 Band gap timer 0 (LDOTIMER0)

The LDOTIMER0 is used to manage the timing and activation of the band gap timer 0.

- LDOTIMER0[TIMEN]: Set this bit to '1' to enable the band gap timer 0. The timer starts counting immediately after being set, therefore, this bit must be written at last as a part of the band gap timer enable sequence. ***Note:*** *Ensure that this bit is disabled (TIMEN = 0) before updating the smart power switch timeout to avoid unintended behavior.*
- LDOTIMER0[TIMCFG]: This 3-bit field configures the band gap timer 0 timeout value. The available timeout values are shown in Table 5:

Table 5. VBAT register

LDOTIMER0[TIMCFG]	Band gap timer 0 timeout
000b	1 s
001b	500 ms
010b	250 ms
011b	125 ms
100b	62.5 ms
101b	31.25 ms
110b	15.625 ms
111b	7.8125 ms

4.2.8 Band gap timer 1 (LDOTIMER1)

The LDOTIMER1 register is used to enable and configure the timeout value for band gap timer 1.

- LDOTIMER1[TIMEN]: Set this bit to '1' to enable the band gap timer 1. The timer starts counting immediately after being set, therefore, this bit must be written at last as a part of the band gap timer enable sequence. ***Note:*** *Ensure that this bit is disabled (TIMEN = 0) before updating the smart power switch timeout to avoid unintended behavior.*
- LDOTIMER1[TIMCFG]: This 24-bit field configures the band gap timer 1 timeout value. It can be configured in the range from 1 s to 16,777,216 s with a resolution of 1 s per increment in the TIMCFG value.

4.3 Smart power switch electrical characteristics

Table 6 lists the key electrical characteristics of the smart power switch, including input voltage, load current capacity, on-state resistance, and leakage current under specific conditions:

Table 6. Smart power switch specifications

Symbol	Description	Min.	Type	Max.	Unit
V-supply	VDD_SWITCH input voltage	1.9	-	3.6	V
I-load	Smart power switch output load current	-	-	40	mA
Ron	Switch series resistance in on-state	-	-	3	Ω
I_leakage1	Typical leakage current when V_SWITCH_IN = 2.7 V at 25 °C	-	4	-	nA
I_leakage2	Typical leakage current when V_SWITCH_IN = 3.3 V	-	-	1	µA

5 Smart power switch test on KW47-EVK

To evaluate the smart power switch functionality on the KW47-EVK, you need to build and program two projects:

- main_image
- wakeup_image

These projects enable the following features:

- Fast wake-up
- Wake-up via pin or timer
- SRAM retention
- Active-state switch control

All features are configurable through preprocessor definitions.

5.1 Smart power switch software

To evaluate the functionality of the smart power switch on the KW47-EVK, the following software setup and configuration guidelines must be followed. This section details the software components, necessary jumper settings, and configurable features required to perform a successful power switch test.

Place both KW47-EVK and KW47-001-M10 module in the default jumper configuration. To verify such configuration, refer to the boards schematics.[1] The application demo software includes two projects:

- main_image
- wakeup_image

Build both projects and program them into KW47 MCU.

The software supports the following features:

- Fast wake-up from smart power switch
- Switch-on through SWITCH_WAKEUP_B pin
- Switch-on through band gap timer 1
- STCM8 SRAM data retention during switch-off

These features can be enabled or disabled through configuration definitions included in the header file, app_config.h contained in the main_image project. The following features can be enabled or disabled using configuration definitions:

- *gAppFastWakeUpEnable*: Set this definition to 1 to enable fast wake-up from the smart power switch. As the fast wake-up feature requires STCM8 SRAM retention to hold wake-up image entry address and image CRC, the *gAppRetentionEnable* definition must set to 1 as well. When this feature is enabled, the application flow jumps to the wake-up image when the smart power switch transitions from off state to on state. When the MCU is running the wake-up image, the green LED D2 starts blinking on the KW47-001-M10 module.
- *gAppRetentionEnable*: Set this definition to 1 to enable STCM8 SRAM array retention during switch-off. When this feature is enabled, the application switches the SRAM array supply from VDD_CORE to VDD_SWITCH prior to turning the switch-off.
- *gAppTimer1WakeupEnable*: Set this definition to 1 to enable a smart power switch on through band gap timer 1. By default, the band gap timer 1 is set to a 190 s timeout period. If *gAppTimer1WakeupEnable* is set to 0, the switch can be turned on through the SWITCH_WAKEUP_B pin (routed to button SW5 on KW47-EVK). If *gAppRetentionEnable* is set to 0, set *gAppTimer1WakeupEnable* to 0 as well to prevent LDO_RAM high power consumption. For more information, refer to Section 4.1.1.

1 For more information, contact yout local FAE or sales representative.

- *gAppSPSControlOnActiveEnable*: Set this definition to 1 to allow software to control the switch state while the MCU is in active state. If *gAppSPSControlOnActiveEnable* is set to 0, the switch automatically turns on at low-power exit and turns off at low-power entry. Set this definition to 0 when the smart power switch is actively controlling the power domains required by the MCU to run in active mode as mentioned Section 4.1.4.
- *gAppVerboseEnable*: Set this definition to 0 when using KW47-EVK.

5.2 KW47-001-M10 module settings

To ensure proper functionality of the application, the following hardware modifications must be performed on the KW47-001-M10 module:

1. Cut the SH9 trace between P3V3_DUT and VDD_REG nodes.

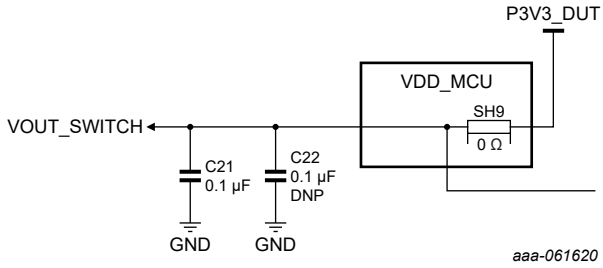


Figure 8. KW47-001-M10 module SH9 schematic view

2. Populate with a 0 Ω resistor in SH9 to connect VDD_REG and VOUT_SWITCH nodes.
3. Populate C20 with a 4.7 µF capacitor on the VOUT_SWITCH node.

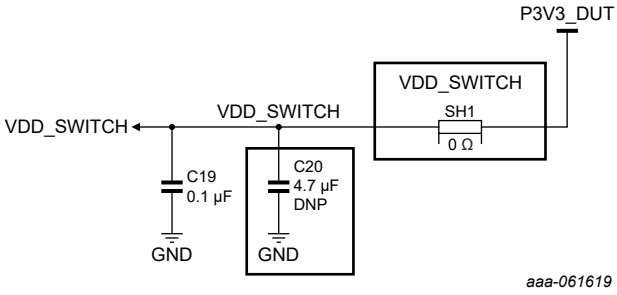


Figure 9. KW47-001-M10 module C20 schematic view

4. Cut the SH10 trace to prevent the reset LED (D1) from being forward biased during smart power switch-off.

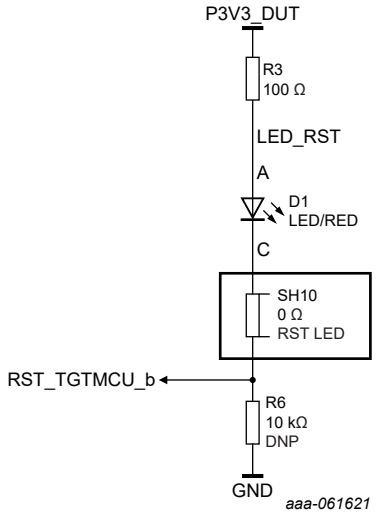


Figure 10. KW47-001-M10 module SH10 schematic view

5.3 KW47-EVK board settings

As mentioned in Section 4, the smart power switch usage is recommended when MCU requires low power consumption for extended periods of time. As the VOUT_SWITCH node can be connected to several external capacitors, it is expected that the VOUT_SWITCH voltage level decreases to approximately 0 V over time. This discharge time depends on the board and mainly on the VOUT_SWITCH rail capacitance.

If VOUT_SWITCH is not discharged to a voltage threshold at which the supplied power domains become nonoperational, and a smart power switch turn-on event occurs (such as a SWITCH_WAKEUP_B falling edge or band gap timer expiration), the device POR cannot execute correctly, potentially affecting the application flow.

The smart power switch operates under the assumption that all onboard devices connected to the KW47 MCU through I/O pins are also powered by VOUT_SWITCH. As VOUT_SWITCH is sensitive to the external supply on I/O pins, caution is required during power-down scenarios. If an MCU I/O pin is pulled high while its corresponding power domain is powered off by the smart power switch off, there is a risk of back-powering that domain through the ESD bus.

To avoid such a scenario, ensure that the connected I/O pins are not pulled high when VOUT_SWITCH = OFF. On the KW47-EVK board, the most effective way to prevent this case is by isolating pins from KW47 MCU. To accomplish this, perform the following board configuration:

1. Cut the JS1 short between VBOARD and VDD_MEM nodes. Populate with jumpers afterward if needed.

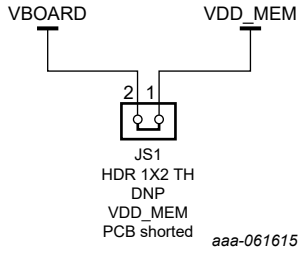


Figure 11. KW47-EVK JS1 schematic view

2. Cut the JS2 short between VBOARD and P_LED nodes. Populate with jumpers afterward if needed.

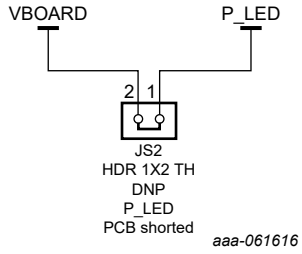


Figure 12. KW47-EVK JS2 schematic view

3. Cut the JS3 short between VBOARD and VDD_SENSOR nodes. Populate with jumpers afterward if needed.

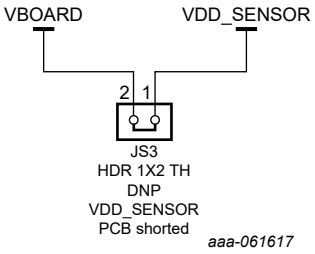


Figure 13. KW47-EVK JS3 schematic view

4. Cut the JS4 short between VBOARD and VDD_PMOD nodes. Populate with jumpers afterward if needed.

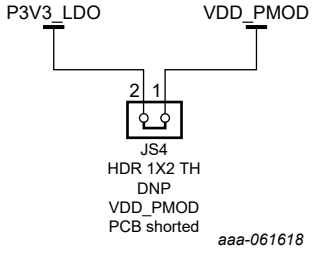


Figure 14. KW47-EVK JS4 schematic view

5. Cut JS6 short between VCC_TGMCU and resistors R128 and R129. Populate jumpers afterward if needed.

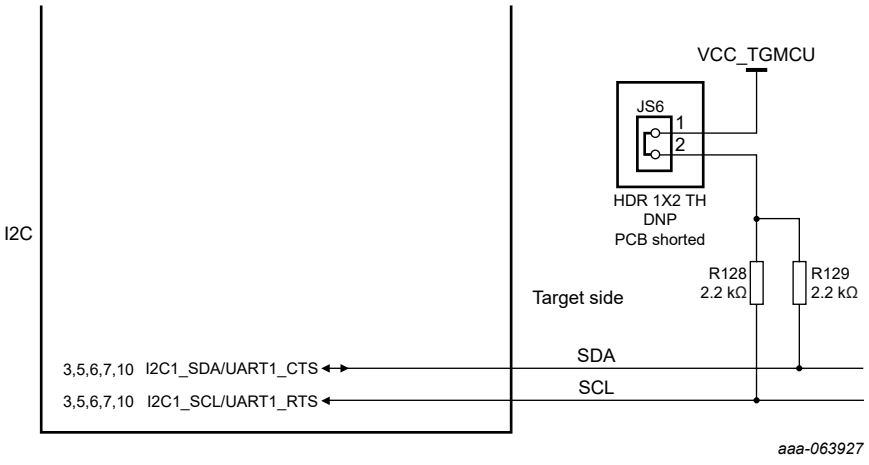


Figure 15. KW47-EVK JS6 schematic view

6. Remove all jumper connections from JP1 and JP3 on the KW47-EVK board. Create a jumper connection between P3V3_LDO and VBOARD nodes for JP3. Create another jumper connection between P3V3_DUT and VBOARD nodes for JP1. Refer to Figure 17 for jumper schematic view.
7. Remove jumper connections JP16 and JP17.

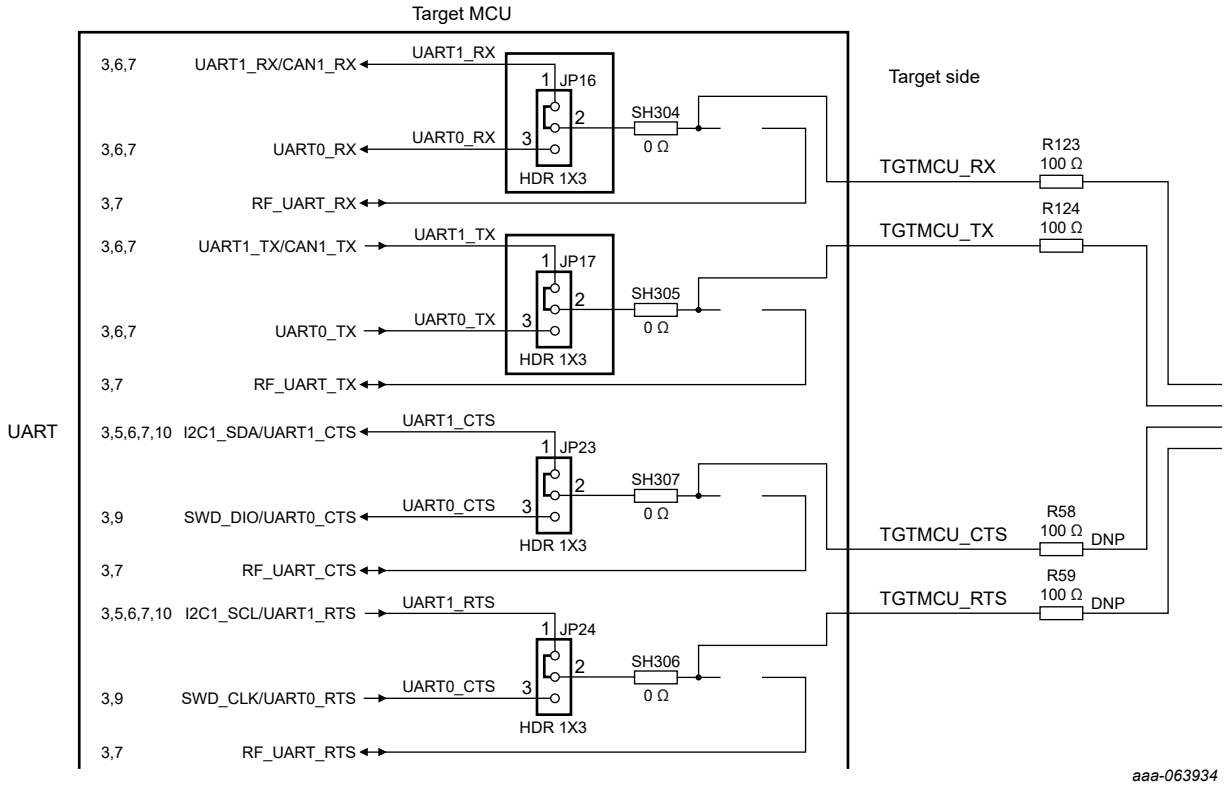


Figure 16. KW47-EVK JP16/JP17 schematic view

8. Remove the JP28 jumper and start the application. Refer to Figure 19 for jumper schematic view.

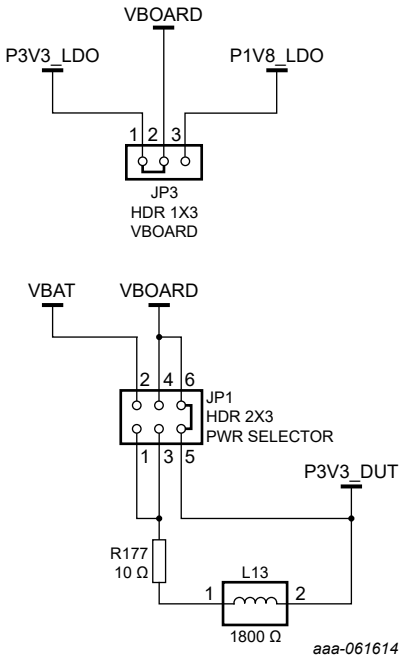
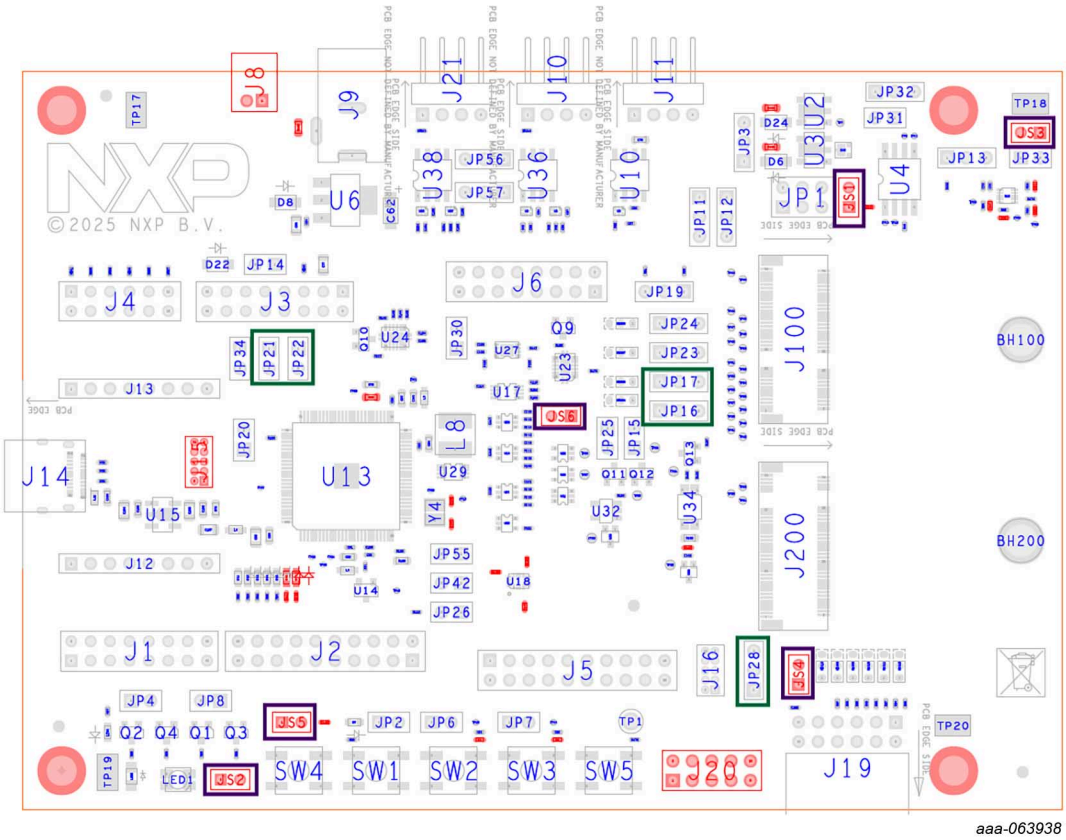


Figure 17. KW47-EVK JP1 and JP3 schematic view

Refer to Figure 18 for the KW47-EVK board view showing all mentioned connections. Connections that require board rework are framed in purple.

Note:

- *Connections that require board rework are framed in purple.*
- *Connections that must be removed while the application runs are framed in green.*



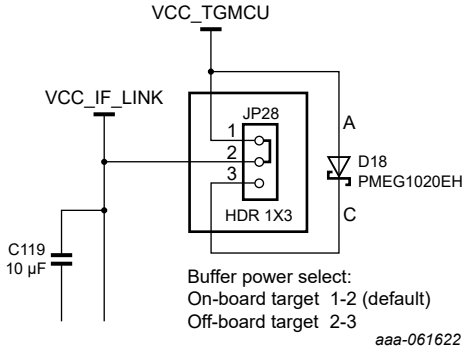
aaa-063938

Figure 18. KW47-EVK board view

5.4 Software reprogramming

When the VDD_IO_ABC power domain is not powered, such as during smart power switch shutdown, the SWD pin interface becomes inactive. This presents a challenge for reprogramming the device. To reprogram the device, follow the steps below:

1. Disconnect the power supply from the KW47-EVK board.
2. Connect a jumper at JP28 between VCC_TGMCU and VCC_IF_LINK (this is the default configuration).



aaa-061622

Figure 19. KW47-EVK JP28 schematic view

3. Connect the power supply to the KW47-EVK while holding down button SW4 (PTA4/BOOT_CONFIG pin). This action forces the KW47 MCU to In-System Programming (ISP) mode, preventing the smart power switch from turning off.
4. Reprogram the KW47 MCU device.
5. Remove the JP28 jumper and restart the application.

5.5 KW47-EVK: Smart power switch demo results

This section lists the current and power consumption peformance of the KW47-EVK smart power switch in two different configurations.

5.5.1 Test setup 1

Test setup 1 evaluates the low-power performance of the KW47-EVK with the SRAM array not retained. It focuses on current and power consumption during the switch-off state with wake-up triggered through SWITCH_WAKEUP_B pin.

- Hardware: KW47-EVK + KW47-001-M10 module
- Power configuration:
  - DC-DC mode
  - DCDC_OUT = 1.8 V
  - VDD_SWITCH = 3.3 V
- Memory retention: STCM8 SRAM array not retained
- Wake-up source: SWITCH_WAKEUP_B

Results:

- Current consumption during switch-off: 99.68 nA
- Power consumption during switch-off: 321.12 nW

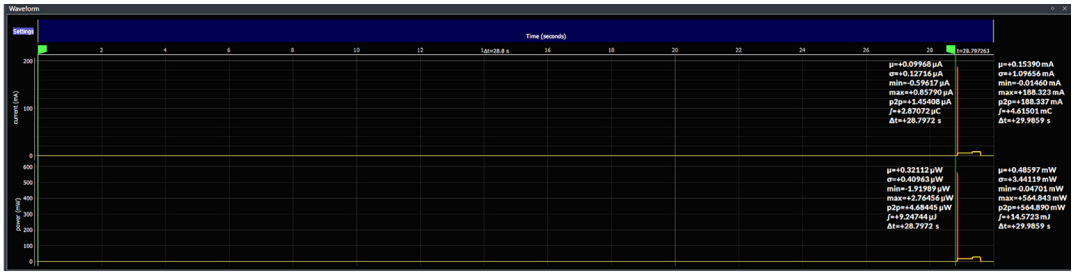


Figure 20. KW47 – SRAM not retained current profile

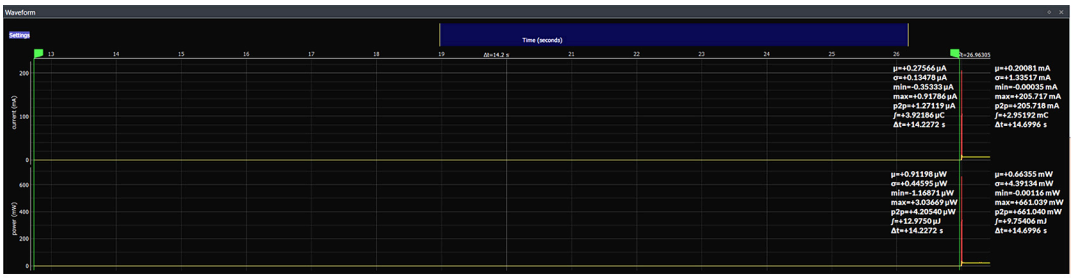
5.5.2 Test setup 2

Test setup 2 assesses the KW47-EVK power behavior when the SRAM array is retained. It uses a band gap timer for wake-up to analyze the trade-offs in current and power consumption during the switch-off state.

- Hardware: KW47-EVK + KW47-001-M10 module
- Power configuration:
  - DC-DC mode
  - DCDC_OUT = 1.8 V
  - VDD_SWITCH = 3.3 V
- Memory retention: STCM8 SRAM array retained
- Wake-up source: Band gap timer 1

Results:

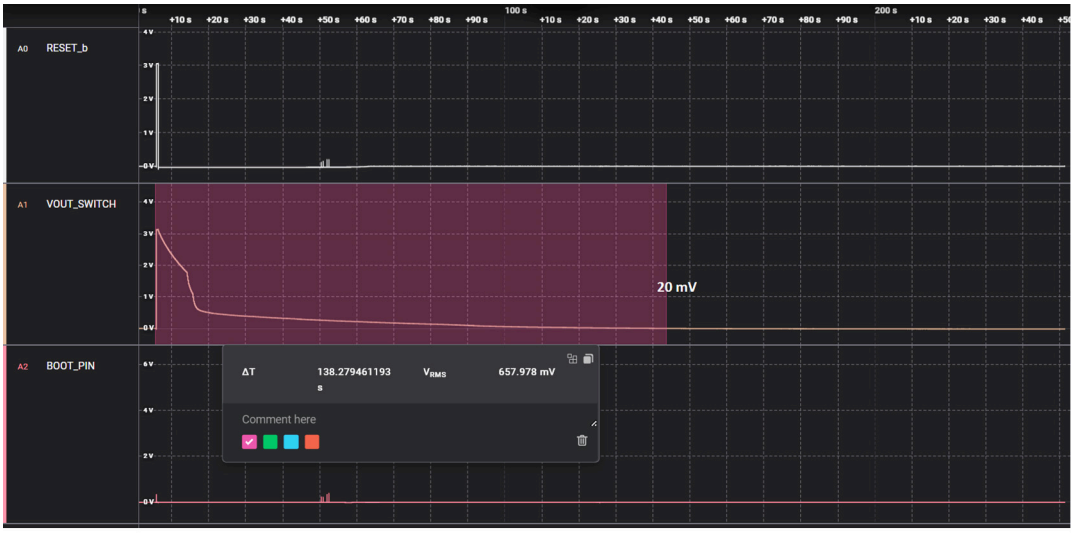
- Current consumption during switch-off: 275.66 nA
- Power consumption during switch-off: 911.98 nW



aaa-061627

Figure 21. KW47 – SRAM retained current profile

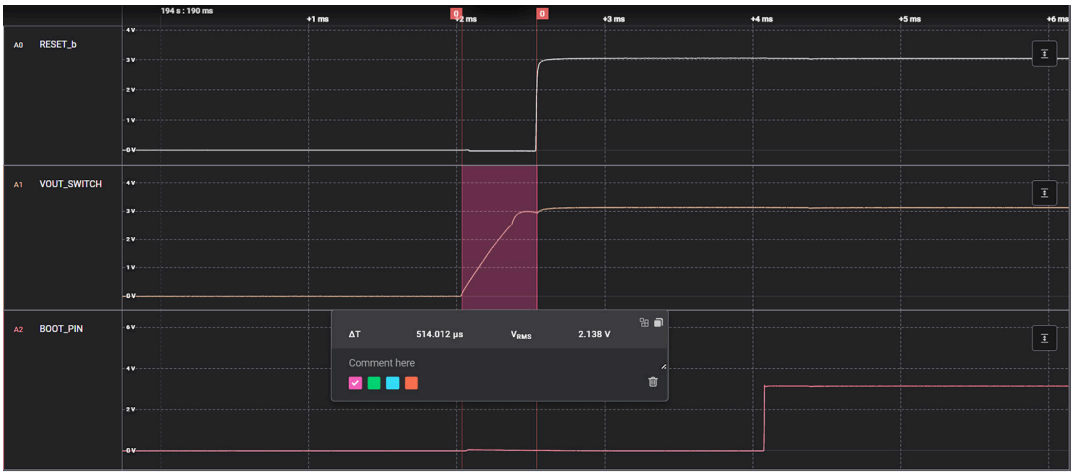
Once the smart power switch turns off, the VOUT_SWITCH takes approximately 140 s to reach 20 mV.



aaa-061623

Figure 22. KW47-EVK – VOUT_SWITCH discharge time

Once the smart power switch turns on, the VOUT_SWITCH takes approximately 515 µs to reach the required voltage threshold for hardware initialization.



aaa-061625

Figure 23. KW47-EVK – VOUT_SWITCH rising voltage time

To analyze the power rails during a smart power switch wake-up event, connect an oscilloscope to track VOUT_SWITCH, DCDC_OUT, and LDO_CORE_OUT. In DC-DC mode, VOUT_SWITCH powers VDD_DCDC, which then powers VDD_LDO_CORE to its operational voltage. The MCU asserts PTD3_WKUP_SIGNAL (PTD3 pin) at main core boot before RAM initialization. After RAM initialization, PTD3_WKUP_SIGNAL toggles indefinitely, indicating a successful wake-up from the smart power switch.

Set the *gAppFastWakeUpEnable* and *gAppRetentionEnable* macros to 1 in the software configuration. Set *gAppTimer1WakeupEnable* to 0 to use SWITCH_WAKEUP_B (SW5 on the board) and its falling edge as the reference for the wake-up event.

For more details, refer to the Section 5.1.

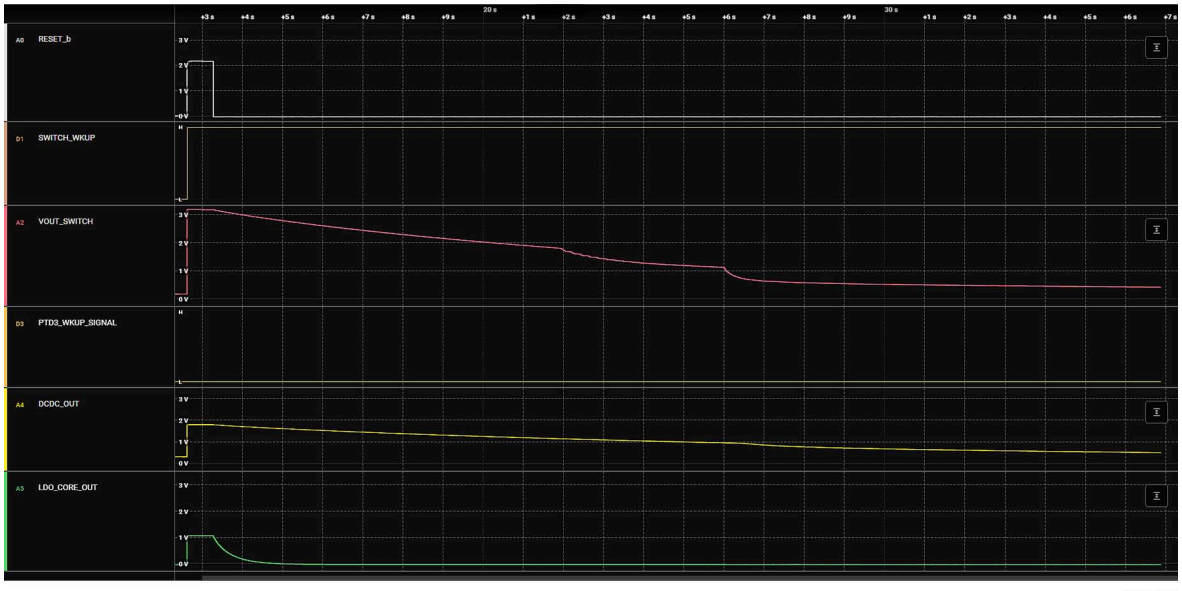


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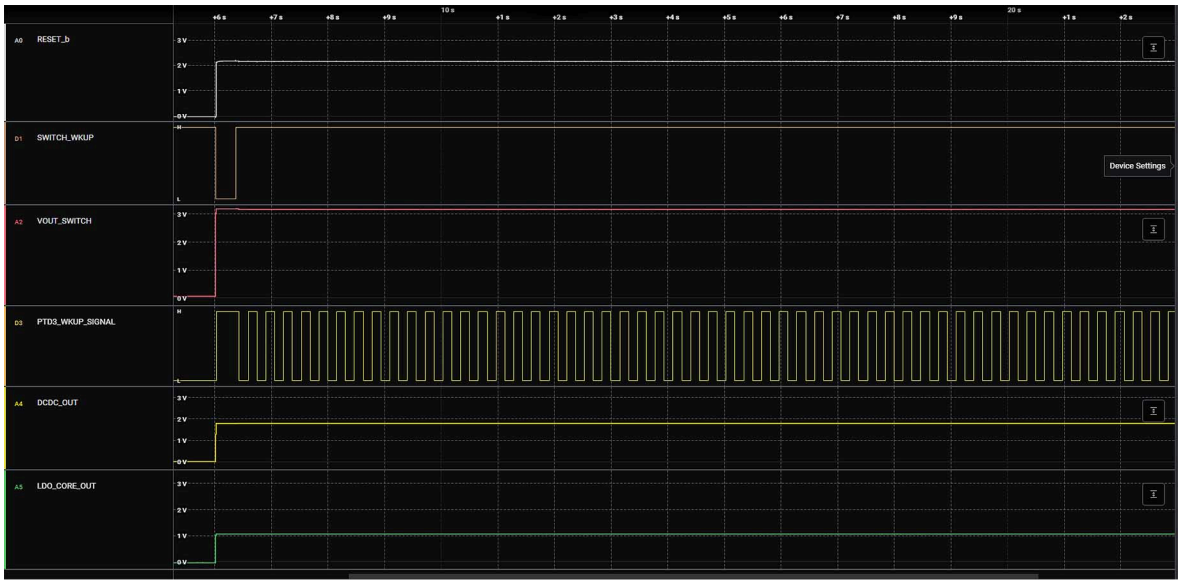
Figure 24. Smart power switch-off event power rail analysis



aaa-063940

Figure 25. Smart power switch-on event power rail analysis

On the KW47-EVK, the MCU takes about 658.28 µs to complete wake-up from the smart power switch. The boot sequence depends on VOUT_SWITCH voltage stability, which in turn depends on VOUT_SWITCH capacitance as explained earlier.

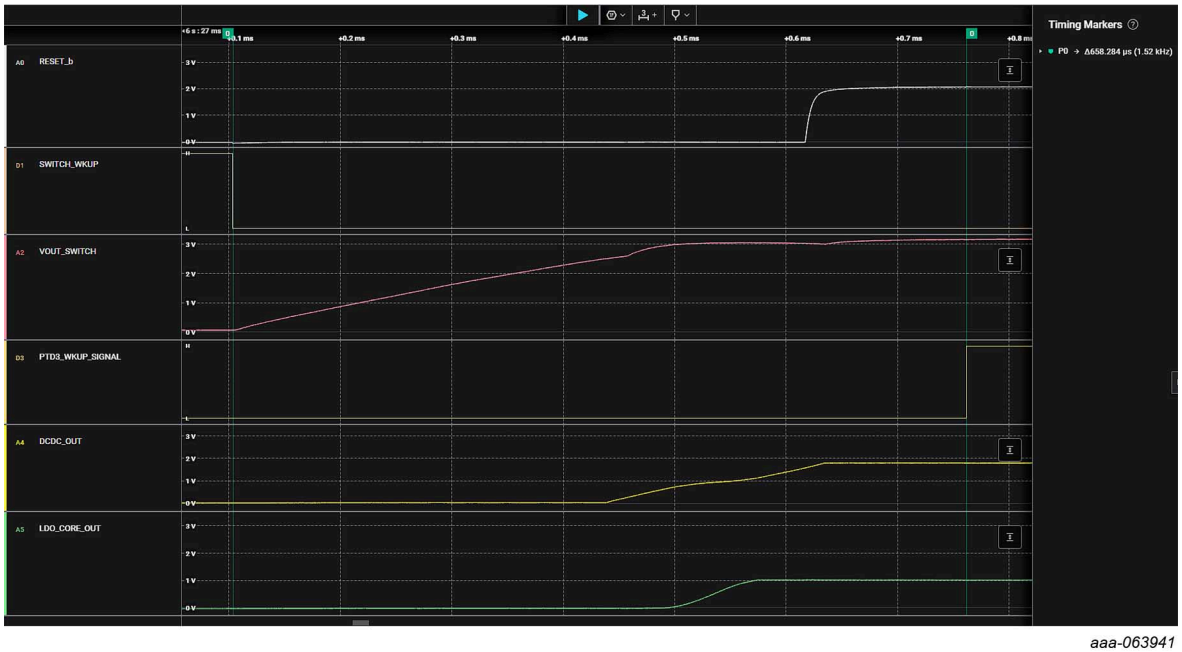


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Figure 26. Wake-up from smart power switch event power rail analysis and wake-up latency

6 Acronyms

Table 7 lists the acronyms used in this document.

Table 7. Acronyms

Term	Description
ADC	Analog-to-Digital Converter
DC	Direct Current
ECC	Error Correction Code
ISP	In-System Programming
LDO	Low Dropout Regulator
OSC	Oscillator
POR	Power-on Reset
RAM	Random Access Memory
RF	Radio Frequency
STCM8	System Tightly Coupled Memory 8
SPC	System Power Controller
SRAM	Static Random Access Memory

7 Revision history

Table 8 summarizes the revisions to this document.

Table 8. Revision history

Document ID	Release date	Description
AN14684 v.2.0	10 December 2025	Initial public release
AN14684 v.1.0	21 July 2025	Initial NDA release

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