AN14673

i.MX RT1040 Product Lifetime Usage Estimates

Rev. 1.0 — 26 May 2025 **Application note**

Document information

Information	Content
Keywords	AN14673, i.MX RT1040, lifetime estimates
Abstract	This document provides guidance on how to interpret the different i.MX RT1040 qualification levels in terms of the target operating frequency of the device, the maximum supported junction temperature (Tj) of the processor, and how this relates to the lifetime of the device.

1 Introduction

The i.MX RT series consists of an extensive number of processors that deliver a wide range of processing and multimedia capabilities across various qualification levels.

This document provides guidance on how to interpret the different i.MX RT1040 qualification levels in terms of the target operating frequency of the device, the maximum supported junction temperature (Tj) of the processor, and how this relates to the lifetime of the device.

Each qualification level supported (commercial and industrial) defines a number of Power-on Hours (PoH) available to the processor under a given set of conditions, such as:

- The target frequency for the application (commercial and industrial).
  - The target frequency is determined by the input voltage to the processor's core complex (VDD_SOC_IN).
  - The use of the DCDC-enabled or DCDC-bypass mode.
    - When using the DCDC-bypass mode, do not set the target voltage to the minimum specified in the data sheet. All power-management ICs have allowable tolerances. Set the target voltage higher than the minimum specified voltage to account for the tolerance of the PMIC. The tolerance assumed in the calculations in this document is +/-25 mV.
    - The DCDC-enabled mode uses the DCDC module to generate a power supply for the core logic on the i.MX RT series. The DCDC module is well characterized and you can set it to output the exact minimum specified voltage. You can achieve longer PoH using the DCDC-enabled mode.
- The percentage of active use compared to the standby mode.
  - Active use means that the processor is running in an active performance mode.
    - For the commercial and industrial tiers, there are two performance modes available: 600 MHz and 528 MHz.
  - In the DSM mode, the data sheet defines lower operating conditions for VDD_SOC_IN, reducing the power consumption and junction temperature. In this mode, the voltage and temperature are set low enough so that the effect on the lifetime calculations is negligible and treated as if the device was powered off.
- The junction temperature (Tj) of the processor.
  - The maximum junction temperature of the device is different for each tier of the product (95 °C for commercial and 125 °C for industrial). This maximum temperature is guaranteed by the final test.
  - Ensure that your device is appropriately thermally managed, such that you do not exceed the maximum junction temperature.

Note: *All data provided within this document are estimates for PoH that are based on extensive qualification experience and testing with the i.MX RT series. These statistically derived estimates should not be viewed as a limit on an individual device's lifetime, nor should they be construed as a guarantee by NXP as to the actual lifetime of the device. Sales and warranty terms and conditions still apply.*

2 Device qualification level and available PoH

This section describes the device qualification level and available PoH.

2.1 Commercial qualification

Table 1 provides the number of PoH for the typical use conditions for the commercial device.

Table 1. Commercial qualification lifetime estimates

-	Arm core speed (MHz)	Power-on Hours [PoH] (hours)	Arm core operating voltage (V)	Junction temperature [Tj] (°C)
Case C1: DCDC enabled	600	28,098	1.25	95
Case C2: DCDC enabled	528	76,379	1.15	95
Case C3: DCDC bypassed	600	21,883	1.275	95
Case C4: DCDC bypassed	528	59,484	1.175	95

Figure 1and Figure 2 establish the guidelines for estimating PoH as a function of the CPU frequency and junction temperature. You can read the PoH directly off the charts below to determine the necessary trade-offs to CPU frequency and junction temperature to increase the estimated PoH of the device.

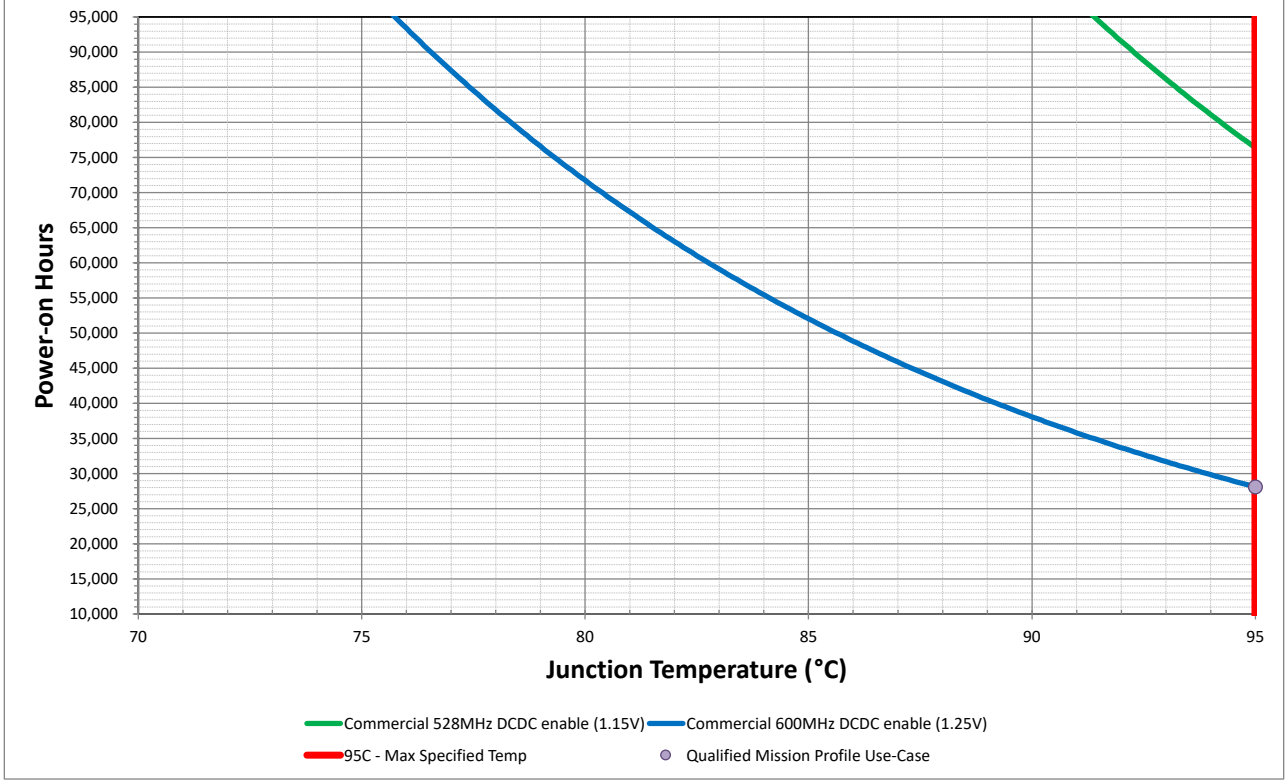

Figure 1. i.MX RT1040 commercial lifetime estimates for DCDC-enabled mode

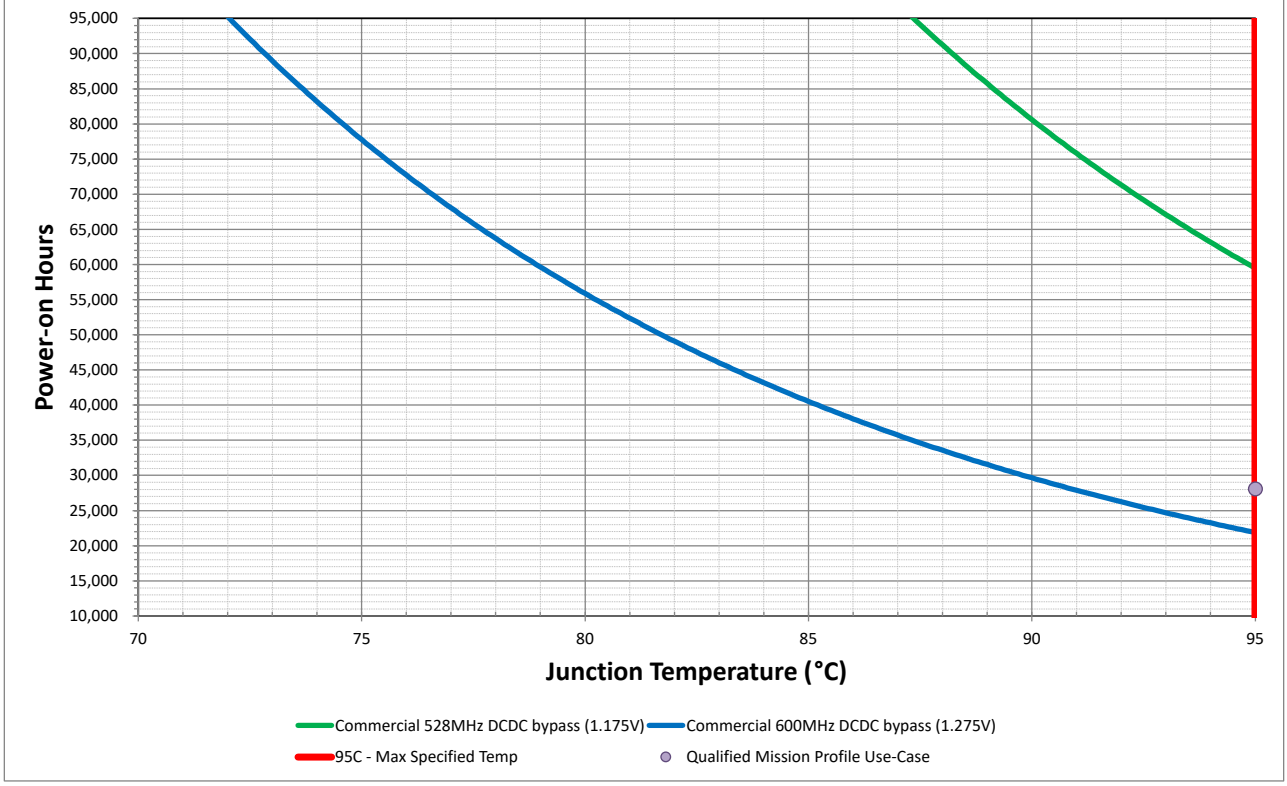

Figure 2. i.MX RT1040 commercial lifetime estimates for DCDC-bypass mode

2.2 Industrial qualification

Table 2 provides the number of PoH for the typical use conditions for the industrial device.

Table 2. Industrial qualification lifetime estimates

-	Arm core speed (MHz)	Power-on Hours [PoH] (hours)	Arm core operating voltage (V)	Junction temperature [Tj] (°C)
Case I1: DCDC enabled	528	30,041	1.15	125
Case I2: DCDC bypassed	528	23,396	1.175	125

Figure 3 and Figure 4 establish the guidelines for estimating the PoH as a function of the CPU frequency and junction temperature. You can read the PoH directly off of the charts below to determine the necessary trade-offs to the CPU frequency and junction temperature to increase the estimated PoH of the device.

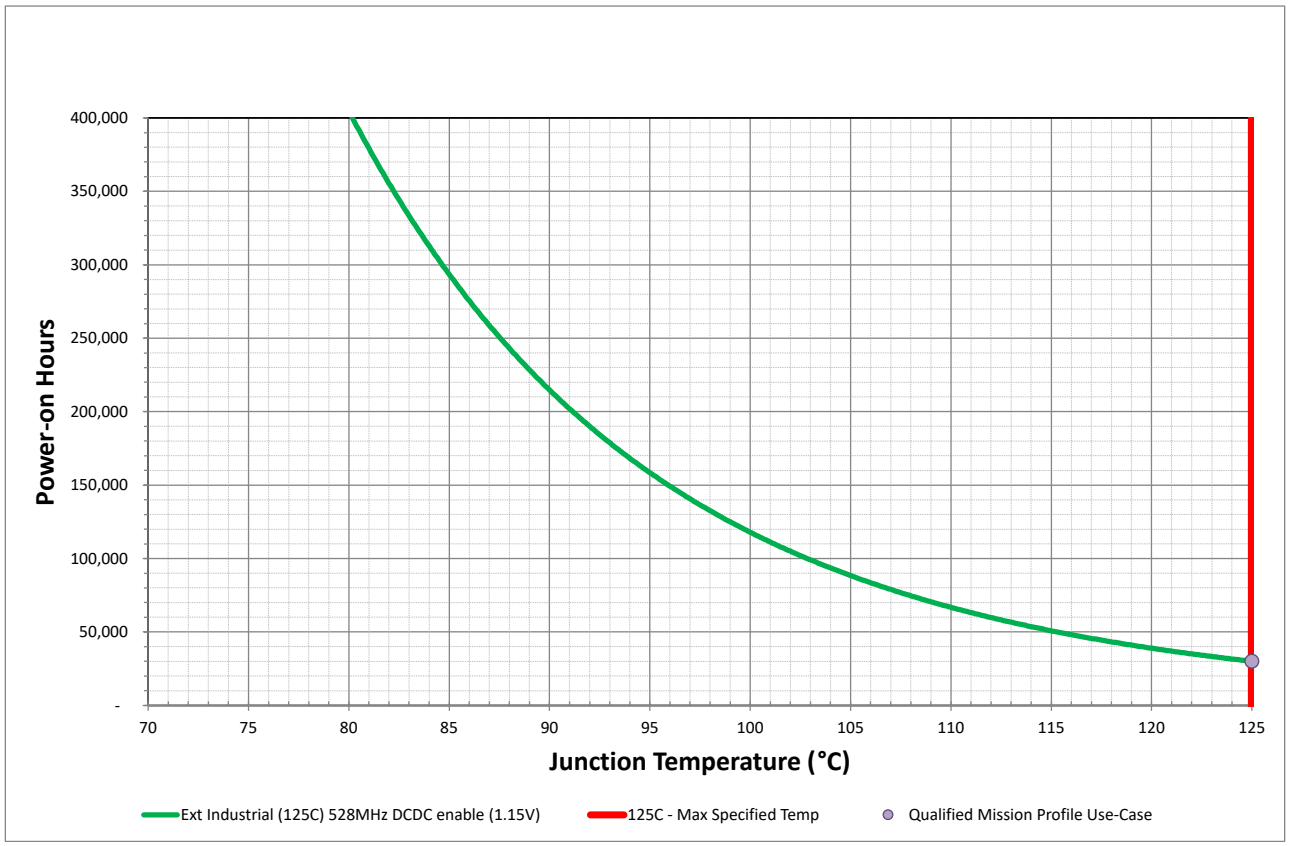

Figure 3. i.MX RT1040 industrial lifetime estimates for DCDC-enabled mode

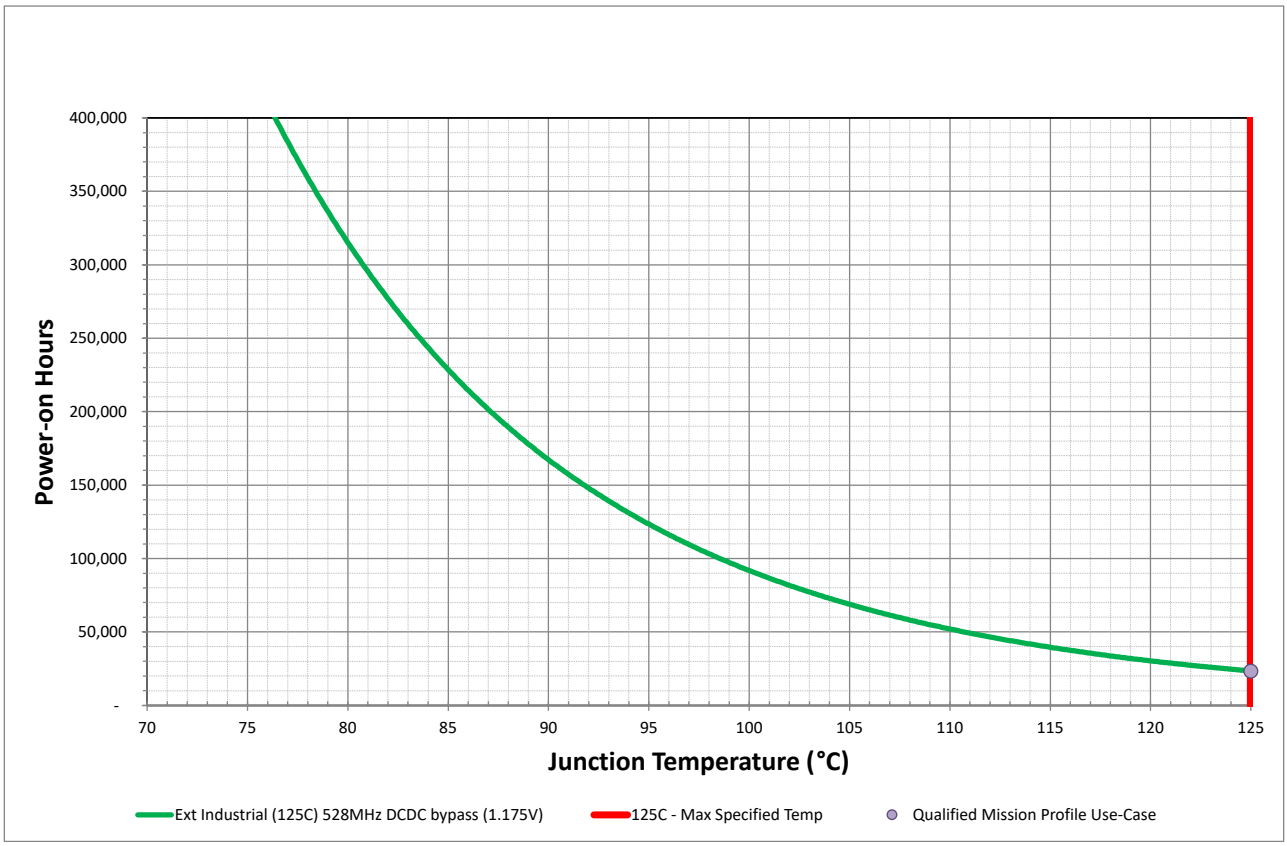

Figure 4. i.MX RT1040 industrial lifetime estimates for DCDC-bypass mode

3 Combining use cases

In some applications, a constant operating use case cannot deliver the target PoH. In this case, it is useful to use multiple operating conditions. This method provides some of the lifetime benefits of running at a lower performance use case, while keeping the ability of the system to use the highest performance state according to the application demands.

3.1 Scenario 1: switching between two power states with different voltages

In this scenario, the system is using the 600-MHz full-power state, and the 528-MHz reduced power state. For these calculations, we assume that the temperature stays constant in either mode. If the system spends 50 % of its power-on time at 600 MHz and 50 % of its power-on time at 528 MHz, the two PoH (read from Figure 5) combine using those percentages: 31,698 x 0.5 + 86,165 x 0.5 = 58,931 PoH.

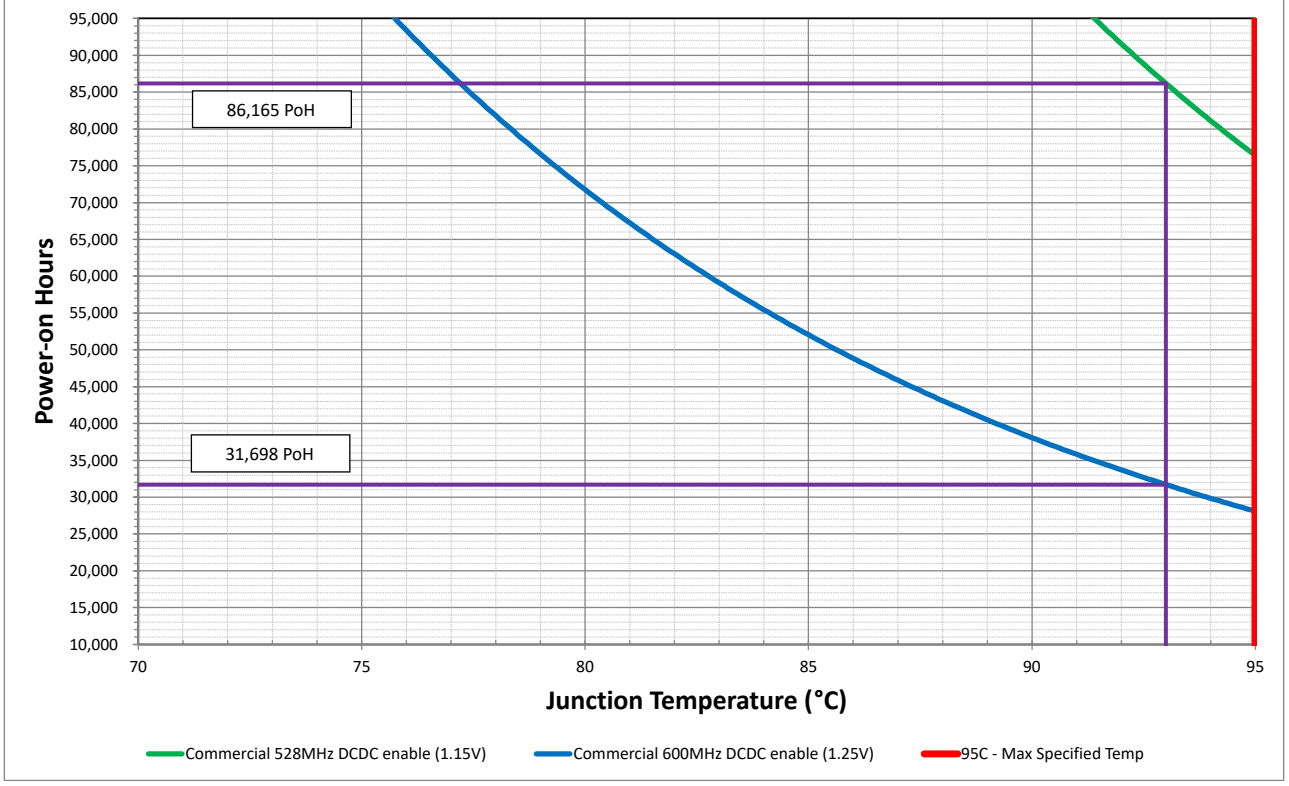

Figure 5. Multiple power state use case

3.2 Scenario 2: switching between two power states with different temperatures

This scenario assumes that the system can achieve a drop in temperature by throttling back the performance, while still maintaining a constant voltage. You can achieve this temperature change by changing the frequency or by scaling back the loading on the Arm cores or processing units. This use case is useful for customers who want to take advantage of the full commercial temperature range of the i.MX RT series. In this scenario, the system spends 30 % of its PoH at 93 °C and 70 % of its PoH at 85 °C (as shown in Figure 6). The two PoH can be combined as follows: 31,698 x 0.3 + 52,038 x 0.7 = 45,932 PoH.

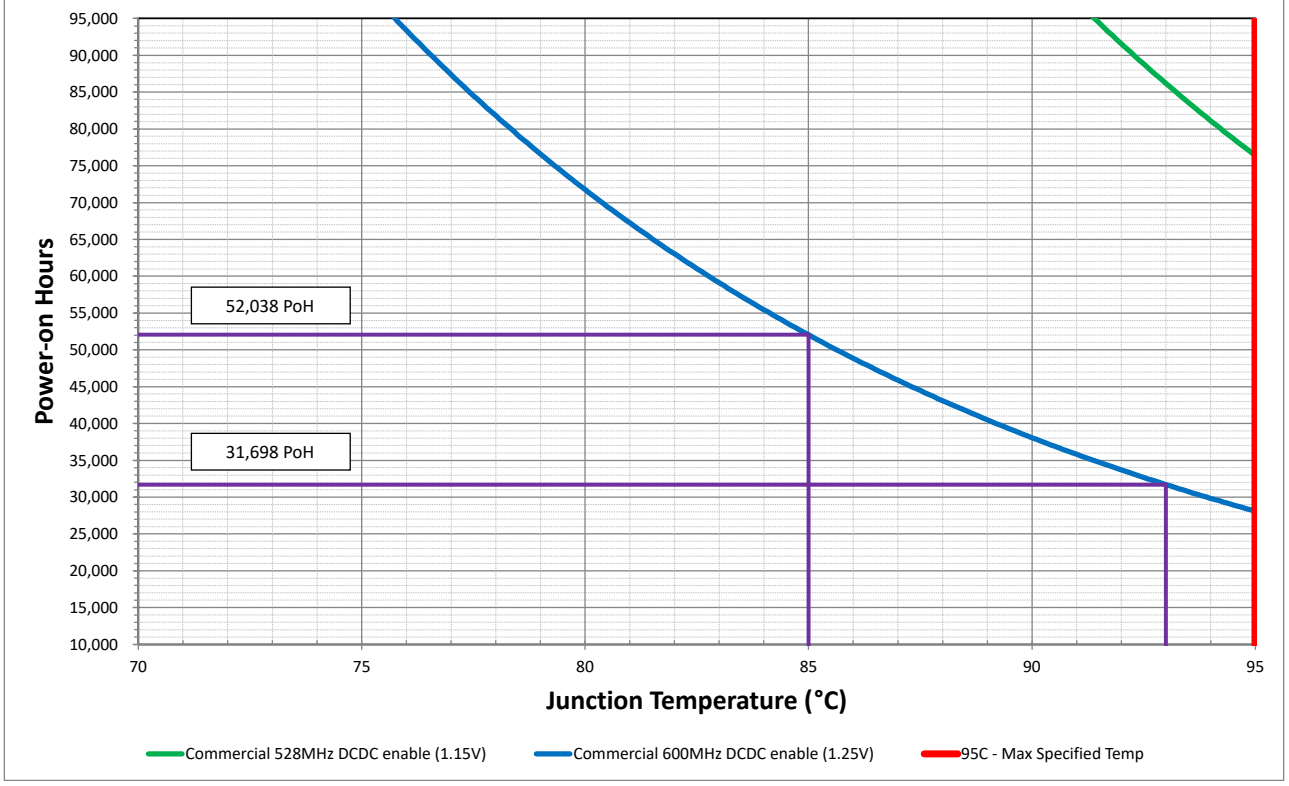

Figure 6. Multiple temperature use case

3.3 Scenario 3: using three or more power states

This scenario shows how to extend this strategy to more than two power states. While this example only has three power states, there is no limit to the actual number of the power states to combine. The power states used in this scenario are 528 MHz (at 93 °C) and 600 MHz (at 85 °C and 93 °C). It uses each state for one third of the time. You can combine these power states as follows: 86,165 x 0.34 + 52,038 x 0.33 + 31,298 x 0.33 = 56,796 PoH.

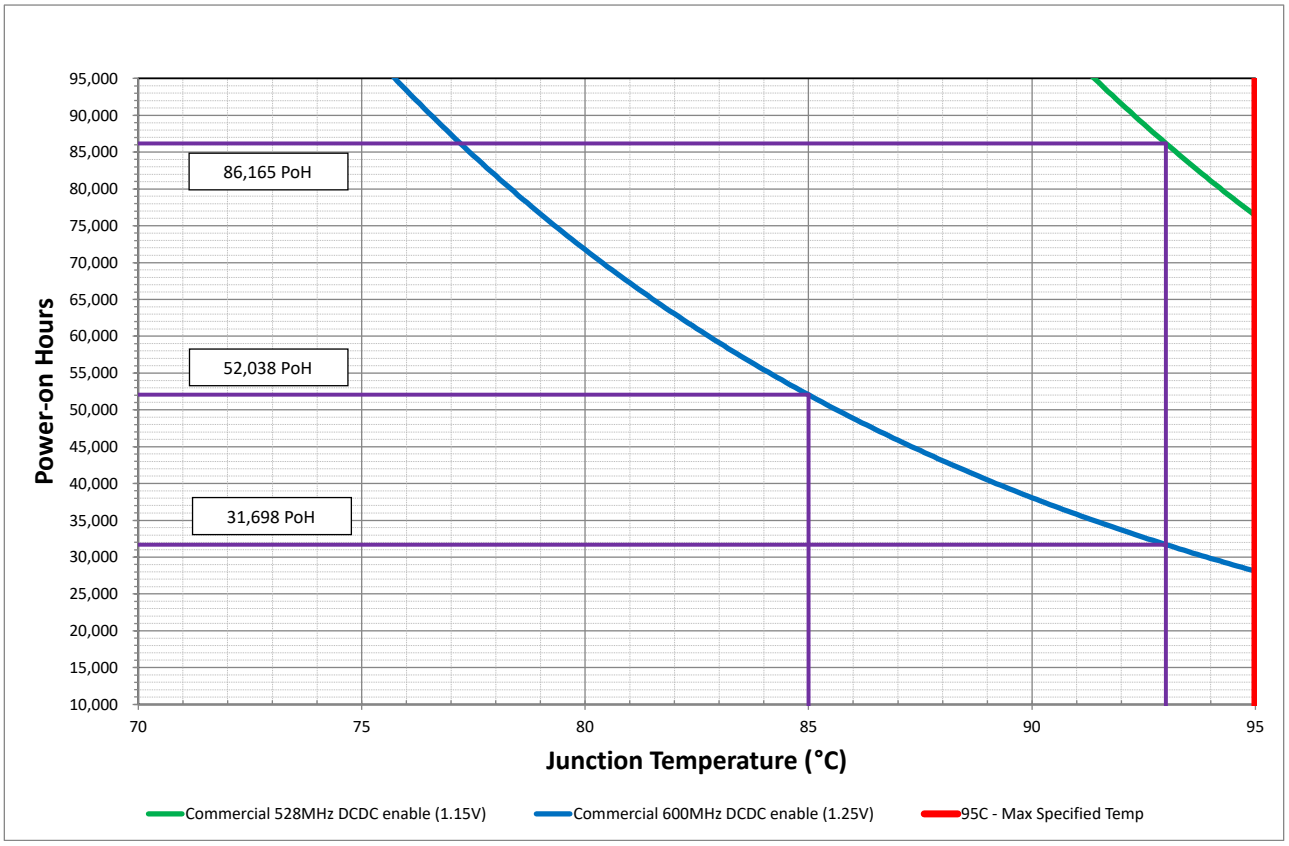

Figure 7. Using three or more power states

4 Revision history

Table 3. Revision history

Document ID	Release date	Description
AN14673 v.1.0	26 May 2025	• Initial version

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