AN14664

Coin Cell Hardware Recommendations for Kinetis Bluetooth LE Applications

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Document information

Information	Content
Keywords	AN14664, KW45, KW47, KW38, MCX W71, MCX W72
Abstract	This document describes some hardware and software solutions to minimize the peaks of current at the coin cell level.

1 Introduction

NXP Kinetis products (KW38/45/47 and MCX W71/72) are designed for Automotive, Industrial, and Internet of Things (IoT) applications, which may be supplied with coin cells. A typical example of a coin cell is CR2032.

This document describes some hardware and software solutions to minimize the peaks of current at the coin cell level. Such solutions are required due to the nature of the Bluetooth LE activity (a low-power mode to Active mode switching happens every few dozen milliseconds). The suitability of such a solution for an application depends on the radio power defined in the application.

These solutions are implemented on the KW4x evaluation boards. The schematics of the KW4x evaluation boards are available on www.nxp.com. This information is also available in the KW4x / MCX W7x Minimum Bill of Materials (BoM) PDFs attached to the following pages:

- The best way to build a PCB first time right with KW45 (Automotive) or K32W1/MCXW71 (IoT/Industrial) - NXP Community
- The best way to build a PCB first time right with KW47 (Automotive) or MCX W72 (IoT/Industrial) - NXP Community

2 Kinetis power configuration

KW4x / MCX W7x has a DC-DC converter embedded. This DC-DC converter can be set in Buck or Bypass mode. In DC-DC Buck mode, the output voltage can be set from 1.25 V to 2.5 V, depending on the radio output power (-30 dBm to +10 dBm). The Bluetooth LE sequence switches from a low-power mode (Deep-Sleep mode) to Active mode (Advertising, Connection, or Scan events). Switching the Kinetis product ON and OFF repeatedly may create peaks of current based on the defined radio output power.

The KW47 / MCX W72 products have the following new hardware features:

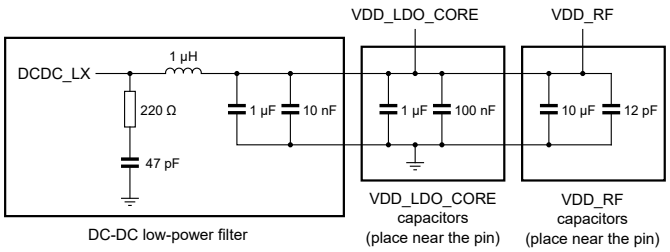
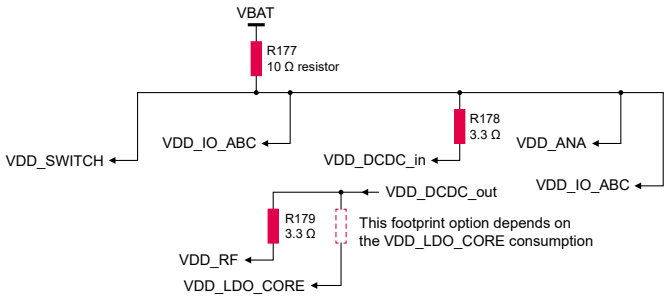
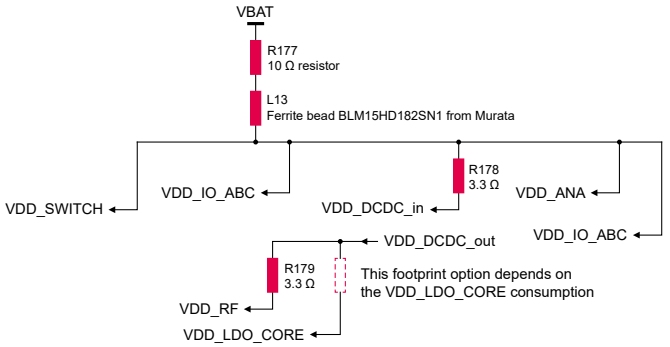
- The DC-DC Ramp can be trimmed to smooth the DC-DC output voltage to the desired value. This feature is implemented to avoid any peak of current at the coin cell level. KW45 / MCX W71 products do not have such a feature. Therefore, hardware recommendations are proposed to limit the peak of current below 10 mA, as recommended by coin cell manufacturers.
- The default POR DC-DC output voltage can be set in the bootloader. The default value is 1.8 V but it can be changed to 1.25 V or 1.35 V. For a coin cell application, the preferred value is 1.25 V.

These two features are not available in the KW45 / MCX W71 products. To reduce the peaks of current at the coin cell level and not to reduce the coin cell lifetime in these products, extra BoM is required.

3 Hardware solutions

Table 1 summarizes the hardware solutions for reducing peaks of current at the coin cell level. The suitability of a solution for an application depends on the radio power defined in the application.

Table 1. Hardware considerations for reducing peaks of current

Hardware consideration	Implementation
For all designs using coin cells, limit the DC-DC output capacitor values to 12 µF and use a 47 µF decoupling capacitor on the DC-DC input.	
For radio TX output power up to +7 dBm, add low serial resistors in line with the coin cell, in front of VDD_DCDC_in, and in front of VDD_RF.	 • Maximum TX output = +7 dBm • Maximum peak of current = 8 mA
For radio TX output power up to +10 dBm, add a ferrite bead in addition to the low serial resistors.	 • Maximum TX output = +10 dBm • Maximum peak of current < 1 mA

4 KW45 – Application configurations

This section describes the recommendations for minimizing the peaks of current on the coin cell while using the NXP Kinetis KW45 / MCX W71 products.

The radio TX output power defines the DC-DC output voltage. In a low-power mode, the DC-DC output voltage is set to 1.25 V. In Active mode (Advertising, Connection, or Scan events), the DC-DC output voltage is set as follows:

- 1.25 V for TX <= +0 dBm
- 1.8 V for +0 dBm < TX <= +7 dBm
- 2.5 V for TX > +7 dBm

Switching the DC-DC output from 1.25 V to 1.8 V or 2.5 V causes the charging/discharging of the capacitor bank and creates peaks of current. It is explained in detail for an application in the subsections that follow using these three use cases:

- Radio TX output power <= +0 dBm
- +0 dBm < radio TX output power <= +7 dBm
- Radio TX output power > +7 dBm

4.1 Radio TX output power <= +0 dBm (DCDC_output = 1.25 V)

When an application requires radio TX output power only up to +0 dBm, the DC-DC output voltage is set to 1.25 V. A low-power mode also needs the same voltage (1.25 V). Therefore, no peak of current occurs when a Bluetooth LE event switches from a low-power mode to Active mode. However, this use case has a constraint at power-on reset (POR). By default, at POR and at each reset, the DC-DC output voltage is equal to 1.8 V. Therefore, the bootloader must be updated to set the default DC-DC output voltage to 1.25 V. This way, only one peak occurs when the battery is replaced with another battery. No peak occurs during application reset.

The KW45B41Z-EVK schematics recommend using the following capacitors:

- A 1 µF decoupling capacitor at each of the DC-DC output and VDD_LDO_CORE
- A 10 µF capacitor at VDD_RF

Use these capacitance values for a coin cell application. It avoids overloading the DC-DC output.

The proposed hardware solution is shown in Figure 1.

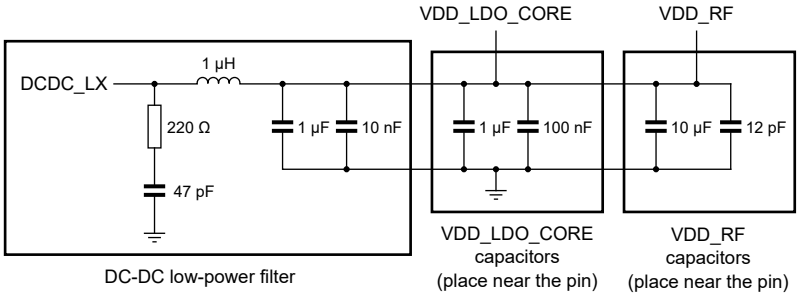


Figure 1. Hardware solution for TX <= +0 dBm

4.2 +0 dBm < radio TX output power <= +7 dBm (DCDC_output = 1.8 V)

When an application requires radio TX output power from +0.1 dBm up to +7 dBm, the DC-DC output voltage is set to 1.8 V. Because a low-power mode uses 1.25 V voltage, a voltage gap exists between a low-power mode and Active mode. If no action is taken to fix this issue, peaks of current occur when switching from a low-power mode to Active mode.

One software solution is to set the DC-DC output voltage to 1.8 V during a low-power mode. This simple solution avoids the peaks of current but reduces the battery life (due to consumption of 1.8 V instead of 1.25 V). Therefore, this solution is not a good solution.

Another solution, which is a preferred solution, is to add components on the PCB to reduce the peaks of current. A simple hardware solution is to add three low serial resistors as follows:

- A 10 Ω resistor in line with the coin cell
- A 3.3 Ω resistor in front of VDD_DCDC_in
- Another 3.3 Ω resistor in front of VDD_RF

Also, one footprint can be added (if necessary) in line with VDD_LDO_CORE.

These values can be fine-tuned if the overall current at VBAT is too high and can create a voltage drop that is large enough to reach the brownout (reset threshold) of the KW45 device.

When used with the SDK LP_peripheral and LP_central applications, the proposed resistor values do not reach the reset threshold in voltage (VBAT = 2.4 V minimum) and temperature (-40 °C to +125 °C). The maximum peak of current measured is 8 mA.

In this use case (radio TX output power level), the POR creates a peak of current when the battery is replaced with another battery. This use case implementation has negligible impact on the total battery life.

The proposed hardware solution is shown in Figure 2.

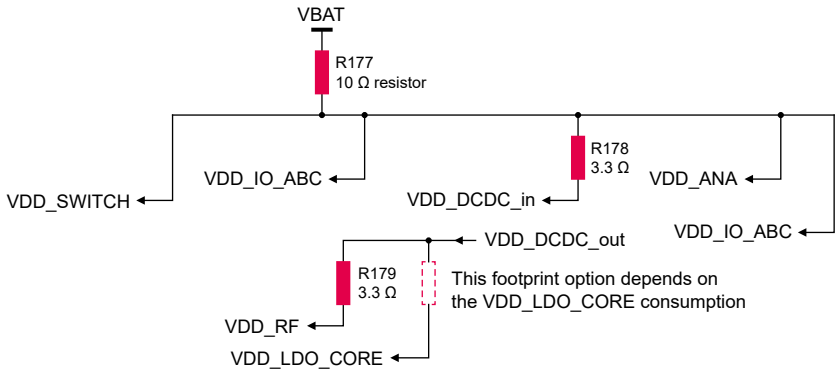


Figure 2. Hardware solution for +0 dBm < TX <= +7 dBm

4.3 Radio TX output power > +7 dBm (DCDC_output = 2.5 V)

When an application requires radio TX output power from +7.1 dBm to +10 dBm, the DC-DC output voltage is set to 2.5 V. Because a low-power mode uses 1.25 V voltage, a voltage gap exists between a low-power mode and Active mode. If no action is taken to fix this issue, peaks of current occur when switching from a low-power mode to Active mode.

One software solution is to set the DC-DC output voltage to 2.5 V during a low-power mode. This simple solution avoids the peaks of current but reduces battery life significantly (due to consumption of 2.5 V instead of 1.25 V). Therefore, this solution is not a good solution.

Another solution, which is a preferred solution, is to add a ferrite bead to the second hardware solution described in Section 4.2. Therefore, the hardware solution involves adding the following components:

- A ferrite bead (for example, BLM15HD182SN1 from Murata) and a low serial resistor (10 Ω) in line with the coin cell
- A 3.3 Ω resistor in front of VDD_DCDC_in
- Another 3.3 Ω resistor in front of VDD_RF

Also, one footprint can be added (if necessary) in line with VDD_LDO_CORE.

These values can be fine-tuned if the overall current at VBAT is too high and can create a voltage drop that is large enough to reach the brownout (reset threshold) of the KW45 device. In this solution, the maximum peak of current measured is below 1 mA.

When used with the SDK LP_peripheral and LP_central applications, the proposed resistor values do not reach the reset threshold in voltage (VBAT = 2.4 V minimum) and temperature (-40 °C to +125 °C). The maximum peak of current measured is 8 mA.

In this use case (radio TX output power level), the POR creates a peak of current when the battery is replaced with another battery. This use case implementation has negligible impact on the total battery life.

The proposed hardware solution is shown in Figure 3.

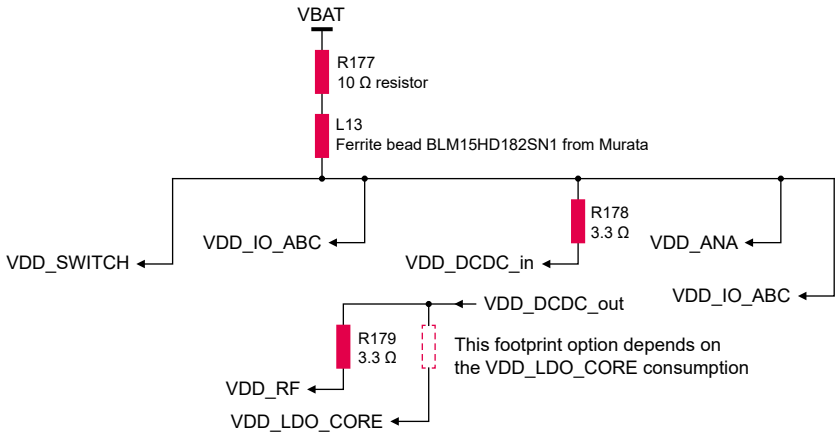


Figure 3. Hardware solution for +7 dBm < TX <= +10 dBm

5 KW47 – Application configurations

KW47 / MCX W72 products have two new hardware features that help reduce/suppress the peaks of current when switching from a low-power mode to Active mode in Bluetooth LE events (Advertising, Connection, or Scan events).

5.1 DC-DC Ramp trim

A new feature, *DC-DC Ramp trim*, allows you to smooth the DC-DC output voltage to the desired voltage value. This feature is implemented to avoid any peak of current at the coin cell level. It is implemented using the RAMP_CNTRL and RAMP_CNTRL_EN bit fields of the DCDC Configuration (DCDC_CFG) register of the KW47 device.

By default, this feature is disabled. SDK applications LP_peripheral and LP_central provide an option to enable this feature. It can be enabled using the `gBoardDcdcRampTrim_c` parameter in the `board_platform.h` file as follows:

```
/*! \brief Increase DCDC voltage with a ramp to avoid peak of current when
 *          DCDC output is set to higher voltage.
 *
 * \details gBoardDcdcRampTrim_c can vary between 0 and 7
 *          gBoardDcdcRampTrim_c = 0 means feature disabled
 *          gBoardDcdcRampTrim_c = 1 is the smoothest ramp
 *          gBoardDcdcRampTrim_c = 7 is the steepest ramp
 *
 * \note Cannot be applied when switching between low-power DCDC configuration
 *       and active configuration.
 *       The DCDC ramp feature is only functional when the SPC is configured in
 *       Normal drive strength.
 *       The NBU core will handle the switch to the targeted
 *       DCDC output voltage. The targeted voltage will depend on
 *       the TX output power requested by the application.
 *       After exiting low-power, the NBU core will request the high power mode.
 *       After that, it will wait for the transition to be over and the
 *       targeted voltage to be reached before resuming any other activities.
 *       The smoothest the ramp is, the longer the low-power exit procedure will
 *       take time. The value 3 is a good trade-off between peak of current and
 *       low-power exit duration.
 */
```

```
//#define gBoardDcdcRampTrim_c 3

/*! \brief  Enable the high power mode configuration to activate the
 *          dynamic DCDC output voltage switching when TX output power is less
 *          or equal to 7dBm.
 *
 * \details The NBU requires higher DCDC output voltage for radio transmits for
 *          output power between 0dBm and 7dBm. It will adapt the
 *          DCDC output voltage depending the required TX power.
 *          - benefit : The DCDC output voltage does not have to increase
 *          as much as needed by the Tx ouput power requested when only the
 *          main power domain is active.
 *
 * \note limitation : NBU cannot switch to 2.5V by itself via
 *       high power mode voltage, a setting on SPC is also required.
 *       NBU will not be able to handle TX power higher than 7dBm as it requires
 *       2.5V on the DCDC output voltage.
 */
//#define gBoardDcdcEnableHighPowerModeOnNbu_d 1
```

Figure 4 shows the RAMP_CNTRL and RAMP_CNTRL_EN descriptions in KW47 Reference Manual.

Diagram

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0								RAMP_CNTRL			RAMP_CN...	BLEED_EN	VOUT 2P5...	0	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		FREQ_CNTRL						0				0			FREQ_CN...
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields

Field	Function
31-24 —	Reserved
23-21 RAMP_CNTRL	DCDC Ramp Control Select Controls and selects the DCDC Voltage ramp rate when switching DCDC trim for a higher voltage level. NOTE DCDC Ramp Rate = [567-(DCDC Ramp Trim*2 - DCDC Ramp Trim/2)]/2^RAMP_CNTRL NOTE DCDC Ramp Trim is the internal trim value changing by one lsb after every DCDC RAMP Rate delay
20 RAMP_CNTRL_EN	DCDC Trim Step Enable Enables DCDC trim voltage stepping.

Figure 4. RAMP_CNTRL and RAMP_CNTRL_EN descriptions in Reference Manual

5.2 Peak current measurement results

This section describes how peak current can be reduced by changing the DC-DC Ramp trim configuration.

When the DC-DC Ramp control is disabled, the maximum peak current is 33 mA, as shown in Figure 5.

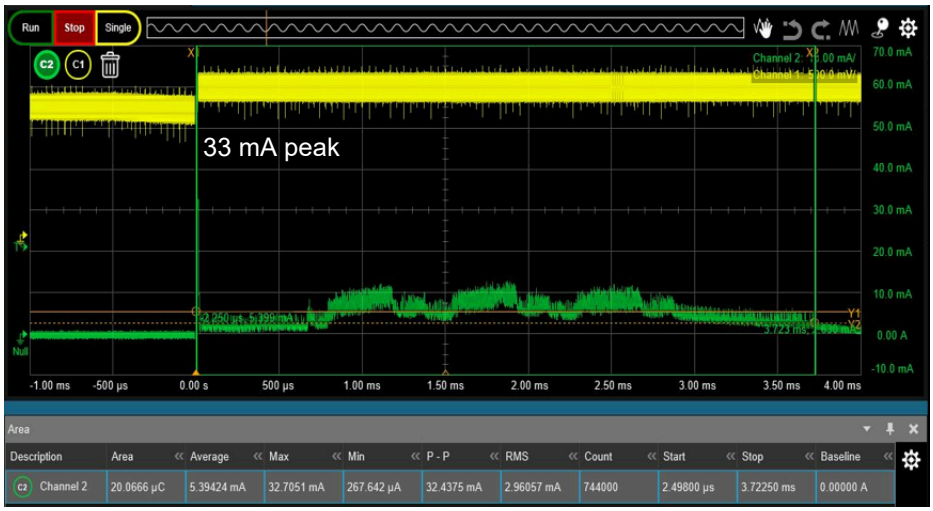


Figure 5. DC-DC Ramp control disabled

When the DC-DC Ramp control is enabled and DCDC_RAMP_CNTRL = 7, the maximum peak current is 19 mA, as shown in Figure 6.

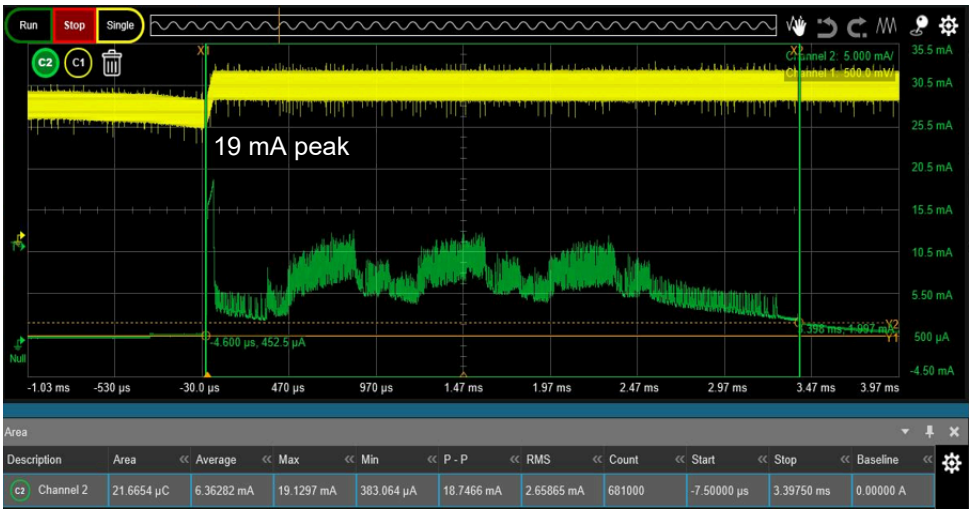


Figure 6. DC-DC Ramp control enabled and DCDC_RAMP_CNTRL = 7

When the DC-DC Ramp control is enabled and DCDC_RAMP_CNTRL = 6, the maximum peak current is still 19 mA, as shown in Figure 7.

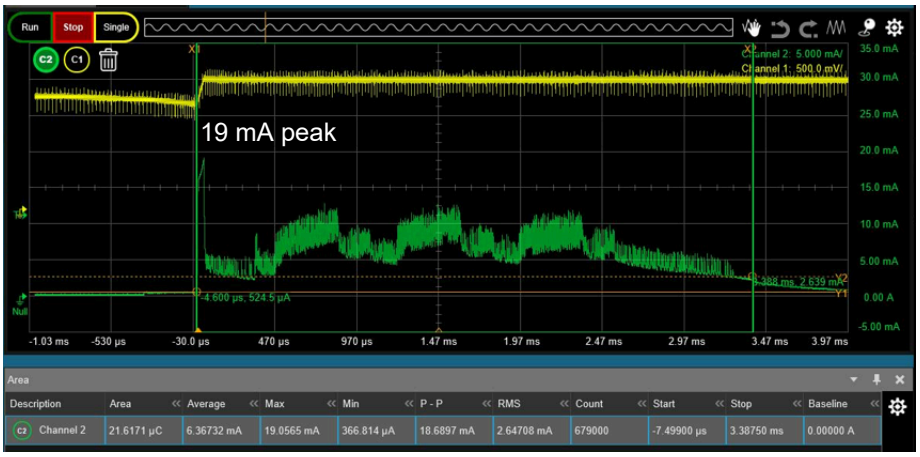


Figure 7. DC-DC Ramp control enabled and DCDC_RAMP_CNTRL = 6

When the DC-DC Ramp control is enabled and DCDC_RAMP_CNTRL = 5, the maximum peak current is 15 mA, as shown in Figure 8.

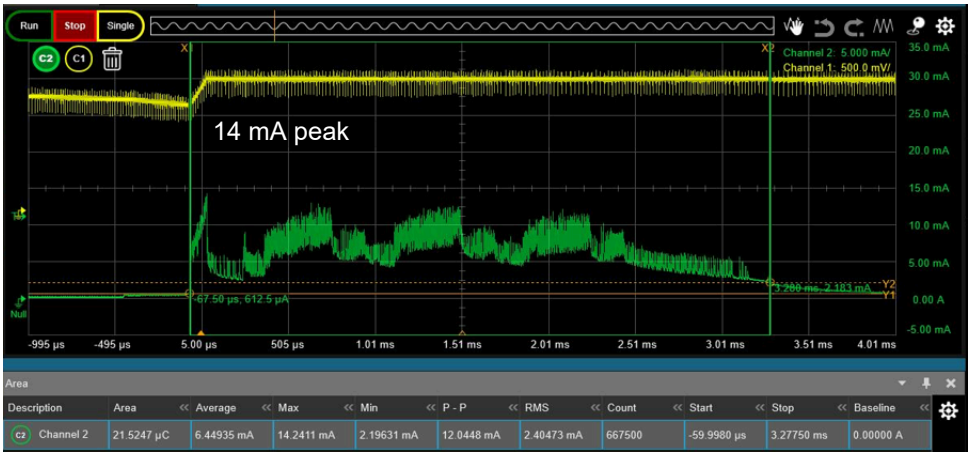


Figure 8. DC-DC Ramp control enabled and DCDC_RAMP_CNTRL = 5

When the DC-DC Ramp control is enabled and DCDC_RAMP_CNTRL = 4, the maximum peak current is 11 mA, as shown in Figure 9.

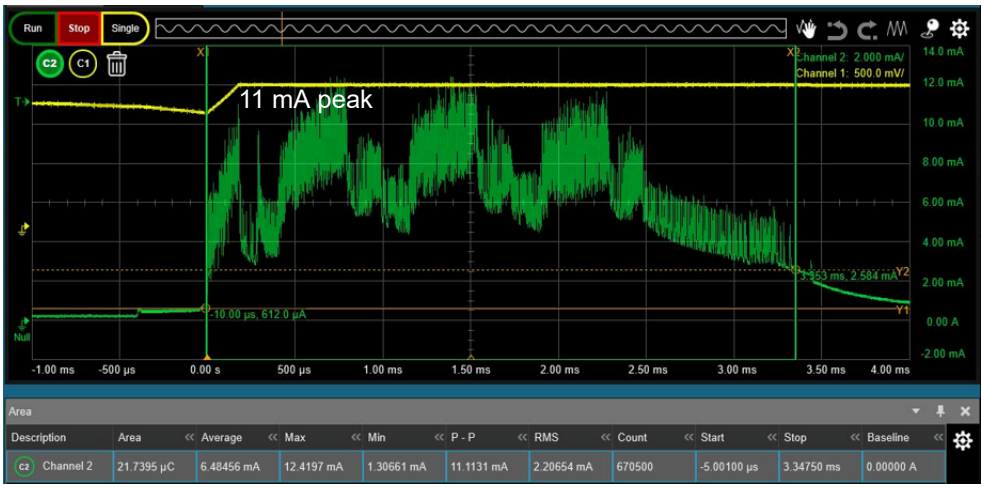


Figure 9. DC-DC Ramp control enabled and DCDC_RAMP_CNTRL = 4

When the DC-DC Ramp control is enabled and DCDC_RAMP_CNTRL <= 3, no peak current occurs, as shown in Figure 10, Figure 11, and Figure 12.

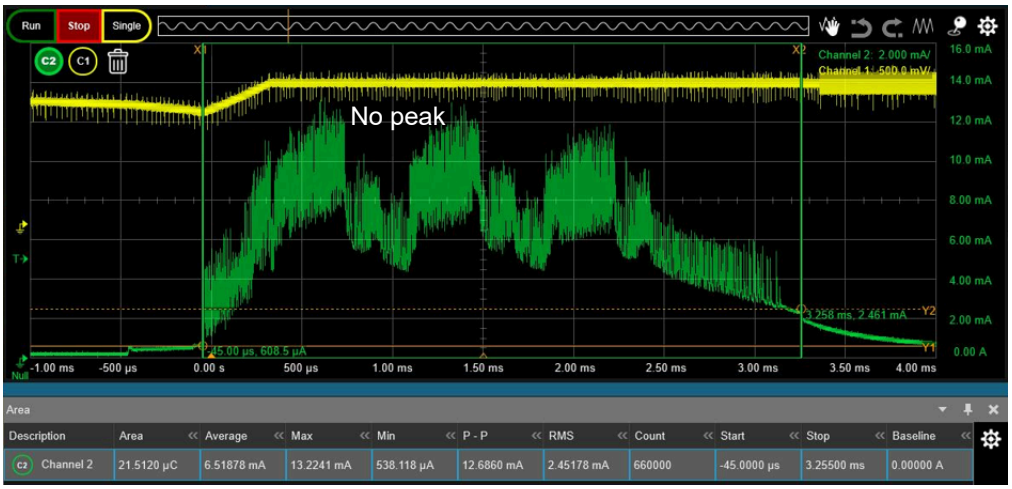


Figure 10. DC-DC Ramp control enabled and DCDC_RAMP_CNTRL = 3

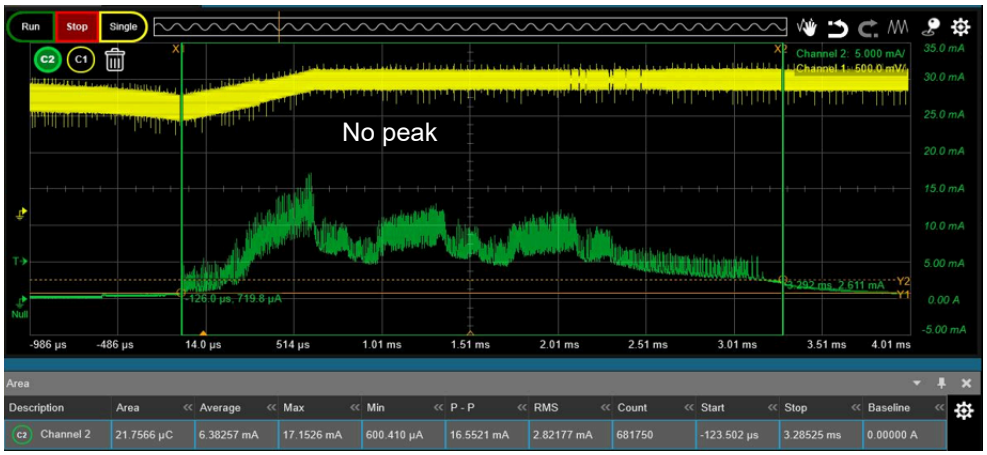


Figure 11. DC-DC Ramp control enabled and DCDC_RAMP_CNTRL = 2

Figure 12. DC-DC Ramp control enabled and DCDC_RAMP_CNTRL = 1

Table 2 provides the peak current and other measurement results for different DC-DC Ramp trim configurations.

Table 2. Measurement results

RAMP_CNTRL_EN and RAMP_CNTRL	Peak current level (mA)	Peak duration (µs)	DC-DC Ramp duration (µs)	Advertising duration (ms)	Advertising energy (µC)
EN = 0, CNTRL = x	33 mA	16	Not applicable	3.724	20.06
EN = 1, CNTRL = 7	19 mA	40	40	3.395	21.66
EN = 1, CNTRL = 6	19 mA	40	40	3.392	21.62
EN = 1, CNTRL = 5	14 mA	97	97	3.347	21.52
EN = 1, CNTRL = 4	11 mA	185	185	3.362	21.73
EN = 1, CNTRL = 3	**No peak**	**No impact on TX**	**365 < preprocessing time**	**3.302**	**21.51**
EN = 1, CNTRL = 2	No peak	First TX impacted	765 > preprocessing time	3.305	21.75

Table 2. Measurement results...*continued*

RAMP_CNTRL_EN and RAMP_CNTRL	Peak current level (mA)	Peak duration (µs)	DC-DC Ramp duration (µs)	Advertising duration (ms)	Advertising energy (µC)
EN = 1, CNTRL = 1	No peak	2x TX impacted	1518 > preprocessing time	3.235	20.53
EN = 1, CNTRL = 0	No peak	2x TX impacted	1562 > preprocessing time	3.290	20.77

5.3 IFR default DC-DC output voltage

The default power-on reset (POR) DC-DC output voltage can be set in the bootloader. The default value is 1.8 V but it can be changed to 1.25 V or 1.35 V. 1.25 V is the preferred voltage for a coin cell application.

The DC-DC glitch at POR can be resolved by changing the default information register (IFR) DC-DC output voltage from 1.8 V to 1.25 V or 1.35 V.

In the IFR, the default voltage value is 1.8 V. You can change it to either 1.25 V or 1.35 V, depending on the selected boot speed. Figure 13 shows the default boot configuration settings from KW47 Reference Manual.

0x0050	1	Boot Configuration	Bit 0 - Enable ISP or not • 0 = BOOT_CFG pin disabled • 1 = BOOT_CFG pin enabled (default) Bit 2:1 – Boot speed • 00 = Normal boot (48 MHz) • 10 = Fast Boot (96 MHz) • 01, 11 = Normal boot (default) Bit 3 – DCDC boot power mode • 0 = Lower power boot mode • 1 = Normal power mode See Table 59 for more details. bit 7:4 – Reserved
	15	Reserved	Reserved

Figure 13. Default boot configuration settings from Reference Manual

6 Acronyms

Table 3 lists the acronyms used in this document.

Table 3. Acronyms

Acronym	Description
BoM	Bill of materials
IFR	Information register
LE	Low Energy

Table 3. Acronyms...*continued*

Acronym	Description
POR	Power-on reset

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8 Revision history

Table 4 summarizes the revisions to this document.

Table 4. Revision history

Document ID	Release date	Description
AN14664 v.1.1	10 December 2025	Initial public release
AN14664 v.1.0	7 May 2025	Initial NDA release

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