AN14387

MCXW71 - Power Management Hardware

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Document information

Information	Content
Keywords	AN14387, MCXW71, power configurations, power domains
Abstract	This application note describes the use of different modules dedicated to power management in the MCXW71 microcontroller.

1 Introduction

This application note describes the use of different modules dedicated to power management in the MCXW71 microcontroller. MCXW71 integrates a DC-DC buck converter, a couple of low-dropout regulators, and a programmable solid-state switch to turn on/off the MCXW71 power domains. Also, the MCXW71 integrates independent power domains for each group of hardware. For example, there is a dedicated power domain for the reset hardware, GPIOs, and analog. The dedicated hardware for power management and the possibility to have independent voltages for each power domain gives the flexibility to meet most of the application requirements in the wireless applications.

2 MCXW71 power domains

The MCXW71 microcontroller has independent power domains, which are grouped as follows:

- VDD_SWITCH: Represents the input voltage for the smart power switch (VBAT). This power domain supplies the voltage to the internal hardware associated with the VBAT.
- VDD_ANA: Drives the analog peripherals on this microcontroller, such as the analog-to-digital converter (ADC) and the VREF regulator.
- VDD_IO_ABC: Drives the voltage on the PTA, PTB, and PTC pins.
- VDD_IO_D/VDD_DCDC: Drives the voltage on the PTD pins, including the reset system. It is also shared with the inputs for the DC-DC Buck converter, and for the LDO_SYS regulator.
- VDD_SYS: Manages the power delivered to some peripherals on this chip. See Table 1 for the list of peripherals supplied by this domain.
- VDD_CORE: The core-power domain supplies to the main core processor and some peripherals on this chip. This power domain is split into core main, core wake, and core radio domains for an independent power mode selection. The voltage on this power domain is associated with the maximum clocking frequency at which this device can operate. See Table 1 for the list of peripherals supplied by this domain.
- VDD_RF: The RF power domain provides the voltage that drives the radio analog system in this chip and the 32 MHz-OSC oscillator.
- VDD_PA_2.4G: Drives the voltage for the radio power amplifier. The VDD_PA_2.4G voltage can be provided internally from the VDD_RF power domain.

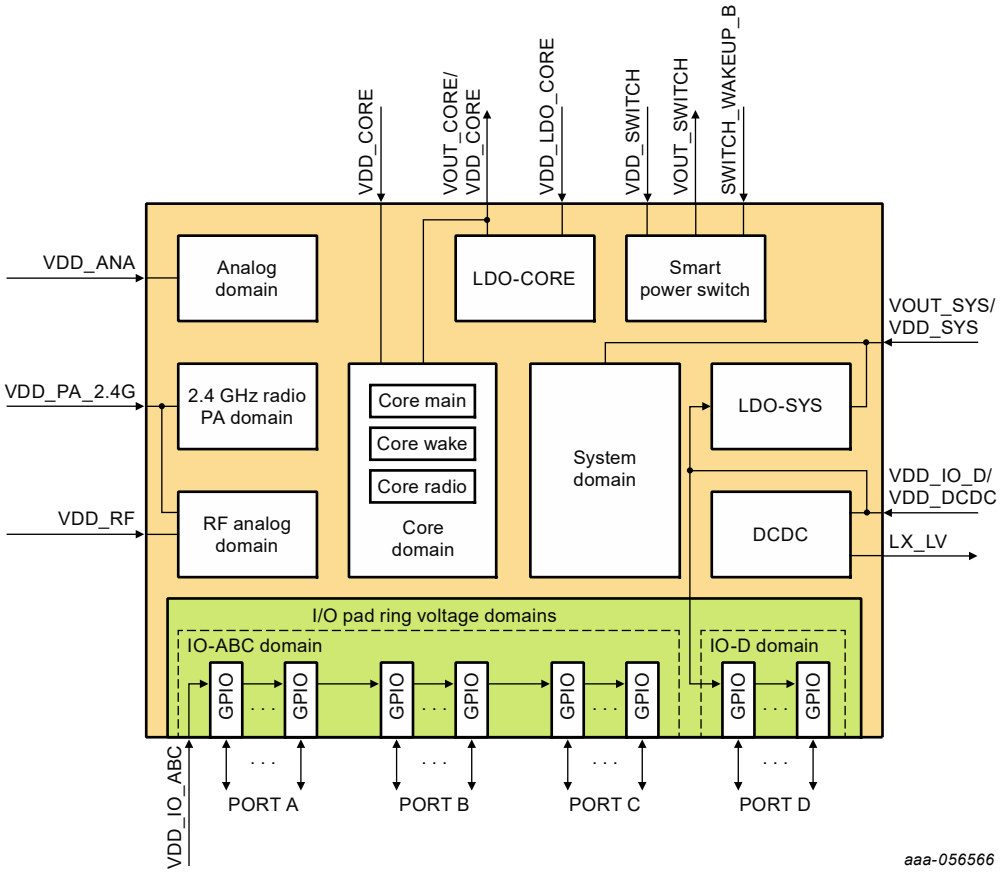


Figure 1. MCXW71 power domain block diagram

2.1 Peripherals supplied by each power domain

Table 1 shows the MCXW71 power domains and their associated on-chip peripherals supplied by each domain.

Table 1. Peripheral power domain assignments

Power domain	Voltage supply	Modules associated with the power domain
Analog domain	VDD_ANA VSS_ANA	ADC0 VREF0
Core main	VDD_CORE_MAIN (Tied internally to VDD_CORE pin)	CM33, DSP, FPU, MPU, NVIC, SYSTICK TZM, DAP, DWT, ITM, TPIU, AXBS0, eDMA0, MSCM, SMSCM PRBRIGDE2, TRGMUX, MRCC, SFA0, CACHE-CODE FLASH, ROM, BOOT, CRC0, EdgeLock Secure Enclave TRDC0, LPIT0, TPM1, FlexCAN0, FlexIO0 LPI2C1, I3C0, LPSPI 1, LPUART1, GPIOB/C, SEMA42, PORTB/C, ADC0, VREF0, and TCM-SYS
Core wake	VDD_CORE_WAKE (Tied internally to VDD_CORE pin)	SWD, CMC0, EWM0, WDOG0/1, FRO-6M, MRCC, SCG0, TSTMR0, TPM0, LPI2C0, LPUART0, LPSPI0, GPIOA, PORTA, and LPCMP0/1
Core radio	VDD_CORE_2.4G	RF-2.4G, NBU, RF-FMU, RF-FRO192M

Table 1. Peripheral power domain assignments*...continued*

Power domain	Voltage supply	Modules associated with the power domain
	(Tied internally to VDD_CORE pin)	
IO-ABC	VDD_IO_ABC	PORTA, PORTB, PORTC, LPCMP0/1
IO-D	VDD_IO_D	LDO-SYS, DC-DC, PORTD
Smart power switch	VDD_SWITCH	Power switch, RAM LDO, FRO16K, power switch controller
System	VDD_SYS	RFMC0, Bluetooth LE LL (from MBU), WUU0, FRO192M, LPTMR0/1, SPC0, OSC-RTC, FRO32K, REGFILE0/1 – RTC, TAMPER, RTC0, GPIOD, PORTD
RF analog	VDD_RF	OSC-RF, RF-2.4G
2.4 GHz Radio PA	VPA_2.4G	RF-PA-2.4G

MCXW71 includes hardware dedicated to power management embedded in the chip. Table 2 shows a brief description of the regulators available on this MCU.

Table 2. On-chip regulator description

On-chip regulator	Voltage supply	Description
DC-DC	VDD_DCDC	DC-DC can be used to power the LDO-SYS, I/O ring, RF analog, and 2.4 GHz radio power amplifier. It also powers the external components. The user must consider that the total load current expected never exceeds the maximum DC-DC current capacity. The DC-DC current capacity depends on the DC-DC Drive mode.
LDO-CORE	VDD_LDO_CORE	LDO-CORE can be used to power the VDD_CORE domain. It is not intended to supply external loads.
LDO-SYS	VDD_IO_D	The LDO-SYS can be used to power the VDD_SYS domain. It is not intended to supply external loads.

Table 3 shows the supported voltage options for each on-chip regulator.

Table 3. On-chip regulator voltages

On-chip regulator	Voltage options
DC-DC	1.25 V, 1.35 V, 1.8 V, and 2.5 V[1]
LDO-CORE	1.05 V, 1.1 V, and 1.15 V
LDO-SYS	1.8 V and 2.5 V[2]

[1] The DC 2.5 V option is only available in DC-DC Normal Drive Strength mode.
[2] Do not enable the LDO-SYS 2.5 V option while the application is running. This option is intended only to program the eFuses.

2.2 Power domain rates

Table 4 shows the maximum and minimum DC voltage requirements for each power domain in MCXW71 MCUs.

Table 4. Power domain rates

Power domain	Voltage supply	Minimum	Maximum	Unit
Core domain	VDD_CORE: • Mid Drive (1.05 V)	1.0 1.04	1.1 1.21	V

Table 4. Power domain rates*...continued*

Power domain	Voltage supply	Minimum	Maximum	Unit
	• Normal Drive (1.1 V) • Safe-mode (1.15 V)	1.04	1.21	
System domain	VDD_SYS: • Normal mode • Fuse programming	1.8 2.25	1.98 2.75	V
IO-ABC domain	VDD_IO_ABC	1.71	3.6	V
IO-D domain	VDD_IO_D	1.86	3.6	V
Smart power switch	VDD_SWITCH	1.9	3.6	V
RF analog domain	VDD_RF	1.175	3.6	V
2.4 GHz radio PA	VPA_2.4G	0.9	2.4	V
Analog domain	VDD_ANA	1.71	3.6	V

3 MCXW71 power configurations

The MCXW71 microcontroller has independent power domains, allowing various power configurations. You can implement any power configuration depending on the voltage required on each power domain, according to the needs of the application. For more information on DC voltage requirements for each power domain in MCXW71, refer to Section 2.2.

The purpose of this section is to show the most common power configurations, advantages, and considerations.

3.1 MCXW71 Bypass mode configuration

This section describes the MCXW71 Bypass mode configuration as follows:

- The MCXW71 Bypass mode disables the DC-DC and directly connects each power domain to a unique power supply.
- This configuration is the lowest-cost hardware implementation due to the small number of external components required.
- However, this configuration does not allow you to have independent voltages on each power domain, and therefore, has the highest power consumption.
- In this configuration, the following is recommended:
  - Disable the DC-DC
  - Clear the SPC -> CNTRL[DCDC_EN] = 0
  - Leave the DCDC_LX pin (DC-DC output pin) floating in the design

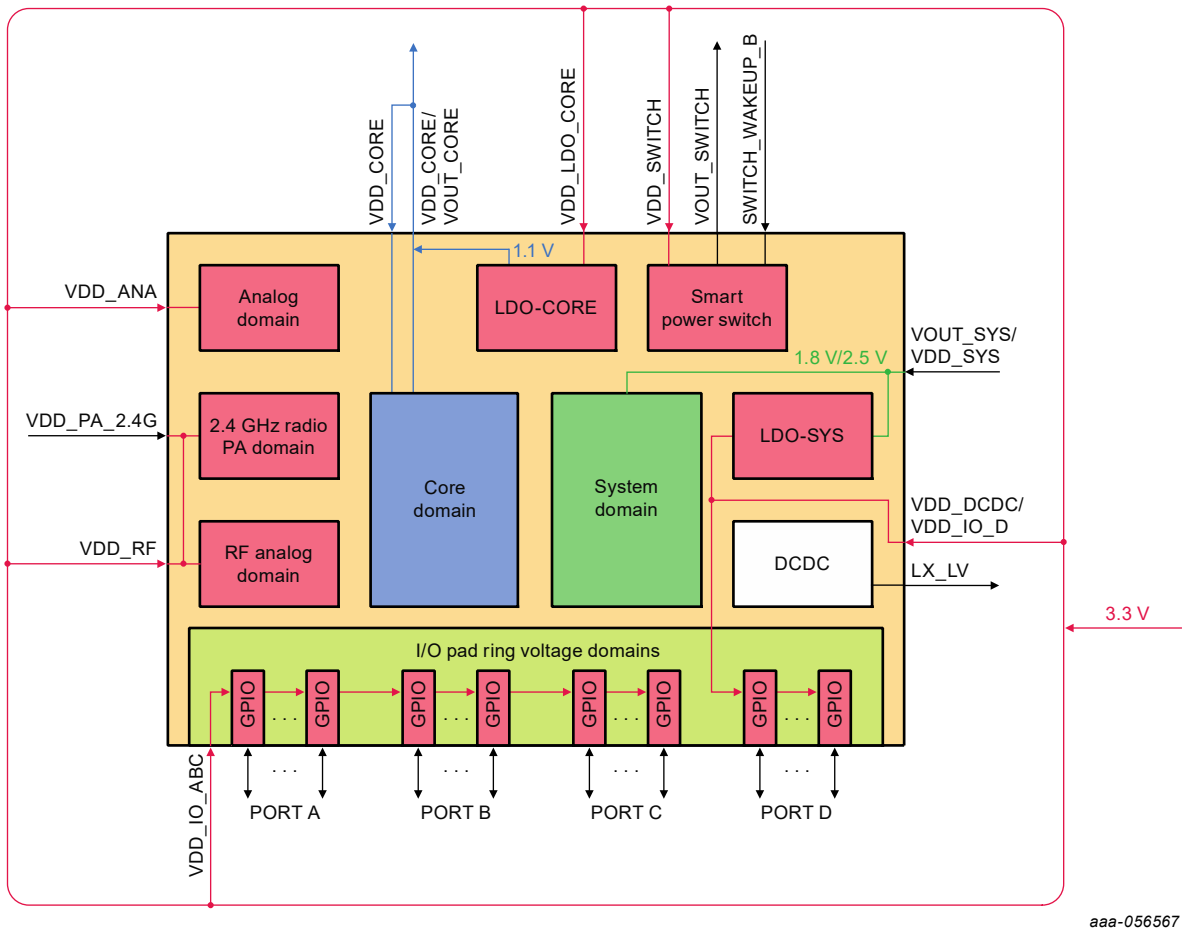


Figure 2. MCXW71 Bypass mode configuration

3.2 MCXW71 DC-DC Buck mode configuration

This section describes the MCXW71 DC-DC Buck mode configuration as follows:

- The DC-DC Buck mode configuration provides the best balance in power consumption and cost. As a consequence, this mode is the most-used configuration.
- In DC-DC Buck mode, a single power supply is used to deliver power to many power domains including the DC-DC input.
- The DC-DC output can provide a different configurable voltage for the RF domain and LDO-CORE.
- The DC-DC output is targeted to deliver the voltage needed for the RF power domain to reach up to +10 dBm TX output power.
- It is also possible to decrease the DC-DC output voltage as a power-saving mechanism while the RF domain is idle.
- The DC-DC can also be used to feed external circuitry.

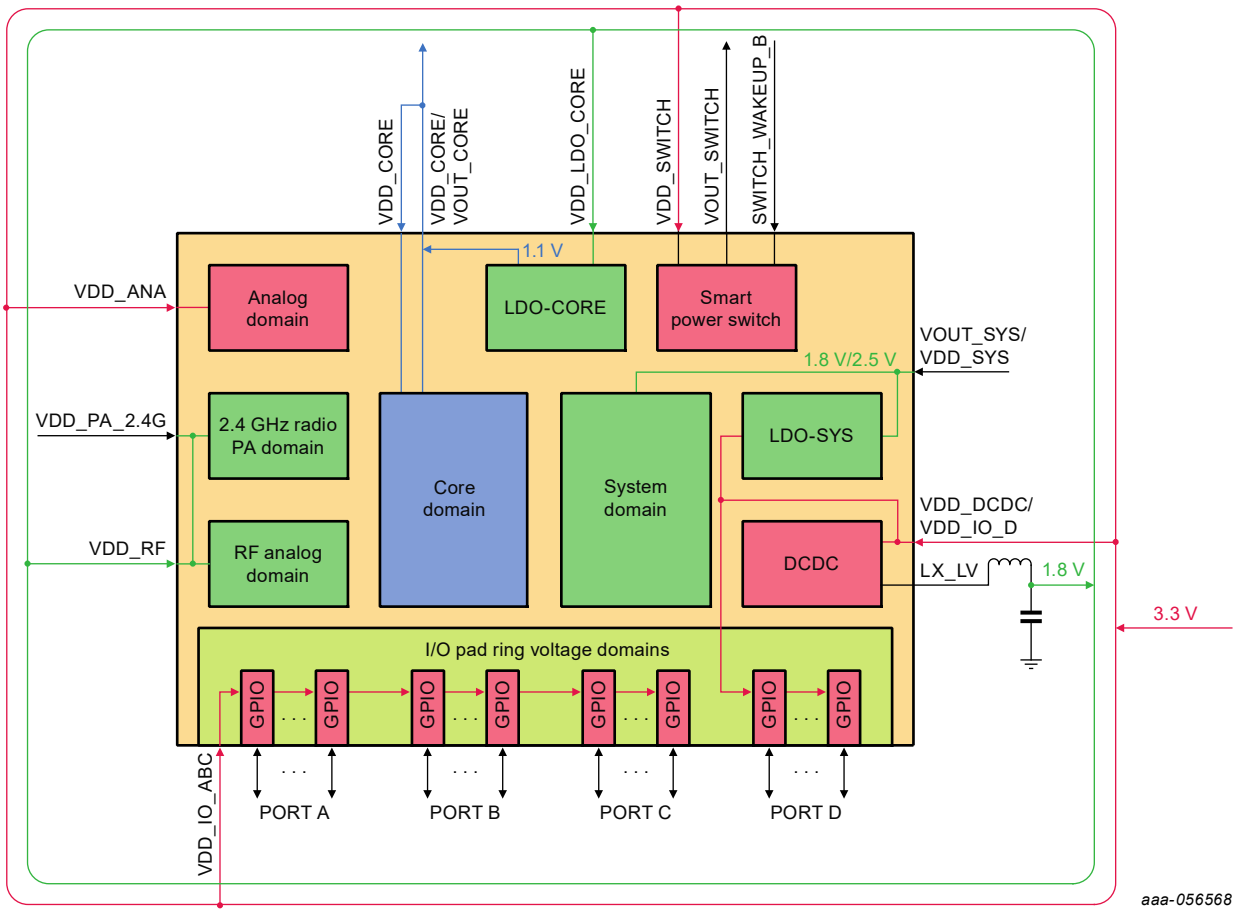


Figure 3. MCXW71 DC-DC Buck mode configuration

3.3 MCXW71 PMIC mode configuration

This section describes the MCXW71 PMIC mode configuration as follows:

- This configuration is intended to disable the on-chip regulators and directly connect each power domain to a different power supply through a power management-integrated circuit (PMIC).
- This configuration allows for independent power supply control based on the needs of each power domain, leading to optimal power consumption.

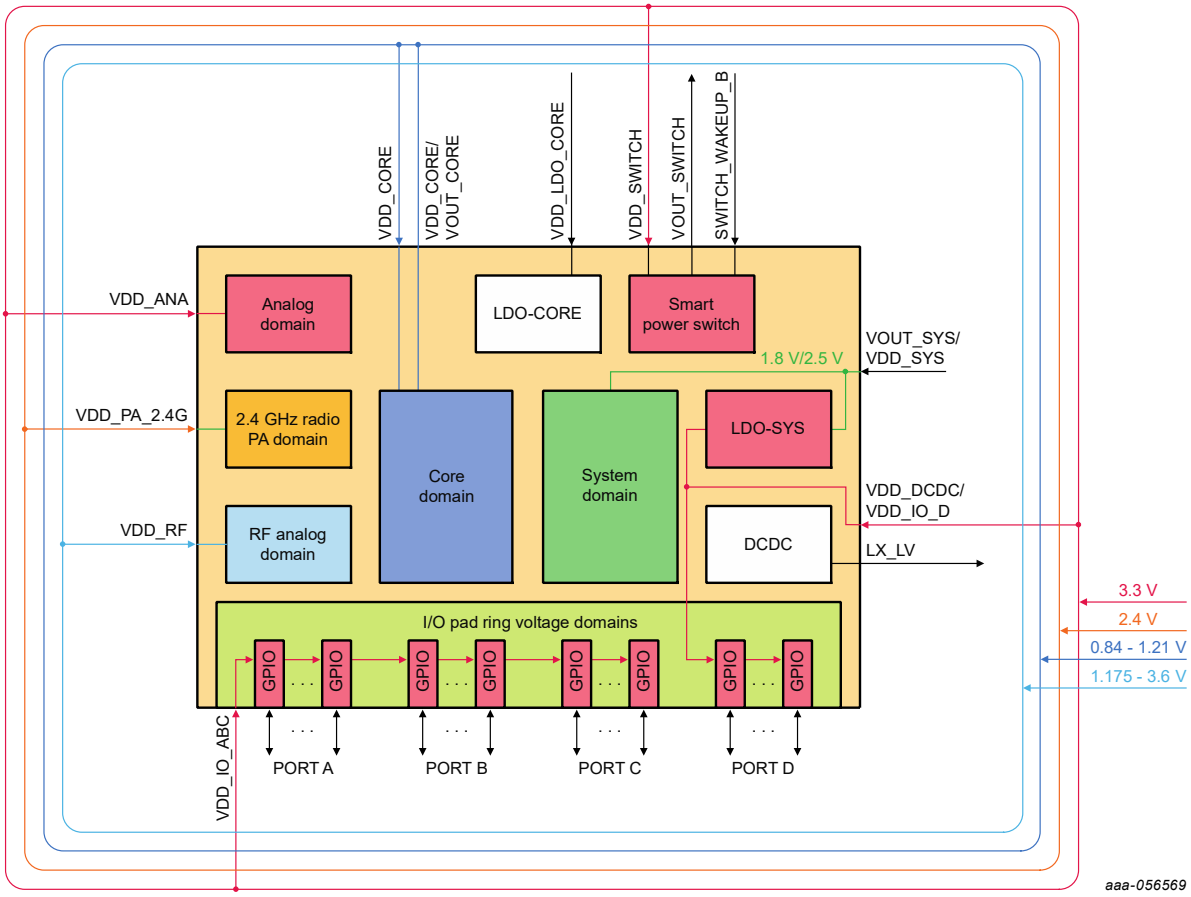


Figure 4. MCXW71 PMIC configuration

3.4 MCXW71 DC-DC mode controlled with smart power switch

This section describes the MCXW71 DC-DC mode controlled with the smart power switch as follows:

- The smart power switch (VBAT) is a low-resistance solid-state switch that works with the power management system to implement power-saving mechanisms.
- It provides two band gap timers and an LDO voltage regulator dedicated to supply the retention SRAM while the rest of the MCU remains switched off.
- The smart power switch can be used to turn off all the MCU or some specific power domains to obtain an optimized power consumption.
- The smart power switch can be used to switch on/off external circuitry with a low-dropout voltage as well.
- In this mode, the smart power switch domain (VDD_SWITCH), is the only voltage domain required to be powered permanently.
- The software can disable the smart power switch and enable it using any of the VBAT band gap timers or a falling edge on the SWITCH_WAKEUP_B pin.

Figure 5 shows the configuration with the smart power switch as follows:

- The external 3.3 V power source supplies the smart power switch.
- Its output is connected to the DC-DC, LDO-SYS, VDD_ANA, VDD_IO_D, and VDD_IO_ABC.
- The DC-DC output is connected to the LDO-CORE and VDD_RF.

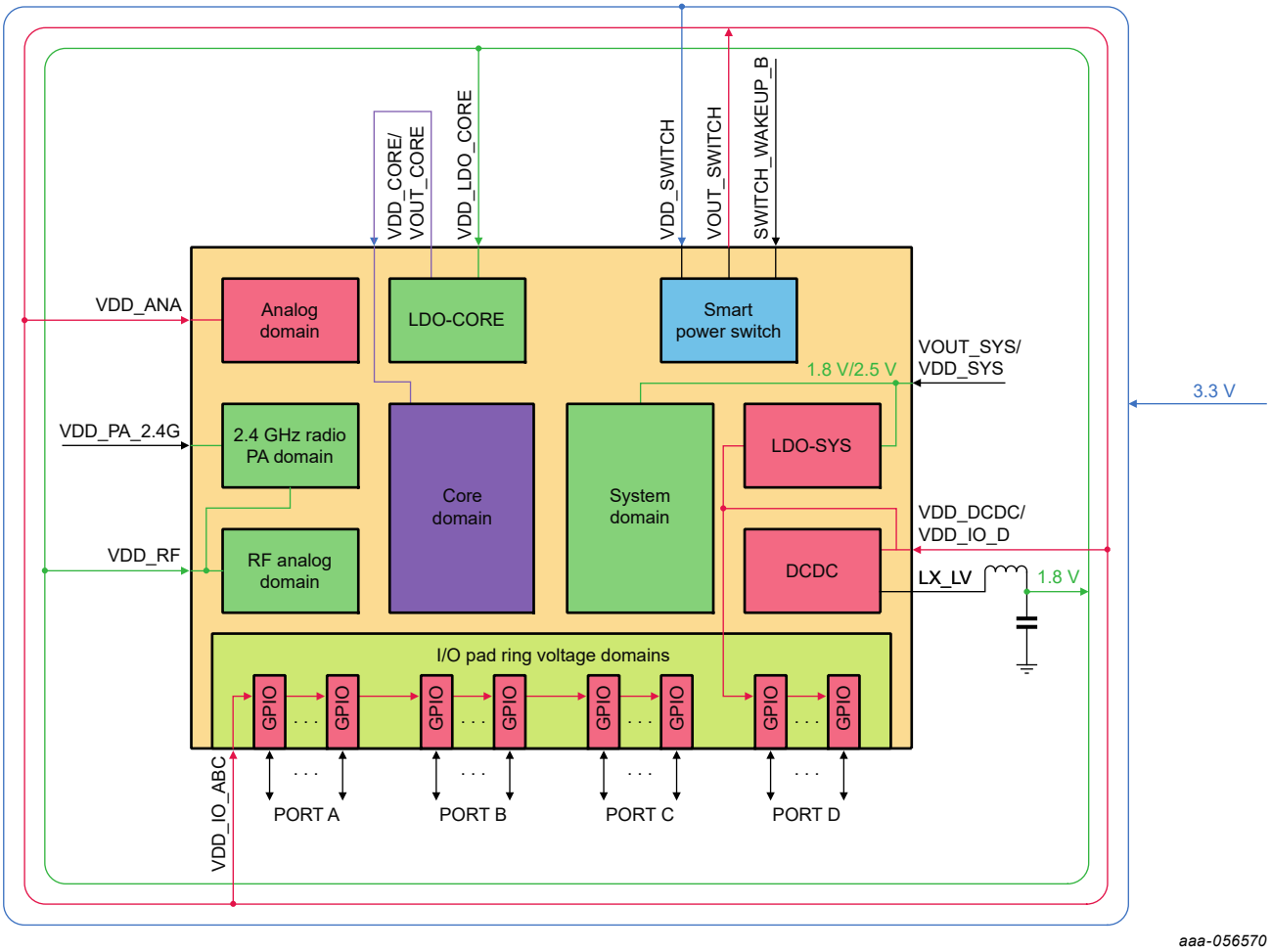


Figure 5. Power all domains with a smart power switch

Figure 6 shows the configuration with the smart power switch as follows:

- The external 3.3 V power source supplies the smart power switch and VDD_DCDC/VDD_IO_D.
- Its output is connected to VDD_ANA and VDD_IO_ABC.
- The DC-DC output is connected to the LDO-CORE and VDD_RF.

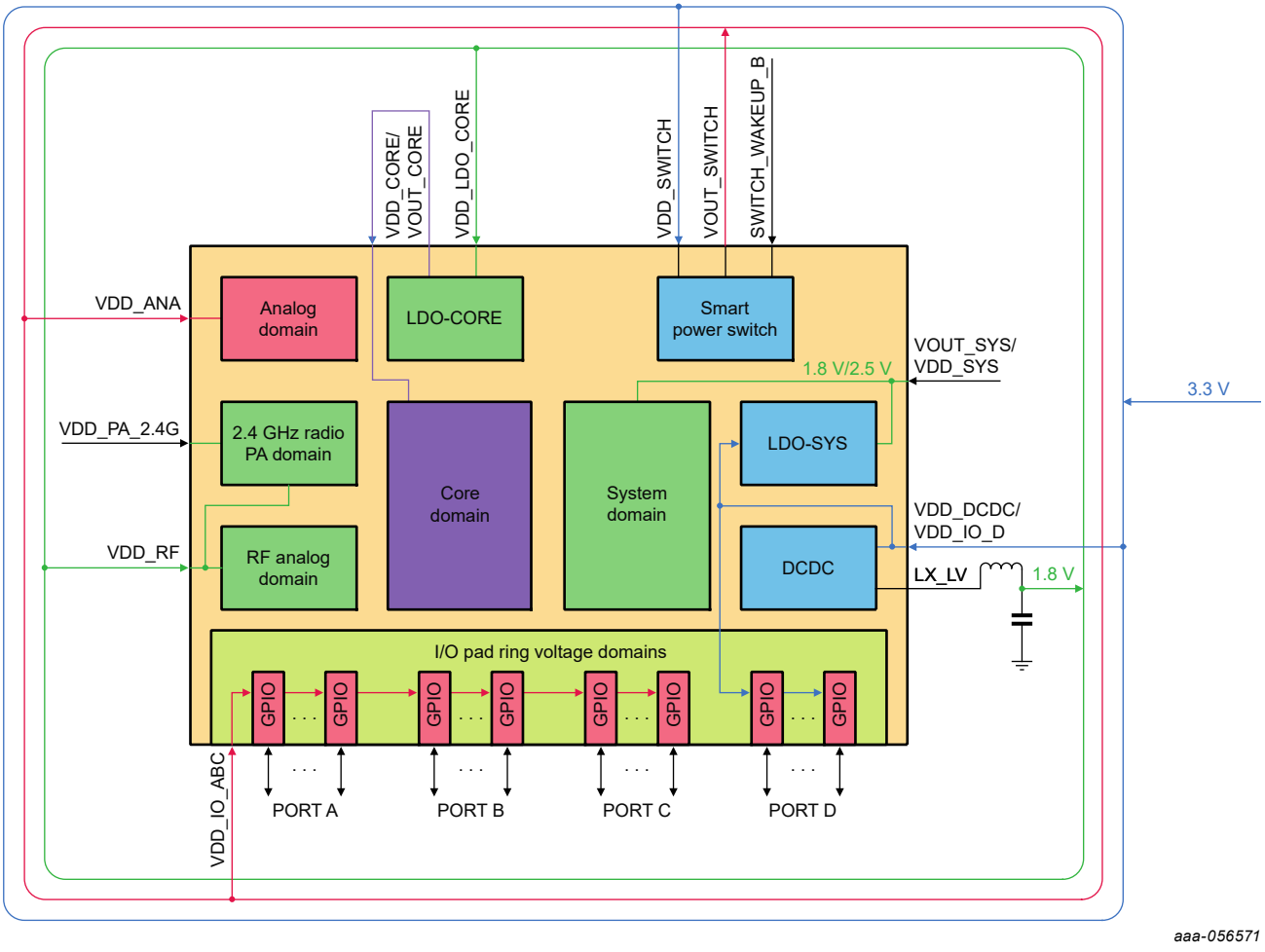


Figure 6. Power all supplies except VDD_IO_D and VDD_DCDC

4 DC-DC buck converter

This section describes the characteristics, features, and operation of the DC-DC buck converter.

4.1 Enabling and disabling DC-DC buck converter

The DC-DC buck converter can be enabled and disabled according to the application configuration and requirements. The SPC regulator control register (CNTRL) can enable or disable the DC-DC on-chip converter by writing the SPC -> CNTRL[DCDC_EN] = 0. By default, the DC-DC is enabled. However, if your design is bypassing the DC-DC, clear this bit to disable the DC-DC converter and prevent a leakage current.

4.1.1 DC-DC timing characteristics

Figure 7 shows the DC-DC startup time:

- MCXW71 has been connected in DC-DC Buck mode and no external loads added.
- The DC-DC input and output voltages are DCDC_IN = 3.3 V and DCDC_OUT = 1.8 V.
- DC-DC is configured in Normal Drive Strength mode.
- In this capture, the yellow curve represents the DCDC_OUT and the blue curve represents the DCDC_IN.

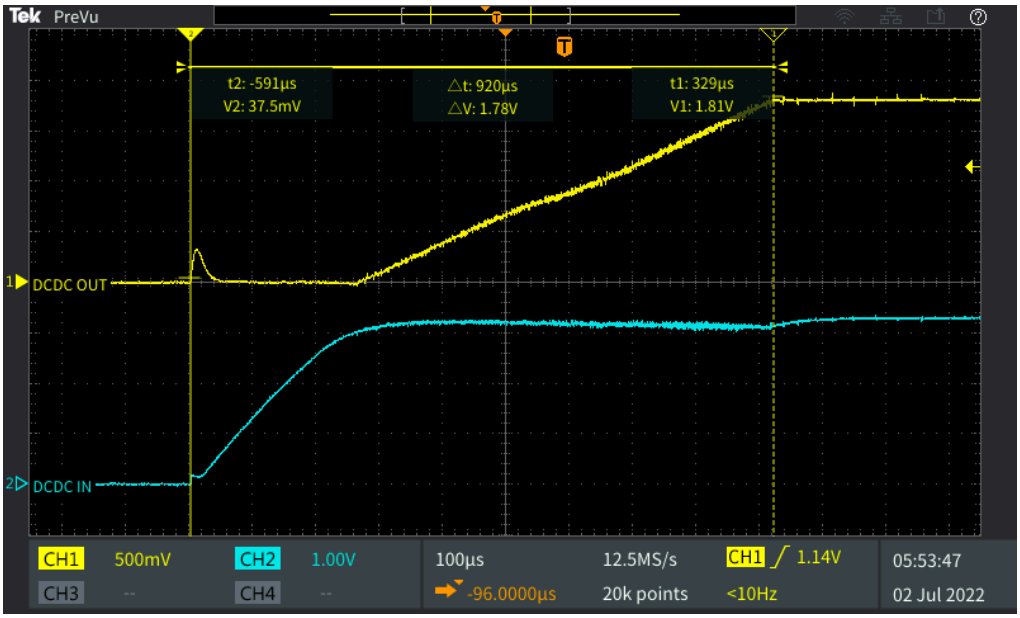


Figure 7. DC-DC startup time

Figure 8 shows the DC-DC shutdown time, considering the drop from 100 % to 10 % of the configured voltage:

- MCXW71 connected in DC-DC Buck mode and no external loads added.
- The DC-DC input and output voltages are DCDC_IN = 3.3 V and DCDC_OUT = 1.8 V.
- DC-DC is configured in Normal Drive Strength mode.
- In this capture, the yellow curve represents the DCDC_OUT and the blue curve represents the DCDC_IN.

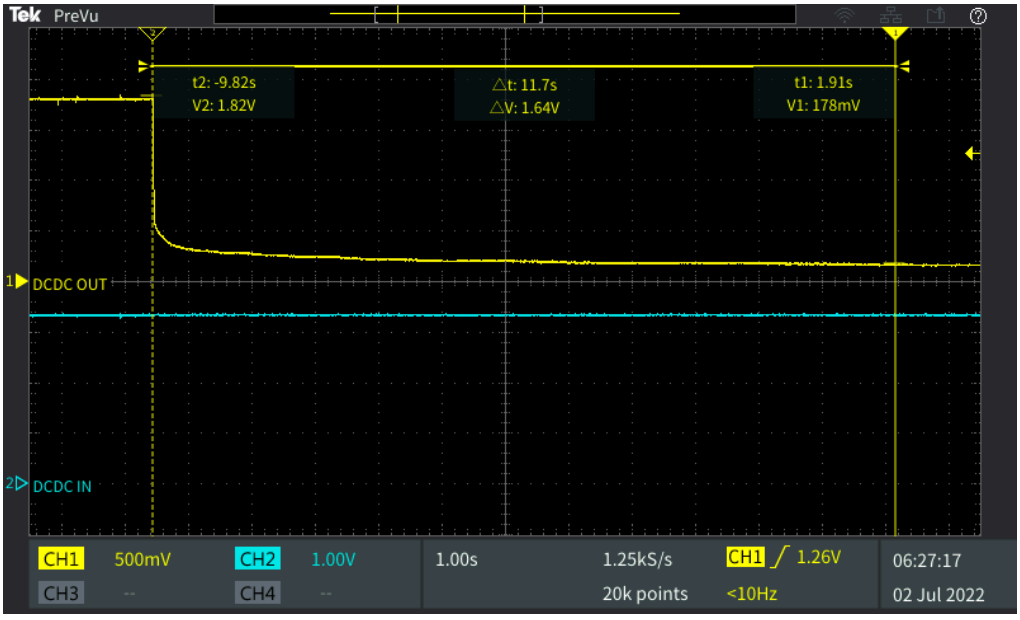


Figure 8. DC-DC shutdown time

4.2 DC-DC drive strength modes

The DC-DC can operate in two different drive modes:

- Active mode
- Pulse Refresh mode

For more details about the software enablement, see Section 7.

Figure 9 depicts the DC-DC Drive Strength modes.

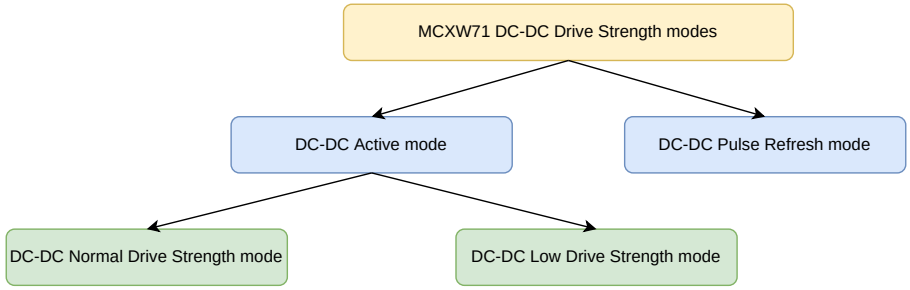


Figure 9. DC-DC drive strength modes

4.2.1 DC-DC Active mode

When operating in Active mode, the DC-DC periodically issues a pulsed burst to maintain the output at the configured regulation voltage based on an internal analog-comparator monitoring system. This control mechanism ensures the regulation voltage always as long as the DC-DC load current is limited within the maximum specification. When the DC-DC is running in Active mode, it can work in two different regulator drive strength modes: Normal Drive Strength and Low Drive Strength. Having different drive strength modes allow control over the quiescent current managed by the DC-DC output driver. As a result, the DC-DC changes its maximum output current, the transient response, and efficiency as follows:

- **Normal Drive Strength mode:** The DC-DC provides the maximum output current capacity with the maximum DC-DC efficiency. This configuration provides the fastest transient response. However, the higher quiescent current at the operating point leads to a bigger DC-DC power consumption.
- **Low Drive Strength mode:** The DC-DC provides a limited output current capacity and less DC-DC efficiency. The transient response is slower than in Normal Drive Strength mode. However, this configuration decreases the overall power consumption of the DC-DC block due to a low quiescent current.

The selection of the drive strength mode must account for the maximum current required by the application and the transient response requirements. If the DC-DC Drive mode operation is not critical in your application, or if the application behavior is hard to predict, keep these settings in the default configuration. It means using DC-DC Active mode with Normal Drive Strength mode. However, if your application requires optimizing the power consumption entering and exiting Low-power modes, consider setting the DC-DC Low Drive Strength mode. Another option is to combine the DC-DC Normal Drive Strength in MCU Active mode and DC-DC Low Drive Strength for Low-power modes.

4.2.2 DC-DC Pulse Refresh mode

When the DC-DC is enabled and running in Pulse Refresh mode, the DC-DC periodically issues a pulsed burst based on a programmed timer embedded on the system power control (SPC). In this mode, the analog-comparator monitoring system is disabled. Therefore, the DC-DC does not perform pulsed bursts to reload the output when the DC-DC output drops below the regulation voltage. Also, the SPC programmable timer period controls the DC-DC refresh burst entirely. In this mode, the DC-DC is turned off after completing the previous DC-DC burst. It turns on at the next timer timeout to reload the output.

The SPC -> DCDC_BURST_CFG [PULSE_REFRESH_COUNT] bit field controls how often the DC-DC is pulsed on and off based on the reference clock provided by the CCM32K module (f_{CCM32K}).

The SPC -> DCDC_BURST_CFG[PULSE_REFRESH_COUNT] bit field is a 16-bit counter value. It controls the frequency of the DC-DC refresh when DC-DC is configured in Pulse Refresh mode.

The formula in Equation 1 is used to calculate DC-DC refresh frequency (f_{DCDC_RFSH}) in Pulse Refresh mode:

$$T_{DCDC\_RFSH} = \frac{1}{f_{CCM32K}} \times \left(\text{PULSE\_REFRESH\_COUNT} + 2\right) \quad (1)$$

4.2.2.1 Conditions to operate in DC-DC Pulse Refresh mode

The following conditions must be accomplished to operate the DC-DC in Pulse Refresh mode:

1. Software must configure the DC-DC Pulse Refresh mode before the MCU goes to sleep. However, the DC-DC does not enter Pulse Refresh mode until:
   - All power domains have requested to enter Low-power mode
   - The SPC has entered a low-power state
   - The MCU has successfully gone to sleep

   At wake-up, the DC-DC returns to the DC-DC Active mode.
2. DC-DC Pulse Refresh mode is not intended to supply external loads, but only the MCU itself. In DC-DC Pulse Refresh mode, the DC-DC is enabled periodically to reload the DC-DC output capacitor based on the PULSE_REFRESH_CNT counter value. The rest of the time the DC-DC remains disabled. The application must configure the PULSE_REFRESH_CNT refresh rate to manage the voltage drop on the DC-DC capacitor and avoid a brownout condition. When the DC-DC is in Pulse Refresh mode, an external load can cause the DC-DC output voltage to drop faster than the next DC-DC reload cycle. This condition brings the device to a brownout condition. Therefore, this mode is recommended when the MCU power domains are the only load connected on the DC-DC. For cases, when the DC-DC supplies external loads while the MCU enters Deep Power Down mode and a low DC-DC power consumption is desired, use the DC-DC in Low Drive Strength instead of DC-DC Pulse Refresh mode.
3. DC-DC Pulse Refresh mode must enable the CCM32K clock output while the MCU enters low power to generate the periodic PWM bursts based on the PULSE_REFRESH_COUNT. The CCM32K peripheral can generate the clock output either from the external 32 kHz Xtal or from the internal FRO32K. If the application requires to disable the 32 kHz Xtal pins as part of the procedures to go to sleep and the DC-DC is configured for Pulse Refresh mode, ensure that the FRO32K is enabled and selected as the main source to generate the CCM32K clock before entering low power.

4.3 DC-DC frequency stabilization

The DC-DC frequency stabilization feature improves the switching frequency variations caused due to voltage transients in the DC-DC input, or dynamic loads at the DC-DC output. This feature can adjust the center switching frequency of the burst pulses. Therefore, you can consider it for applications sensitive to a particular frequency domain that can suffer interference from the DC-DC switching harmonics. Enabling the frequency stabilization feature causes a reduction of the DC-DC input reload current. However, there is a significant reduction of the maximum output current that the DC-DC can drive at its output.

If DC-DC does not experience significant transients or drastic changes in the load, disable this feature (by default the DC-DC frequency stabilization feature is disabled). On the other hand, if the application requires strict control over the DC-DC spectral content to avoid interference with other systems or if it must operate using a coincell battery where DC-DC current peaks impact directly the battery lifetime, this feature can be worth exploring. However, remember that enabling it reduces the DC-DC output current capability.

DC-DC frequency stabilization is enabled/disabled writing the SPC -> DCDC_CFG[FREQ_CNTRL_ON] bit field. When the frequency stabilization feature is enabled, the DC-DC switching frequency can be adjusted through the SPC -> DCDC_CFG[FREQ_CNTRL] 6-bit trimming value. DC-DC frequency stabilization is only available for DC-DC Active mode.

4.4 DC-DC burst synchronization

You can control and monitor the DC-DC burst by the application. Synchronizing with the quiet period between consecutive DC-DC bursts can be valuable for noise-sensitive applications, such as during a high-resolution ADC measurement. For this purpose, the DC-DC and the SPC provide the DCDC_BURST_TRIG_PULSE signal to synchronize the DC-DC burst activity with other peripherals in the device. This signal is asserted when a DC-DC burst completes and the DC-DC has entered the quiet period. This signal can trigger the ADC. To activate this signal, it is necessary to set SPC -> DCDC_BURST_CFG[EXT_BURST_EN] = 1. It is available as a trigger source in the TRGMUX peripheral and can be configured to trigger some on-chip peripherals. For more detail, refer to the *MCXW71 Reference Manual*.

The application can request to initiate the DC-DC burst. For that purpose, the SPC -> DCDC_BURST_CFG[BURST_ACK] must be equal to '0' in the first instance. Then the software can request a burst by setting the SPC -> DCDC_BURST_CFG[BURST_REQ]= 1. DC-DC and SPC hardware sets the SPC -> DCDC_BURST_CFG[BURST_ACK] = 1 when the burst has completed and the DC-DC has entered in the quiet period. Finally, the software must clear the burst acknowledge flag by writing a '1' logic to the SPC -> DCDC_BURST_CFG[BURST_ACK] bit.

For a high-resolution ADC conversion, you can configure the DCDC_BURST_TRIG_PULSE signal to trigger the ADC conversion and then initiate a DC-DC burst by software. At the completion of the current DC-DC burst, the ADC conversion is triggered in the DC-DC quiet period for an optimum ADC conversion result.

4.5 DC-DC operation in power modes

The SPC peripheral has control over the DC-DC work modes. The SPC has two configuration registers:

- SPC active power mode configuration register (ACTIVE_CFG)
- SPC low-power mode configuration register (LP_CFG)

These registers are intended to have independent settings for the DC-DC when MCXW71 enters a Low-power mode.

The ACTIVE_CFG and LP_CFG registers can configure the DC-DC voltage and drive strength modes. Therefore, it is possible to configure the DC-DC in a different way automatically when the device moves to low power and exits it. Having independent configurations for Active mode and Low-power mode, allows the implementation of power-saving mechanisms by software. For example, it is possible to reduce the DC-DC voltage and set the DC-DC Low Drive Strength mode when the device goes to sleep, configuring the proper settings on the LP_CFG register. Then restore the DC-DC to a higher voltage and Normal Drive mode at wake-up with the programmed settings in the ACTIVE_CFG. Even if the previous example is the expected operation for most of the applications, it is possible to set the DC-DC to a higher voltage in Low-power mode than in Active mode if the application requires it.

Table 5 describes the DC-DC operation modes allowed in each MCXW71 power mode.

Table 5. DC-DC operation modes

Module	Active	Sleep	Deep Sleep	Power Down	Deep Power Down
DC-DC buck converter	Normal or Low Drive Strength mode controlled by SPC ACTIVE_CFG register	Normal or Low Drive Strength mode controlled by SPC LP_CFG register	• Normal, Low Drive Strength, Refresh mode controlled by SPC LP_CFG • Off (Optional)	• Normal, Low Drive Strength, or Pulsed Refresh mode controlled by SPC LP_CFG • Off (Optional)	Off

The DC-DC Normal Drive Strength mode is available in all power modes except Deep Power Down mode. DC-DC Low Drive Strength mode is available in all power modes except Deep Power Down mode. DC-DC Pulsed Refresh mode is only available in the Deep Sleep and Power Down modes. If the application is required to disable the DC-DC in the Deep Sleep and Power Down modes, it is possible to do so if the DC-DC is not supplying the power domains necessary to wake up. The DC-DC off state is forced automatically when the device enters in Deep Power Down. DCDC_OUT = 2.5 V option is available only in DC-DC Normal Drive Strength mode. The rest of the voltage options are available in all drive strength modes. To configure the DC-DC in Low Drive Strength mode when the MCU is in Active mode, the application must set the same DC-DC output voltage on the ACTIVE_CFG and LP_CFG registers. It is mandatory to disable the HVD/LVD in the LP_CFG register before configuring the DC-DC in Pulsed Refresh mode.

Any changes to the DC-DC drive strength or voltage level cause the SPC -> SC[BUSY] flag to assert to '1' logic level until SPC has completed changing its state to the new value. Therefore, software must check this status bit and wait until this bit clears to '0', to ensure that the SPC has completed the drive strength or voltage transition.

4.6 DC-DC main configuration registers

This section summarizes the main SPC registers involved in the configuration of the DC-DC buck converter in the MCWX71 MCU. Table 6 describes the SPC registers that configure the DC-DC behavior. For the full peripheral description, refer to the *MCXW71 Reference Manual*.

SPC0 base address 4001_6000h

Table 6. DC-DC main configuration registers

Offset	Register	Width (bits)	Access	Reset value
14h	SPC regulator control register (CNTRL) This register controls the enablement of the SPC regulators	32	WONCE	0000_0007h
100h	Active power mode configuration register (ACTIVE_CFG) This register controls the settings of the SPC regulators in Active mode	32	RW	3F10_0E15h
104h	Low-power mode configuration register (LP_CFG) This register controls the settings of the SPC regulators in Low-power modes	32	RW	0002_1D04h
500h	DC-DC configuration register (DCDC_CFG) This register configures the frequency stabilization bit fields	32	RW	0000_0000h
504h	DC-DC BURST configuration register (DCDC_BURST_CFG) This register configures the DC-DC burst control bit fields	32	RW	0140_0000h

4.6.1 SPC regulator control register (CNTRL)

The following bit field controls the enablement of the SPC regulators:

- **CNTRL[DCDC_EN]:** This bit field controls if the DC-DC is turned on (DCDC_EN = 1) or turned off (DCDC_EN = 0). By default, the DC-DC is turned on. Ensure that the power domains supplied by this domain can be disabled before disabling the DC-DC. If the DC-DC is bypassed, disable the DC-DC writing (DCDC_EN = 0).

4.6.2 Active power mode configuration register (ACTIVE_CFG)

The following bit fields control the settings of the SPC regulators in Active mode:

- **ACTIVE_CFG[DCDC_VDD_LVL]:** This bit field controls the DC-DC output voltage when the SPC is in Active mode. DCDC_OUT = 2.5 V is only available for DC-DC Normal Drive Strength. To set DCDC_OUT = 2.5 V, it is required to set DCDC_CFG[VOUT2P5_SEL] = 1. For the rest of the voltage options, the VOUT2P5_SEL bit must be 0.

Table 7. DC-DC VDD regulator level

DCDC_VDD_LVL	VOUT2P5_SEL	DC-DC voltage
00b	0b	1.25 V
01b	0b	1.35 V
10b	1b	2.5 V
11b	0b	1.8 V

- **ACTIVE_CFG[DCDC_VDD_DS]:** This bit field controls the DC-DC drive strength mode when the SPC is in Active mode. The valid drive strength modes when the SPC is in Active mode are DC-DC Normal and DC-DC Low Drive Strength. DC-DC Pulsed Refresh mode is not available for SPC Active mode.

Table 8. DC-DC VDD regulator drive strength

DCDC_VDD_DS	DC-DC Drive mode
00b	Reserved
01b	Set to Low Drive Strength
10b	Set to Normal Drive Strength
11b	Reserved

4.6.3 Low-power mode configuration register (LP_CFG)

The following bit fields control the settings of the SPC regulators in low-power modes:

- **LP_CFG[DCDC_VDD_LVL]:** This bit field controls the DC-DC output voltage when the SPC is in Low-power mode. DCDC_OUT = 2.5 V is only available for DC-DC Normal Drive Strength. To set DCDC_OUT = 2.5 V, it is required to set DCDC_CFG[VOUT2P5_SEL] = 1. For the rest of the voltage options, the VOUT2P5_SEL bit must be 0.

Table 9. DC-DC VDD regulator level

DCDC_VDD_LVL	VOUT2P5_SEL	DC-DC voltage
00b	0b	1.25 V
01b	0b	1.35 V
10b	1b	2.5 V
11b	0b	1.8 V

- **LP_CFG[DCDC_VDD_DS]:** This bit field controls the DC-DC drive strength mode when the SPC is in Low-power mode.

Table 10. DC-DC VDD regulator drive strength

DCDC_VDD_DS	DC-DC Drive mode
00b	Set to Pulse Refresh mode
01b	Set to Low Drive Strength
10b	Set to Normal Drive Strength

Table 10. DC-DC VDD regulator drive strength...*continued*

DCDC_VDD_DS	DC-DC Drive mode
11b	Reserved

4.6.4 DC-DC configuration register (DCDC_CFG)

The following bit fields configure the frequency stabilization function in the DC-DC:

- **DCDC_CFG[VOUT2P5_SEL]:** This bit field must remain enabled (VOUT2P5_SEL = 1) if the desired DC-DC output is 2.5 V (DCDC_VDD_LVL = 10b). Otherwise, this bit must remain disabled (VOUT2P5_SEL = 0). If VOUT2P5_SEL = 1 and DCDC_VDD_LVL is different than 10b (DC-DC output voltage selection is not 2.5 V), the DC-DC output voltage is not predictable. Therefore, you must enable this bit only if the output voltage is 2.5 V. If the output voltage must move from 2.5 V to another voltage level, this bit must be cleared (VOUT2P5_SEL = 0). The 2.5 V option is only available in DC-DC Normal Drive Strength mode. If DC-DC is operating at 2.5 V in DC-DC Normal Drive Strength mode and the DC-DC drive strength mode must be changed, ensure to update the DC-DC output value to any other allowed value and clear this bit.
- **DCDC_CFG[FREQ_CNTRL_ON]:** This bit field enables/disables the frequency stabilization function in the DC-DC. Frequency stabilization is enabled with FREQ_CNTRL_ON = 1 and disabled with FREQ_CNTRL_ON = 0. When it is enabled, the DC-DC burst frequency can be adjusted with the FREQ_CNTRL bit field from the central frequency.
- **DCDC_CFG[FREQ_CNTRL]:** This bit field represents a 6-bit trimming value for the DC-DC burst frequency when the frequency stabilization feature is enabled, FREQ_CNTRL_ON = 1. When FREQ_CNTRL_ON = 0, FREQ_CNTRL trimming value is ignored.

4.6.5 DC-DC burst configuration register (DCDC_BURST_CFG)

The following bit fields configure the DC-DC burst control:

- **DCDC_BURST_CFG[PULSE_REFRESH_CNT]:** This bit field is the 16-bit multiplier value that determines the DC-DC burst occurrence when the DC-DC is in Pulse Refresh mode based on the CCM32K output frequency. See Section 4.2.2.
- **DCDC_BURST_CFG[BURST_ACK]:** This bit field is an indicator flag that sets to '1' when the previous DC-DC burst requested by the software has completed successfully. This bit must be cleared each time at the completion of a burst requested by the software writing BURST_ACK = 1.
- **DCDC_BURST_CFG[EXT_BURST_EN]:** This bit enables/disables the internal DCDC_BURST_TRIG_PULSE signal that is used to trigger some peripherals with the TRGMUX when the DC-DC enters in the quiet period. EXT_BURST_EN = 1 enables the trigger signal, EXT_BURST_EN = 0 disables the trigger signal. This bit must be written only when BURST_ACK = 0, and before writing BURST_REQ = 1 to request a DC-DC burst.
- **DCDC_BURST_CFG[BURST_REQ]:** Write BURST_REQ = 1 to initiate a burst request. Do not initiate a new burst request until the previous one has been completed and acknowledged (clearing the BURST_ACK flag).

4.7 DC-DC electrical characteristics

This chapter includes DC-DC electrical characteristics.

4.7.1 DC-DC converter specifications

Table 11 summarizes the DC-DC converter specifications.

Table 11. DC-DC converter specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_DCDC_IN	DC-DC input voltage	1.71	-	3.6	V	1, 2
V_DCDC_OUT	DC-DC output voltage	1.25	-	2.5	V	1, 2
V_DCDC_RIPPLE	Ripple voltage at DC-DC output: • Normal Drive Strength mode • Low Drive Strength mode	- -	1 25	- -	% mV	3 -
I_DCDC_LOAD	Load current at DC-DC output: • Normal Drive Strength mode • Low Drive Strength mode • Frequency Stabilization on [FREQ_CNTRL_ON = 1]	- - -	- - -	105 15 45	mA	1, 4
LX	DC-DC output inductor value	0.47	1	2.2	µH	5
ESR	DC-DC inductor equivalent series resistance	-	110	-	mΩ	6
COUT	DC-DC output capacitance	6	22	30	µF	7
F_Burst	DC-DC reload burst frequency	3	5	8	MHz	8
F_Burst_Accuracy	DC-DC reload burst frequency accuracy	-	10	-	%	8

Note:

1. *The DC-DC converter generates 1.8 V at DCDC_LX by default. The DC-DC can be used to power VDD_RF, VDD_LDO_CORE, and external components as long as the maximum ILOAD is not exceeded.*
2. *The VDD_DCDC input supply to DC-DC must be at least 500 mV higher than the desired output at DCDC_LX.*
3. *The DC ripple is shown as a percentage in relation with the programmed DC-DC output voltage.*
4. *The maximum load current during boot-up must not exceed 60 mA.*
5. *The recommended inductor value is 1 µH to 1.5 µH. If the inductor is < 1 µH, the DC-DC efficiency is not guaranteed.*
6. *The maximum recommended ESR is 250 mΩ (not a hard limit).*
7. *The variation in capacitance of the capacitor at DCDC_LX due to aging, temperature, and voltage degradation must not exceed the min/max values.*
8. *FREQ_CNTRL_ON = 1.*

4.7.2 DC-DC output waveforms

The DC-DC converter can operate either in Active in Normal or Low Drive Strength modes, or Pulsed mode. Figure 10 shows different captures showing the DC-DC output and DCDC_LX inductor voltage. In DC-DC Active mode, DC-DC adjusts the output voltage constantly through voltage bursts to maintain the DC-DC output at the desired level independent from the DC-DC load. In DC-DC Pulsed mode, an internal counter refreshes the DC-DC based on the CCM32K frequency. In DC-DC Pulsed mode, the DC-DC output voltage is not guaranteed with high load currents as explained in Section 4.2.

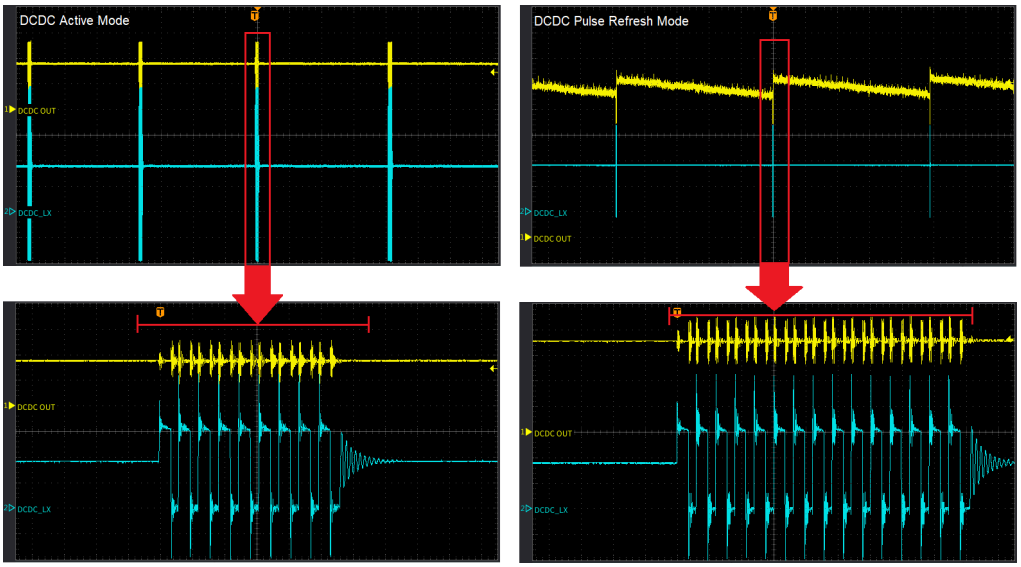


Figure 10. DC-DC Active and Pulse Refresh modes

4.7.3 DC-DC efficiency charts

The power delivered by the DC-DC converter is a function of many variables, such as the DC-DC load and voltage. Figure 11 to Figure 17 show some examples of the DC-DC efficiency real numbers obtained with different voltages and currents. The DC-DC output current has been adjusted at a fixed value and the input power has been measured considering that the DC-DC input pin is shared with the LDO system and VDD_IO_D power domains.

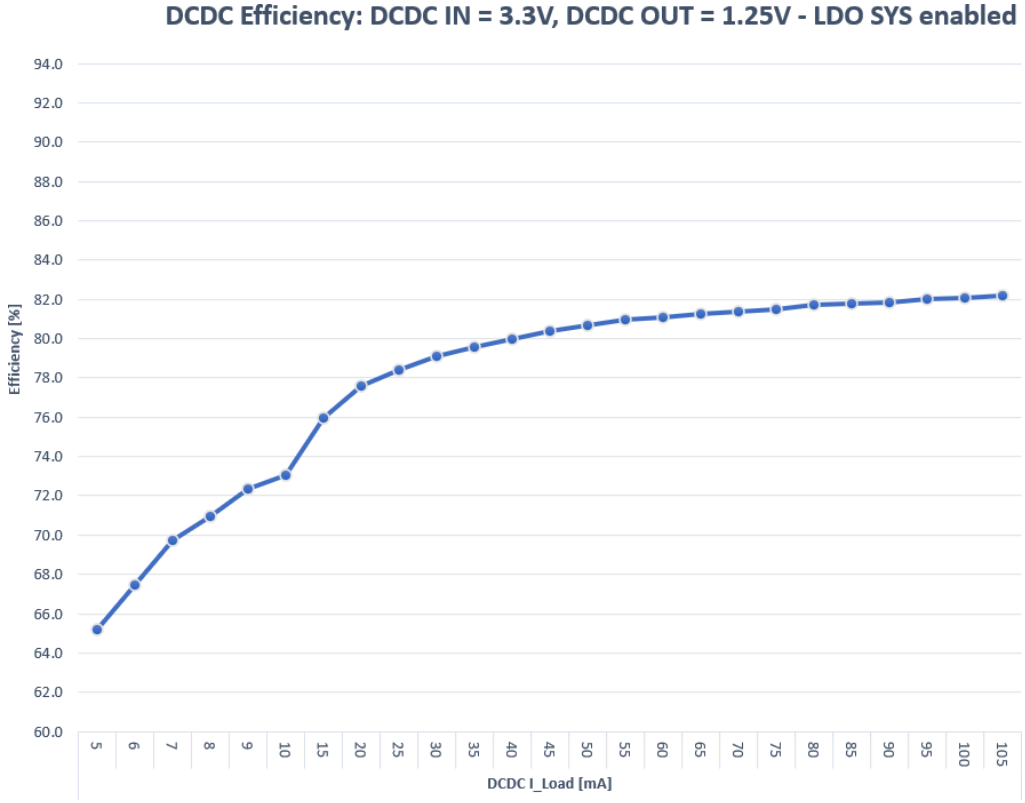


Figure 11. DC-DC Efficiency Normal Drive Strength mode, DCDC_OUT = 1.25 V

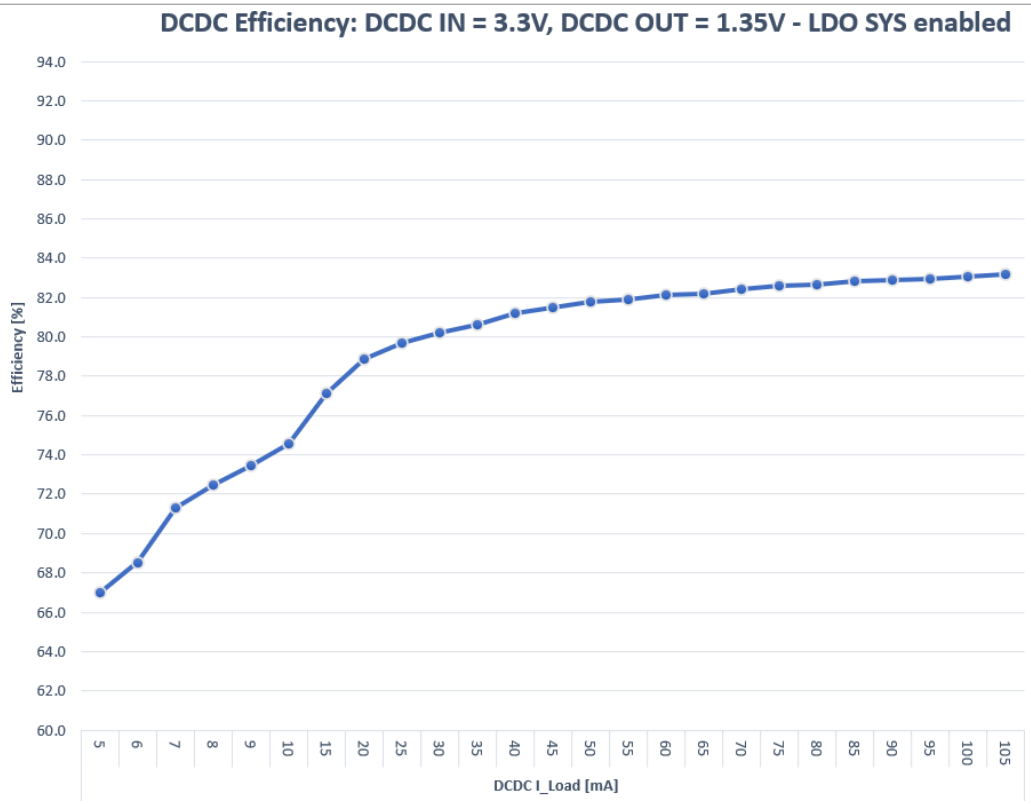


Figure 12. DC-DC Efficiency Normal Drive Strength mode, DCDC_OUT = 1.35 V

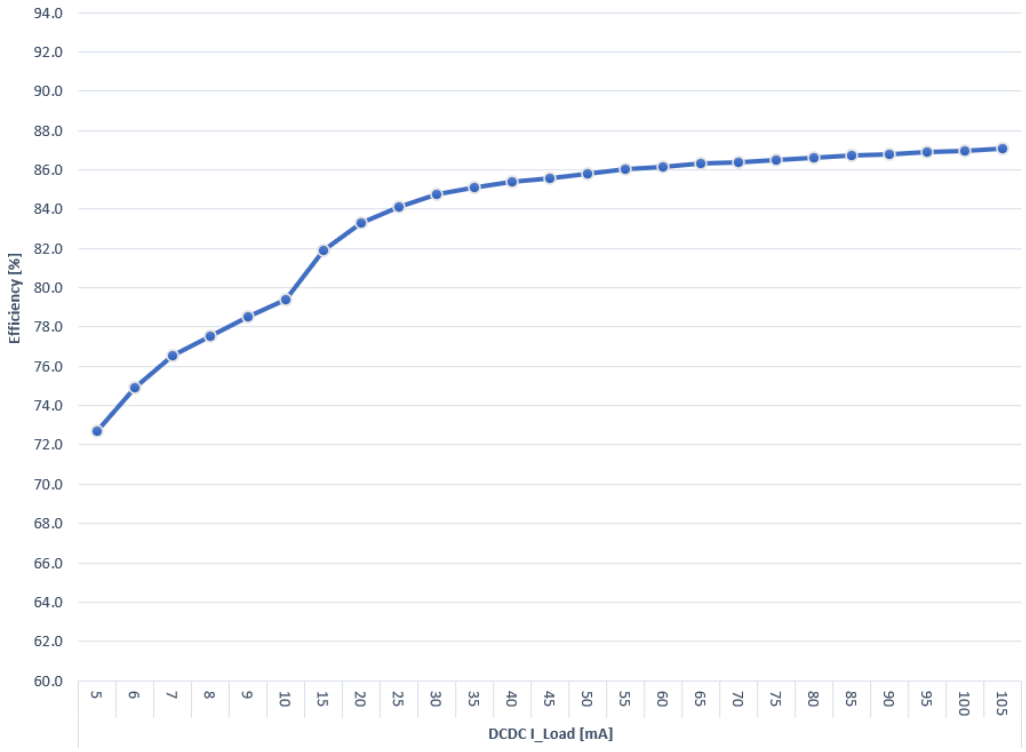


Figure 13. DC-DC Efficiency Normal Drive Strength mode, DCDC_OUT = 1.8 V

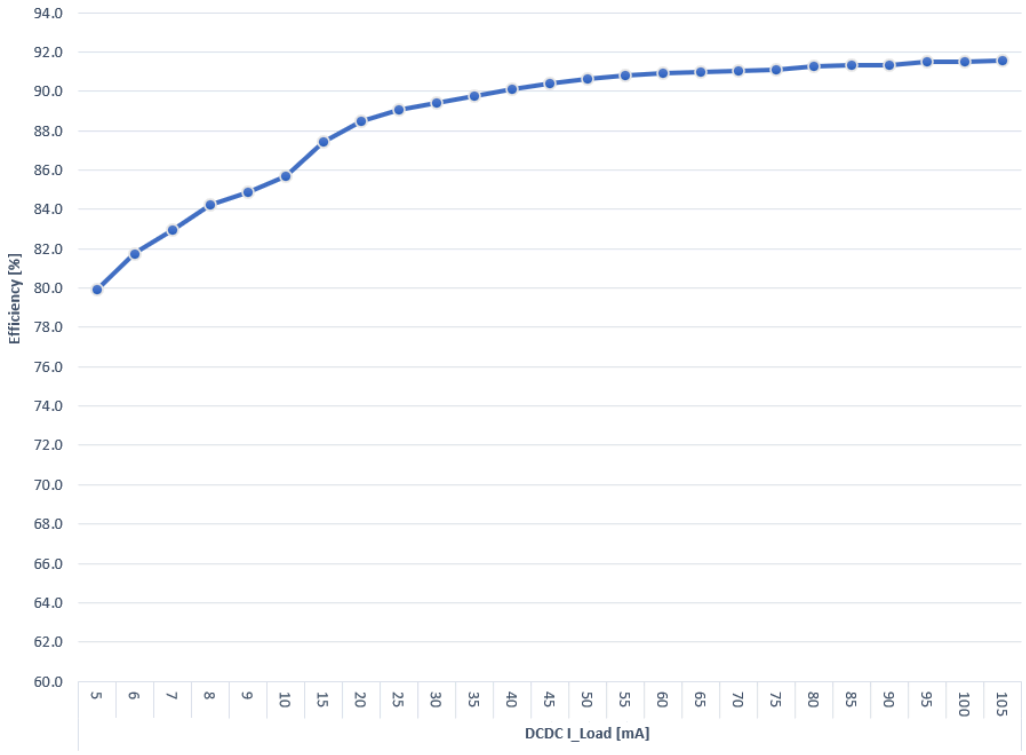


Figure 14. DC-DC Efficiency Normal Drive Strength mode, DCDC_OUT = 2.5 V

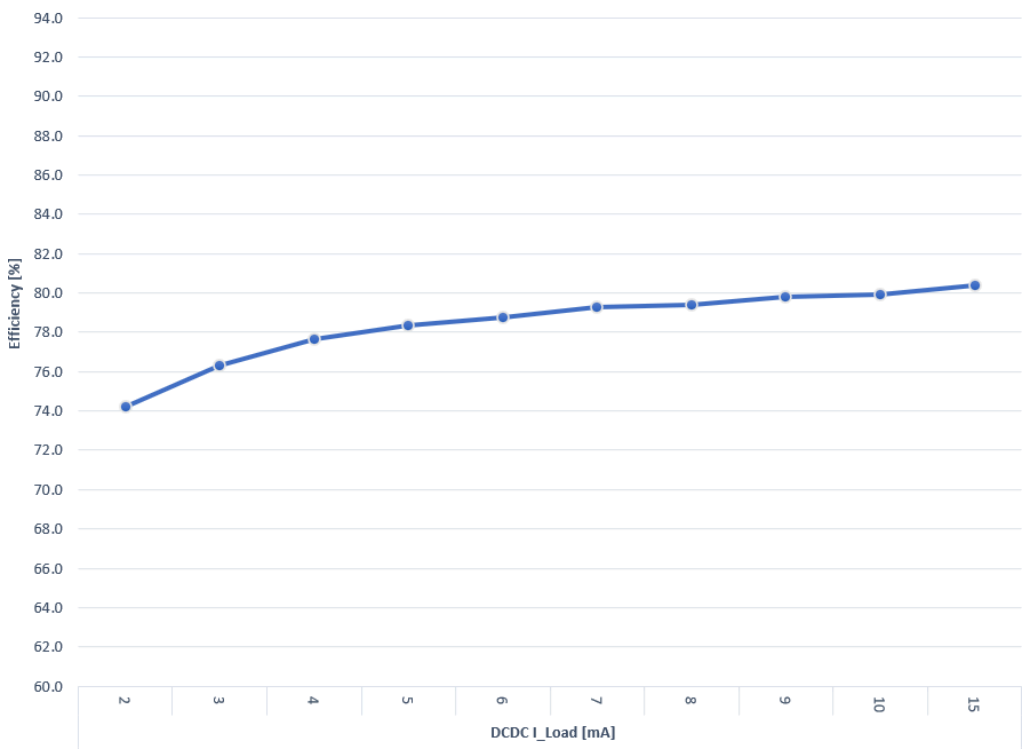


Figure 15. DC-DC Efficiency Low Drive Strength mode, DCDC_OUT = 1.25 V

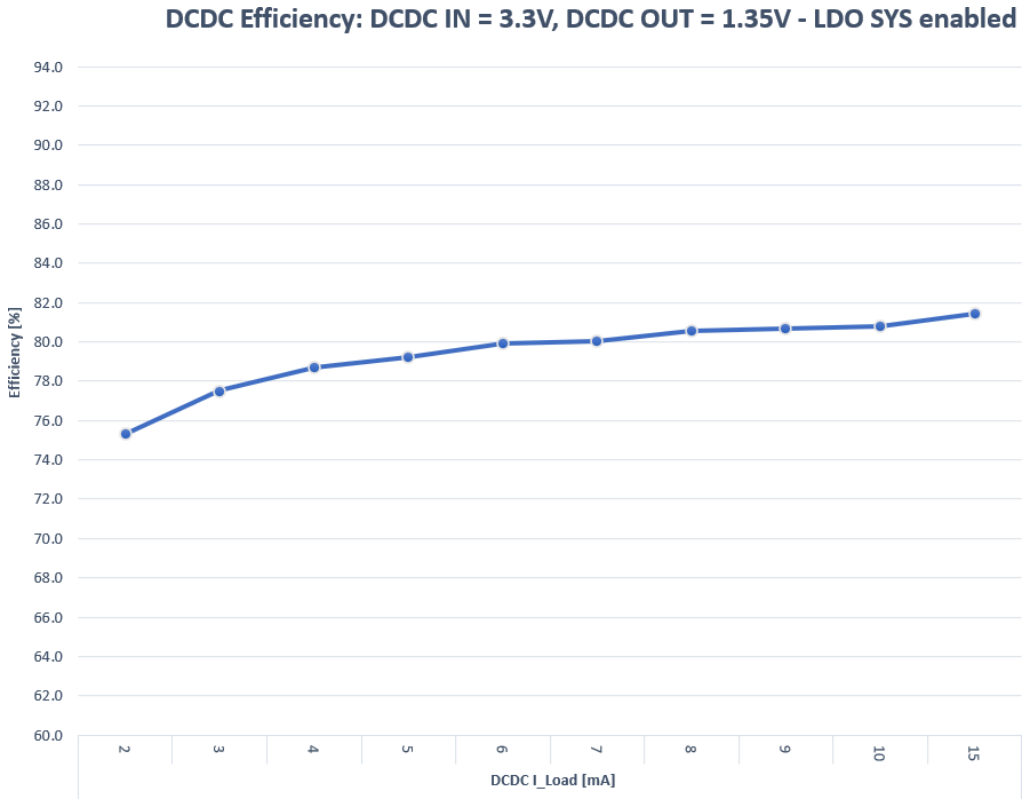


Figure 16. DC-DC Efficiency Low Drive Strength mode, DCDC_OUT = 1.35 V

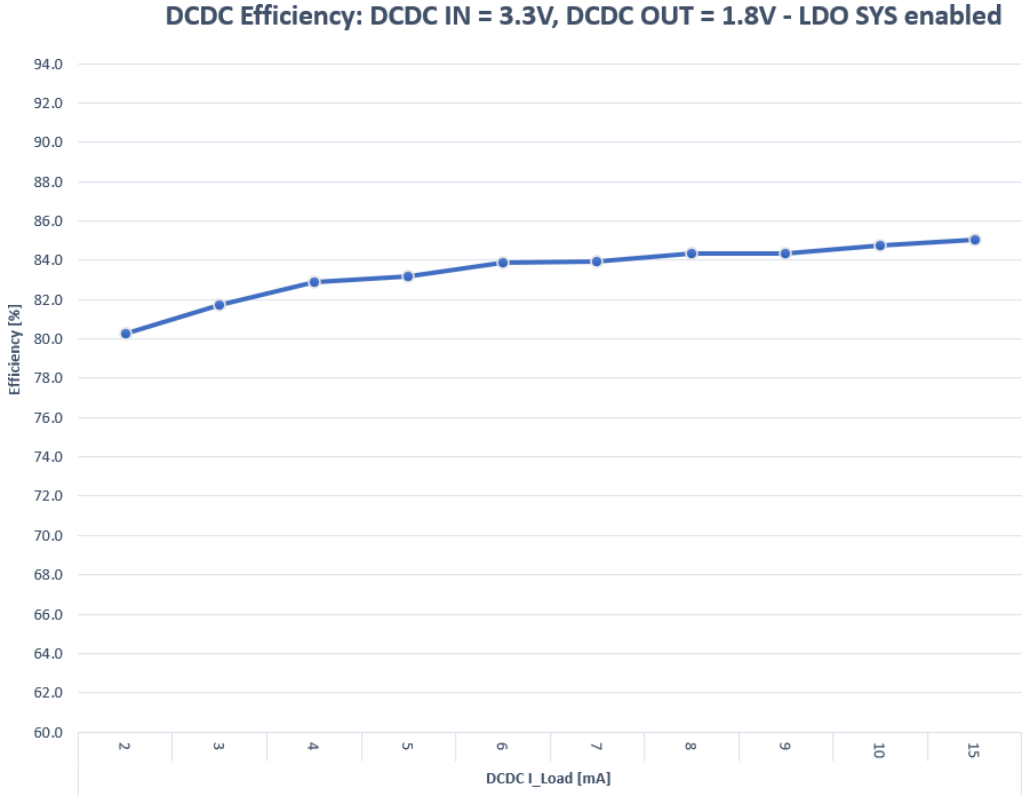


Figure 17. DC-DC Efficiency Low Drive Strength mode, DCDC_OUT = 1.8 V

4.7.4 Refresh period in DC-DC Pulse Refresh mode

The formula in Equation 1 in Section 4.2.2 shows the DC-DC refresh rate in Pulsed mode. Figure 18 and Figure 19 are two examples that show the DC-DC refresh period in Pulsed mode to demonstrate the impact of the DCDC_BURST_CFG[PULSE_REFRESH_CNT] value.

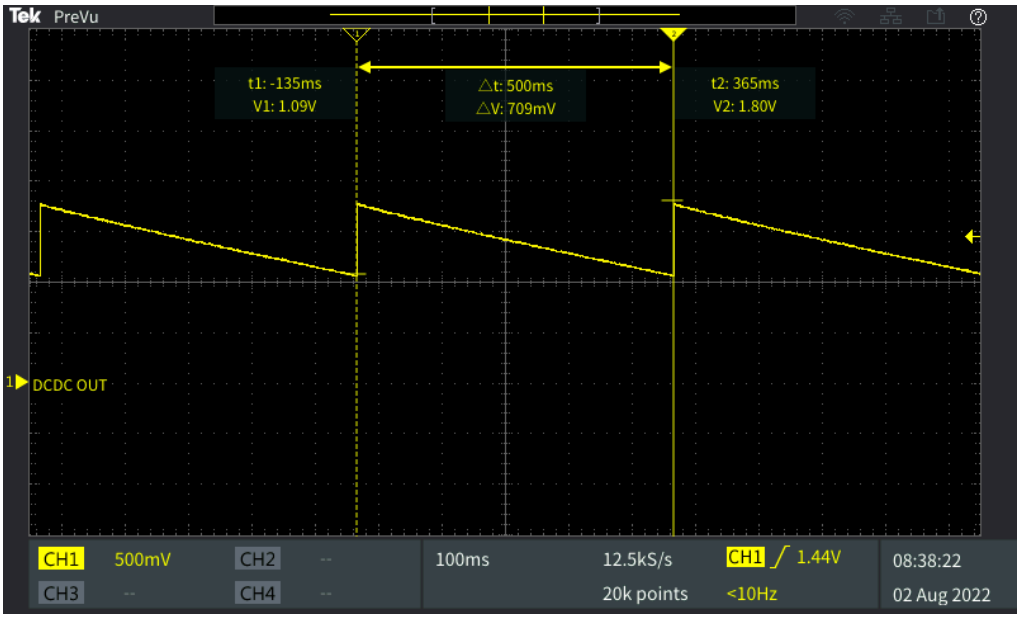


Figure 18. DC-DC in Pulse Refresh mode, PULSE_REFRESH_CNT = 16382, Tdcdc = 500 ms

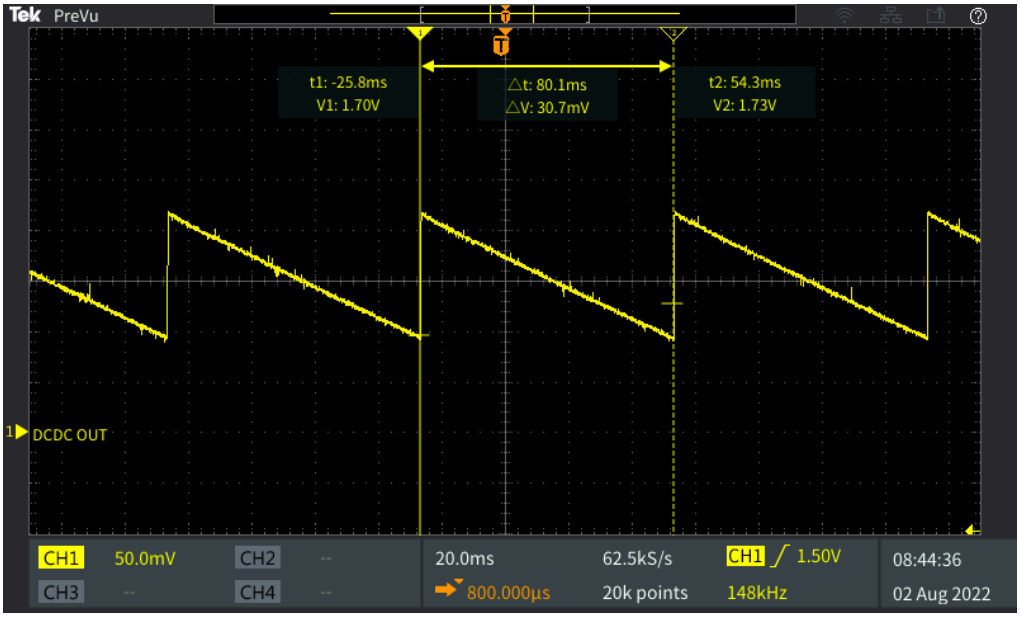


Figure 19. DC-DC in Pulse Refresh mode, PULSE_REFRESH_CNT = 2619, Tdcdc = 80 ms

Table 12 describes the parameters programmed on the device used to capture the above examples.

Table 12. Refresh period measured

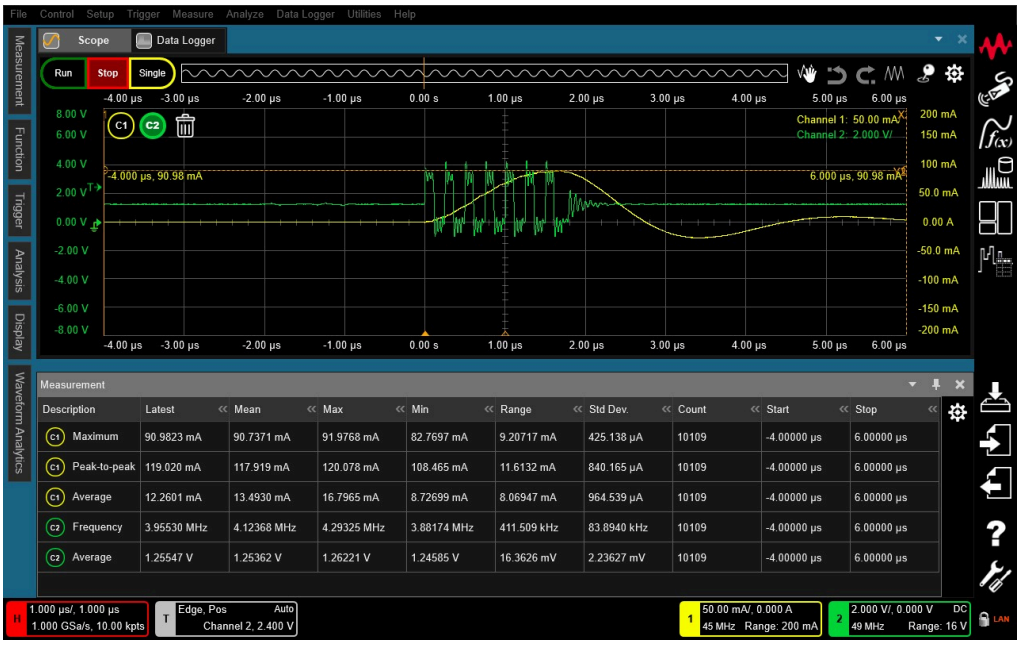
Example	f_{CCM32K}	PULSE_REFRESH_COUNT	T_{DCDC_RFSH} calculated	T_{DCDC_RFSH} measured on the device
Figure 18	32.768 kHz	16382	500 ms	500 ms
Figure 19	32.768 kHz	2619	79.98 ms	80.1 ms

4.7.5 DC-DC frequency stabilization, DC-DC peak current, and spectral content

Enabling DC-DC frequency stabilization via DCDC_CFG[FREQ_CNTRL_ON] bit modifies the DC-DC burst frequency and the DC-DC peak current as explained in Section 4.3. Therefore, DC-DC harmonic content changes, and DC-DC peak reload current decreases at the expense of the DC-DC maximum load capability.

The following examples show how these parameters are affected depending on the DC-DC settings. In each example, the first picture shows the DC-DC input reload current in yellow (DCDC_IN) and the DC-DC output burst (DCDC_OUT). The second picture shows the DC-DC output spectral content with a vertical scale of 10 dBm/div and a horizontal scale of 10 MHz/div.

- Frequency stabilization feature disabled:
  - DCDC_CFG[FREQ_CNTRL_ON] = 0x0
  - DCDC_IN = 3.3 V
  - DCDC_OUT = 1.25 V
  - No external loads
  - DC-DC burst frequency = 4.12 MHz
  - DCDC_IN max current = 90.73 mA



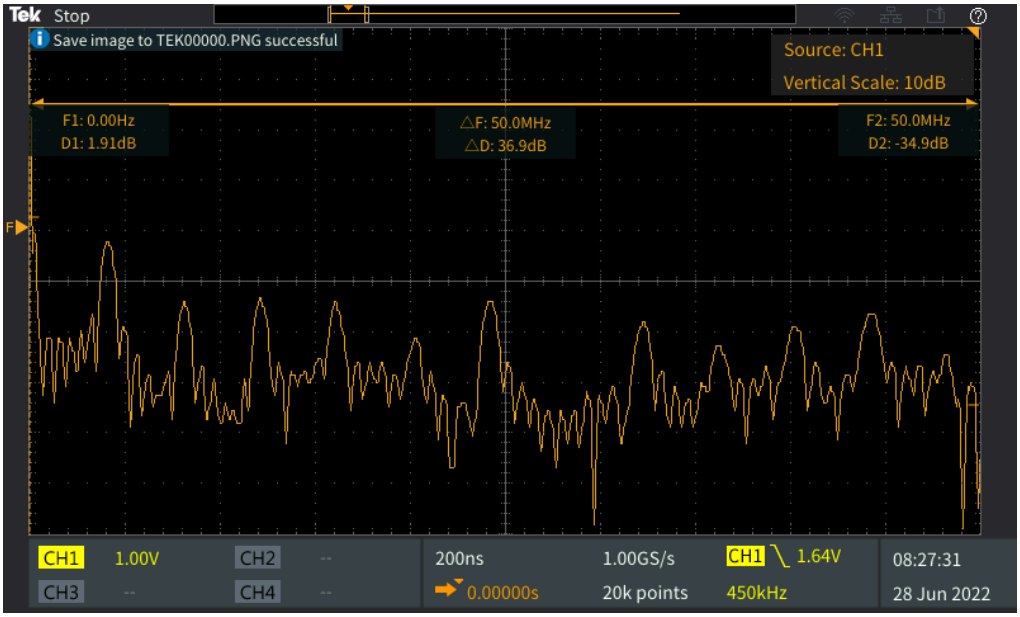


Figure 20. DC-DC frequency stabilization off, DCDC_OUT = 1.25 V

- Frequency stabilization feature enabled:
  - DCDC_CFG[FREQ_CNTRL_ON] = 0x1
  - DCDC_CFG[FREQ_CNTRL] = 0xF
  - DCDC_IN = 3.3 V
  - DCDC_OUT = 1.25 V
  - No external loads
  - DC-DC burst frequency = 6.11 MHz
  - DCDC_IN max current = 52.93 mA

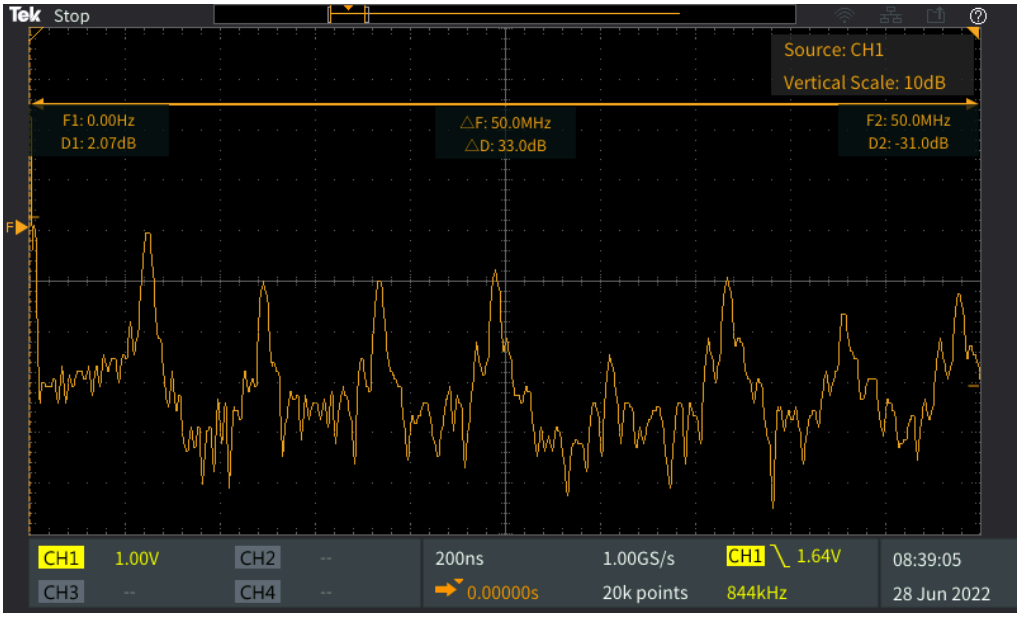


Figure 21. DC-DC frequency stabilization on, DCDC_OUT = 1.25 V

- Frequency stabilization feature disabled:
  - DCDC_CFG[FREQ_CNTRL_ON] = 0x0
  - DCDC_IN = 3.3 V
  - DCDC_OUT = 1.8 V
  - No external loads
  - DC-DC burst frequency = 4.11 MHz
  - DCDC_IN max current = 123.37 mA

Figure 22. DC-DC frequency stabilization off, DCDC_OUT = 1.8 V

- Frequency stabilization feature enabled:
  - DCDC_CFG[FREQ_CNTRL_ON] = 0x1
  - DCDC_CFG[FREQ_CNTRL] = 0x3
  - DCDC_IN = 3.3 V
  - DCDC_OUT = 1.8 V
  - No external loads
  - DC-DC burst frequency = 4.13 MHz
  - DCDC_IN max current = 76.71 mA

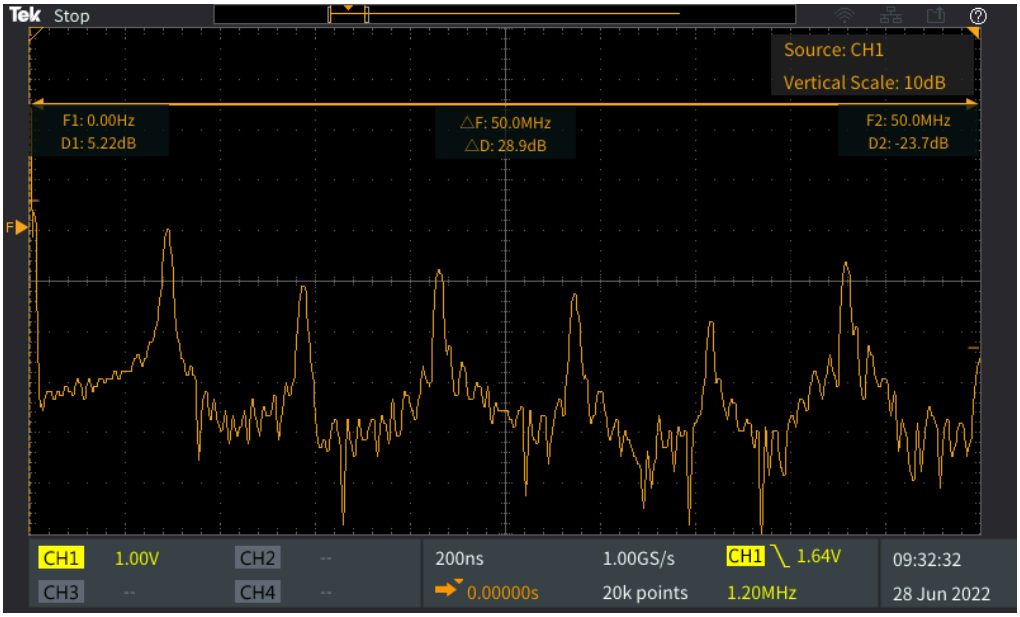


Figure 23. DC-DC frequency stabilization on, DCDC_OUT = 1.8 V

4.7.6 DC-DC power estimation

Different methods can be used to estimate the DC-DC power delivered.

Note: *A portion of the power generated by the DC-DC is internally supplied to monitor the DC-DC output voltage and to ensure the voltage regulation value.*

For more information, refer to section "Power Consumption Operative Behaviors" of the device data sheet.

If it is required to measure the power consumption at runtime, it is possible to measure the DC-DC input voltage and current to calculate the DC-DC input power. This value can be multiplied by the DC-DC efficiency value that better matches with your application. You can find the DC-DC efficiency report for some use cases in Section 4.7.3 when the LDO system is enabled. Consider that there can be variance when using this method because DCDC_IN, the PORTD domain, and the LDO_SYS_IN share the DC-DC input pin available to measure in this device (VDD_IO_D/VDD_DCDC pin).

To estimate the DC-DC output power delivered in runtime, measure the DC-DC burst width (t_{DCDC_Burst}), and DC-DC refresh time ($T_{DCDC\_Refresh}$) directly on the DCDC_LX pin of the device. Figure 24 marks the DC-DC burst time (t_{DCDC_Burst}) between cursors x1 and x2.

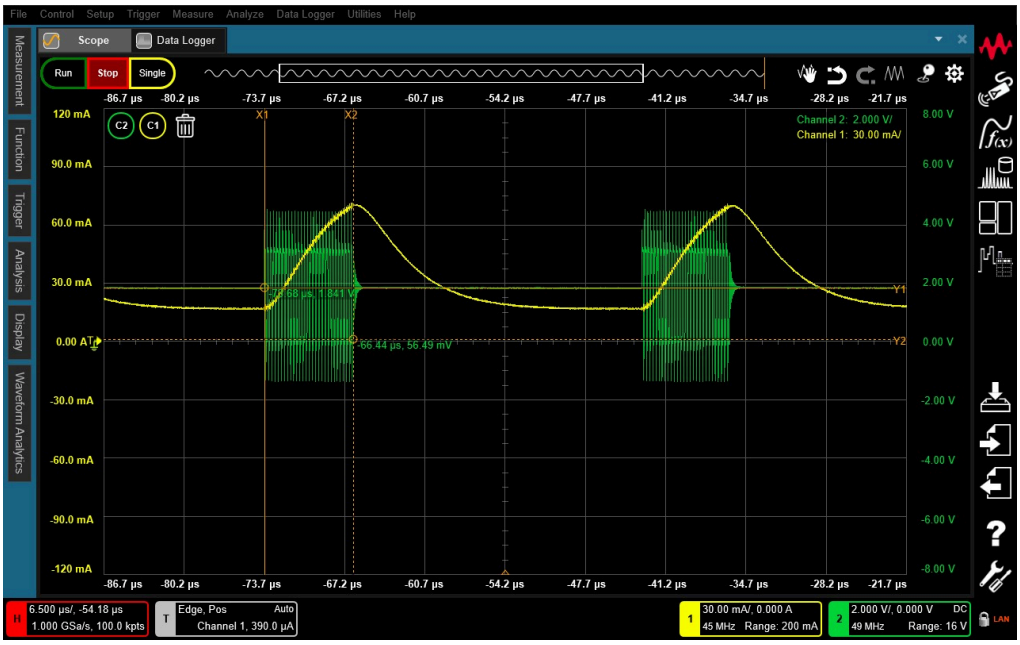


Figure 24. DC-DC burst time

Figure 25 marks the DC-DC refresh time ($T_{DCDC\_Refresh}$) between cursors x1 and x2.

Figure 25. DC-DC refresh time

The formula in Equation 2 is used to estimate the average DC-DC output current based on the previous parameters. This method is valid when the DC-DC operates in Active mode. It is not supported for DC-DC Pulse Refresh mode.

$$DCDC\_Iout_{avg} = k\left(\frac{t_{DCDC\_Burst}}{T_{DCDC\_Refresh}}\right) \quad (2)$$

Where:

- DCDC_Iout$_{avg}$: DC-DC average output current.
- t_{DCDC_Burst}: DC-DC burst time measured directly on the DCDC_LX pin.
- $T_{DCDC\_Refresh}$: DC-DC refresh period measured directly on DCDC_LX pin. It represents the total time between two consecutive DC-DC reload events.
- k: DC-DC current constant. This value depends on the DC-DC drive modes:
  - k = 130 mA for DC-DC Normal Drive Strength mode
  - k = 65 mA for DC-DC Low Drive Strength mode
  - k = 80 mA when the DC-DC frequency stabilization feature is enabled

The following examples show how to estimate the DC-DC output current and its comparison with the real DC-DC output current.

Note: *For a better current estimation, it is necessary to accumulate many current samples over various DC-DC refresh periods.*

For demonstration purposes, the following examples consider one DC-DC reload cycle:

- Figure 26 shows the DC-DC configured in Normal Drive Strength.

Figure 26. DC-DC Normal Drive Strength

- Figure 27 shows DC-DC configured in Low Drive Strength.

Figure 27. DC-DC Low Drive Strength

- Figure 28 shows that the DC-DC frequency stabilization feature is enabled.

Figure 28. DC-DC frequency stabilization on

Table 13 describes the parameters programmed on the device used to capture the above examples.

Table 13. DC-DC current estimation

DC-DC mode	t_{DCDC_Burst}	$T_{DCDC\_Refresh}$	k	Average current estimation	Average current measured on the device
DC-DC Normal Drive Strength	11.42 µs	23.72 µs	130 mA	62.58 mA	65.25 mA

Table 13. DC-DC current estimation*...continued*

DC-DC mode	t_{DCDC_Burst}	$T_{DCDC\_Refresh}$	k	Average current estimation	Average current measured on the device
DC-DC Low Drive Strength	28.64 µs	60.77 µs	65 mA	30.63 mA	32.64 mA
DC-DC frequency stabilization on	14.03 µs	28.73 µs	80 mA	39.06 mA	40.07 mA

5 LDO core and LDO system regulators

This chapter describes the characteristics, features, and operation of the LDO core and LDO system regulators.

5.1 Enabling and disabling LDOs

Both the LDO core and LDO system can be enabled and disabled according to the application requirements. The SPC regulator control register (CNTRL) can enable or disable the LDO CORE and LDO SYS by writing the SPC -> CNTRL[CORELDO_EN] = 0 and SPC -> CNTRL[SYSLDO_EN] = 0, respectively. By default, both LDOs are enabled, however, if your design is bypassing any of these regulators, you must disable such LDO to prevent a leakage current. LDO outputs, VOUT_CORE and VOUT_SYS, are internally tied with VDD_CORE and VDD_SYS power domains respectively. Therefore, before disabling any of these regulators, ensure that such power domain is connected with an external power supply. Some power modes are allowed to turn off the VDD_CORE power domain. Therefore, if no external voltage is connected on the VDD_SYS power domain the LDO system regulator cannot be disabled. To disable the LDO core or LDO system, it is necessary to disable the high and low voltage detectors (SYS_HVDE, CORE_HVDE, SYS_LVDE and CORE_LVDE) in clearing to 0b the corresponding bit fields in the SPC -> ACTIVE_CFG register, wait for the SPC -> SC[BUSY] = 0. Then disable the LDO core regulator by clearing the SPC -> CNTRL[CORELDO_EN] or SPC -> CNTRL[SYSLDO_EN] bit fields as it corresponds.

The LDO core and LDO system have a pulldown resistor that forces the LDO discharge when the software disables the regulator or, in the specific case of the LDO core, when the MCU enters in Deep Power Down mode. This feature is enabled by default. However, when the LDO core and LDO system are disabled to drive the VDD_CORE and VDD_SYS voltages from an external power supply, disable the pulldown resistors to prevent current leakage. Disable the pulldown resistors by writing SPC -> CORELDO_CFG[DPDOWN_PULLDOWN_DISABLE] = 1 for the LDO CORE regulator, and SPC -> SYSLDO_CFG[ISINKEN] = 0 for the LDO SYS regulator.

5.1.1 LDO timing characteristics

This chapter includes the timing characteristics of the LDO core and LDO system regulators.

5.1.1.1 LDO core timing characteristics

Figure 29 shows the LDO core startup time:

- MCXW71 has been connected in DC-DC Buck mode and no external loads have been added.
- In this configuration, the DC-DC output serves as the power supply for the LDO core.
- The DC-DC input voltage is DCDC_IN = 3.3 V.
- The LDO core input and output voltages are LDO_CORE_IN = DCDC_OUT = 1.8 V and LDO_CORE_OUT = 1.05 V.
- The DC-DC and LDO core are configured in Normal Drive Strength mode.

- In this capture, the red curve represents DCDC_IN, the blue curve represents LDO_CORE_IN/DCDC_OUT, and the yellow curve represents LDO_CORE_OUT.

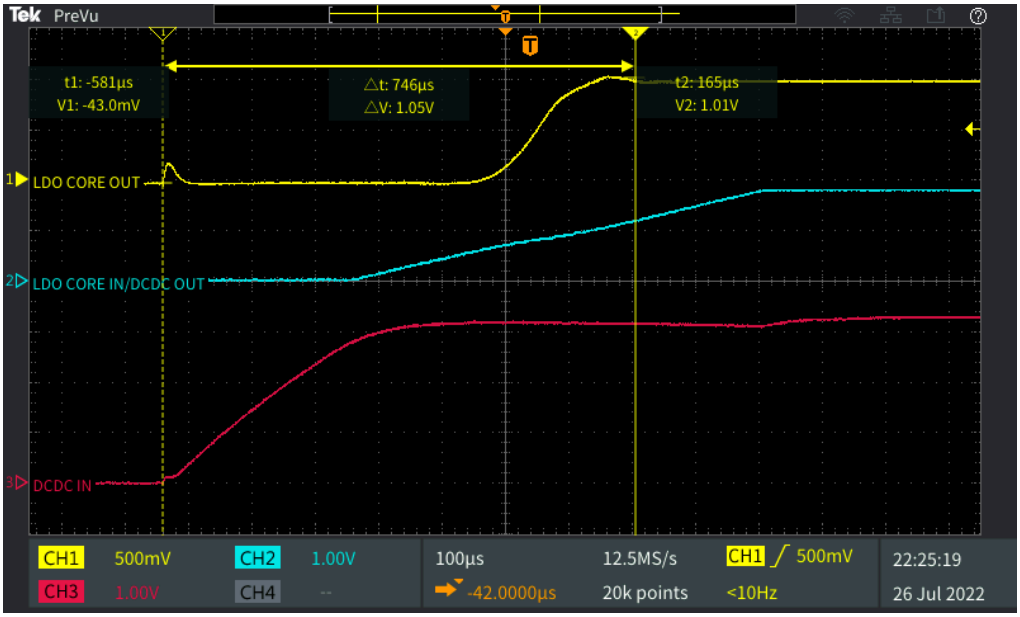


Figure 29. LDO core startup time

Figure 30 shows the LDO core shutdown time:

- MCXW71 has been connected in DC-DC Buck mode and no external loads have been added.
- The DC-DC input voltage is DCDC_IN = 3.3 V.
- The LDO core input and output voltages are LDO_CORE_IN/DCDC_OUT = 1.8 V and LDO_CORE_OUT = 1.05 V.
- The LDO core and DC-DC are configured in Normal Drive Strength mode.
- In this capture, the yellow curve represents LDO_CORE_OUT and the blue curve represents LDO_CORE_IN/DCDC_OUT.

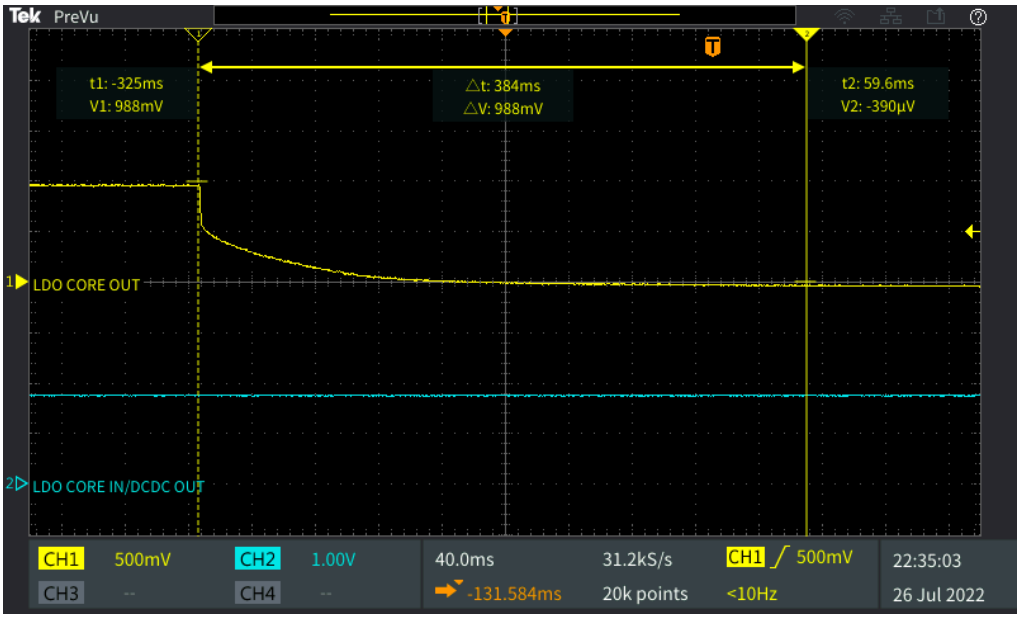


Figure 30. LDO core shutdown time

5.1.1.2 LDO system timing characteristics

Figure 29 shows the LDO system startup time:

- MCXW71 has been connected in DC-DC Buck mode and no external loads have been added.
- The LDO system input and output voltages are LDO_SYS_IN = 3.3 V and LDO_SYS_OUT = 1.8 V.
- The LDO SYS is configured in Normal Drive Strength mode.
- In this capture, the yellow curve represents LDO_SYS_OUT and the blue curve represents LDO_SYS_IN.

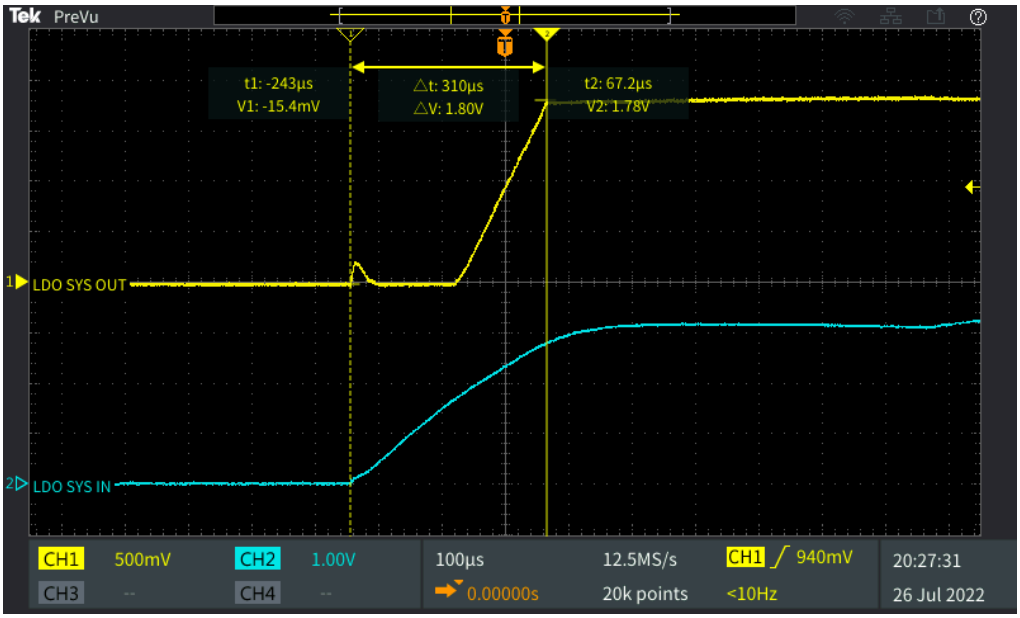


Figure 31. LDO system startup time

5.2 LDO drive strength modes

LDO core and LDO system have two drive strength modes:

- Normal Drive Strength
- Low Drive Strength

In Normal Drive Strength mode, the LDO regulator provides the maximum output current capability. On the other hand, the Low Drive Strength LDO mode limits the output current. The LDO regulators are not targeted to supply external loads but the core and system power domains. If the LDO drive strength mode selection is not critical in your application while the MCU runs in Active mode, keep the default settings, that is, LDO core and LDO system in Normal Drive Strength. If the application requires to enter low power, configure the LDO in Low Drive Strength to reduce power consumption. This approach considers that the power domains supplied through the LDO regulators do not exceed a few microamps and the LDO is not overstressed in this condition. Once the MCU wakes up, you can select the Normal Drive Strength mode for each LDO if required.

5.3 LDO operation in power modes

Similar to the DC-DC buck converter the LDO core and LDO system regulators can be configured in an independent way in Active and Low-power modes. SPC registers, active power mode configuration register (ACTIVE_CFG), and SPC low-power mode configuration register (LP_CFG), provide the configuration alternatives for the corresponding mode.

Table 14 describes the LDO operation modes allowed in each MCXW71 power mode.

Table 14. LDO operation modes

Module	Active	Sleep	Deep Sleep	Power Down	Deep Power Down
LDO core	Normal Drive Strength mode	Normal or Low Drive Strength mode controlled by SPC LP_CFG	• Normal or Low Drive Strength mode controlled by SPC LP_CFG • Off (optional)	• Normal or Low Drive Strength mode controlled by SPC LP_CFG • Off (optional)	Off
LDO system	Normal or Low Drive Strength mode controlled by SPC ACTIVE_CFG	Normal or Low Drive Strength mode controlled by SPC LP_CFG	Normal or Low Drive Strength mode controlled by SPC LP_CFG	Normal or Low Drive Strength mode controlled by SPC LP_CFG	Normal or Low Drive Strength mode controlled by SPC LP_CFG

The LDO core Normal Drive Strength mode is available in all power modes except Deep Power Down mode. When the MCU is in Active mode by default, the LDO core is in Normal Drive Strength mode by default and it is not possible to configure it in Low Drive Strength mode. LDO core Low Drive Strength mode is available in Sleep, Deep Sleep, and Power Down modes. When the MCU is configured to enter in Deep Sleep or Power Down mode, the LDO core can be optionally disabled. When the MCU enters in Deep Power Down mode, the LDO core is forced to the off state. The LDO core output voltage can be updated only if the LDO core is configured in Normal Drive Strength. If the LDO core is configured in Normal Drive Strength mode in the LP_CFG register, the LDO core voltage must be configured at the same value in the ACTIVE_CFG and LP_CFG registers. Before changing the LDO core drive strength mode from Normal to Low Drive Strength mode in the LP_CFG register, disable all HVD/LVD in the corresponding configuration. Enabling any HVD/LVD while the LDO core is in Low Drive Strength, forces the LDO to operate in Normal Drive Strength.

The LDO system Normal Drive Strength mode is available in all power modes. LDO system Low Drive Strength mode is available in all power modes as well. This regulator is the only one that remains enabled when the MCU enters in Deep Power Down mode. The LDO system must be configured at 1.8 V always when the application is running. The LDO system 2.5 V output voltage alternative must be selected only when the MCU must program the eFuses. Therefore, this voltage option is only available when the MCU is running in Active mode. When the LDO system is running at 2.5 V, the LDO is forced to operate in Normal Drive Strength mode.

The LDO system Low Drive Strength mode is available only if the LDO is configured at 1.8 V. Before changing the LDO system drive strength to Low Drive Strength either in ACTIVE_CFG or LP_CFG, ensure to disable all HVD/LVD in the corresponding configuration. Enabling any HVD/LVD while the LDO system is in Low Drive Strength forces the LDO to operate in Normal Drive Strength.

Note: *Any changes to the DC-DC Drive Strength or voltage level cause the SPC -> SC[BUSY] flag to assert to '1' logic level until SPC has completed changing its state to the new value. Therefore, the software must check the SPC -> SC[BUSY] status bit and wait until this bit clears to '0' to ensure that the SPC has completed the drive strength or voltage transition.*

5.4 LDO main configuration registers

This section summarizes the main SPC registers involved in the configuration of the LDO regulators in the MCXW71 MCU. Table 15 describes the SPC registers that configure the behavior of each LDO. For the full peripheral description, refer to the *MCXW71 Reference Manual*.

SPC0 base address 4001_6000h

Table 15. SPC registers

Offset	Register	Width (bits)	Access	Reset value
14h	SPC regulator control register (CNTRL) This register controls the enablement of the SPC regulators.	32	WONCE	0000_0007h
100h	Active power mode configuration register (ACTIVE_CFG) This register controls the settings of the SPC regulators in Active mode.	32	RW	3F10_0E15h
104h	Low-power mode configuration register (LP_CFG) This register controls the settings of the SPC regulators in Low-power modes.	32	RW	0002_1D04h
300h	LDO_CORE configuration register (CORELDO_CFG)	32	RW	0000_0044h
400h	LDO_SYS configuration register (SYSLDO_ CFG)	32	RW	0000_0101h

5.4.1 SPC regulator control register (CNTRL)

This register controls the enablement of the SPC regulators.

- **CNTRL[CORELDO_EN]:** This bit field controls whether the LDO core is turned on (CORELDO_EN = 1) or turned off (CORELDO_EN = 0). By default, the LDO core is turned on. Ensure that the power domains supplied by this domain can be disabled before disabling this LDO. If the LDO core is bypassed, disable the LDO core by writing CORELDO_EN = 0.
- **CNTRL[SYSLDO_EN]:** This bit field controls whether the LDO system is turned on (SYSLDO_EN = 1) or turned off (SYSLDO_EN = 0). By default, the LDO system is turned on. If the LDO system is bypassed, disable the LDO system by writing SYSLDO_EN = 0.

5.4.2 Active power mode configuration register (ACTIVE_CFG)

This register controls the settings of the SPC regulators in Active mode.

- **ACTIVE_CFG[CORELDO_VDD_LVL]:** This bit field controls the LDO core output voltage when the SPC is in Active mode.

Table 16. CORELDO_VDD_LVL and LDO voltage

CORELDO_VDD_LVL	LDO voltage
00b	Reserved
01b	1.05 V
10b	1.1 V
11b	1.15 V

- **ACTIVE_CFG[SYSLDO_VDD_LVL]:** This bit field controls the LDO system output voltage when the SPC is in Active mode.

Table 17. SYSLDO_VDD_LVL and LDO voltage

SYSLDO_VDD_LVL	LDO voltage
0b	1.8 V
1b	2.5 V

- **ACTIVE_CFG[SYSLDO_VDD_DS]:** This bit field controls the LDO system Drive Strength mode when the SPC is in Active mode.

Table 18. SYSLDO_VDD_DS and LDO Drive mode

SYSLDO_VDD_DS	LDO Drive mode
0b	Set to Low Drive Strength
1b	Set to Normal Drive Strength

5.4.3 Low-power mode configuration register (LP_CFG)

This register controls the settings of the SPC regulators in Low-power modes.

- **LP_CFG[CORELDO_VDD_LVL]:** This bit field controls the LDO core output voltage when the SPC is in Low-power mode.

Table 19. CORELDO_VDD_LVL and LDO voltage

CORELDO_VDD_LVL	LDO voltage
00b	Reserved
01b	1.05 V
10b	1.1 V
11b	1.15 V

- **LP_CFG[CORELDO_VDD_DS]:** This bit field controls the LDO core Drive Strength mode when the SPC is in Low-power mode.

Table 20. CORELDO_VDD_DS and LDO Drive mode

CORELDO_VDD_DS	LDO Drive mode
0b	Set to Low Drive Strength
1b	Set to Normal Drive Strength

- **LP_CFG[SYSLDO_VDD_DS]:** This bit field controls the LDO system Drive Strength mode when the SPC is in Low-power mode.

Table 21. SYSLDO_VDD_DS and LDO Drive mode

SYSLDO_VDD_DS	LDO Drive mode
0b	Set to Low Drive Strength
1b	Set to Normal Drive Strength

5.4.4 LDO_CORE configuration register (CORELDO_CFG)

This register controls the settings of the pull-down sink resistor in the LDO core.

CORELDO_CFG[DPDOWN_PULLDOWN_DISABLE]: This configuration register is used to control whether the pull-down sink resistor is enabled or disabled in the LDO core. It is used to discharge the LDO output voltage fast when this regulator is shut down in Deep Power Down mode. This resistor is enabled by default and it is recommended not to change this setting.

5.4.5 LDO_SYS configuration register (SYSLDO_CFG)

This register controls the settings of the pull-down sink resistor in the LDO system.

SYSLDO_CFG[ISINKEN]: This configuration register is used to control whether the pull-down sink resistor is enabled or disabled in the LDO system. It is used to discharge the LDO output voltage fast when this regulator is shut down. This resistor is enabled by default and it is recommended not to change this setting.

5.5 LDO electrical characteristics

This chapter includes the electrical characteristics of the LDO core and LDO system regulators.

5.5.1 LDO core electrical characteristics

Table 22 summarizes the LDO core regulator specifications.

Table 22. LDO core regulator specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_LDO_CORE_IN	LDO core input voltage	1.25	-	3.6	V	1, 2
V_LDO_CORE_OUT	LDO core output voltage: • Normal Drive Strength mode • Low Drive Strength mode	1.05 1.05	- -	1.15 1.15	V	
I_LDO_CORE_LOAD	LDO core max load current at LDO output: • Active mode: V_LDO_CORE_IN ≥ 1.5 V • Active mode: V_LDO_CORE_IN < 1.5 V • Low-power mode: V_LDO_ CORE_IN ≥ 1.5 V • Low-power mode: V_LDO_ CORE_IN < 1.5 V	- - - -	- - - -	60 30 5 5	mA	
I_LDO_CORE_IN	LDO core IN current consumption: • Normal Drive Strength: V_LDO_ CORE_IN ≥ 1.5 V • Normal Drive Strength: V_LDO_CORE_ IN < 1.5 V • Low Drive Strength: V_LDO_CORE_IN ≥ 1.5 V • Low Drive Strength: V_LDO_CORE_IN < 1.5 V	- - - -	- - - -	150 75 0.05 0.05	µA	3

Table 22. LDO core regulator specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Notes
Iinrush	LDO core inrush current	-	-	5 x ILoad	mA	
COUT	LDO core external output capacitor	3.7	4.7	10	µF	
Cdec	LDO core external decoupling capacitor	-	0.1	-	µF	
ESR	External output capacitor equivalent series resistance	-	10	-	mΩ	

Note:

1. *To bypass LDO_CORE, tie VDD_LDO_CORE to VDD_CORE.*
2. *The VDD_LDO_CORE input supply must be set to 200 mV higher than VOUT_CORE in the mid-voltage regulation option (1.05 V). For thr rest of the supported voltage regulation options, it must be set to 250 mV higher than VOUT_CORE.*
3. *In Normal Drive Strength, LDO_CORE draws ~40 µA for every 20 mA of load current. In Low Drive Strength, LDO_CORE draws ~50 µA for every 100 mA of load current.*

5.5.2 LDO system electrical characteristics

Table 23 summarizes the LDO system regulator specifications.

Table 23. LDO system regulator specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_LDO_SYS_IN	LDO system input voltage: • LDO_SYS input supply voltage in Regulation mode • LDO_SYS input supply voltage in Bypass mode • LDO_SYS input in Fuse Programming mode	1.86 1.8 2.75	- - -	3.6 1.98 3.6	V	1
V_LDO_SYS_OUT	LDO system output voltage: • Normal Drive Strength mode • Fuse Programming mode	1.71 2.25	1.8 2.5	1.98 2.75	V	2, 3, 4, 5
I_LDO_SYS_LOAD	LDO system max load current at LDO output: • Normal Drive Strength mode • Low Drive Strength mode • Fuse Programming mode	- - -	- - -	50 2 40	mA	
I_LDO_SYS_IN	LDO system input current consumption: • Normal Drive Strength mode • Low Drive Strength mode	- -	100 70	- -	µA nA	6
Iinrush	LDO core inrush current	-	-	120	mA	7
COUT	LDO core external output capacitor	-	1.5	10	µF	
Cdec	LDO core external decoupling capacitor	-	0.1	-	µF	
ESR	External output capacitor equivalent series resistance	-	30	-	mΩ	

Note:

1. *The regulator automatically switches to pass through (meaning that the driver of the regulator is fully on) with the supply below 1.95 V.*
2. *The LDO_SYS converter generates 1.8 V by default at VOUT_SYS. VOUT_SYS can be used to power VDD_SYS, VDD_RF, VDD_IO_X, VDD_ANA, as long as the max ILOAD is not exceeded.*
3. *VOUT_SYS and VDD_SYS are connected.*
4. *VDD_IO_D must be at least 150 mV higher than the desired VOUT_SYS.*
5. *LDO_SYS can be used to program efuse and in this configuration the output voltage can range between 2.25 V and 2.75 V.*
6. *In Normal Drive Strength, LDO_SYS draws ~100 µA for every 20 mA of load current. For an external output capacitor, the value is 1.5 µF. If the capacitor has a 10 µF value, this value must be 300 mA instead.*

6 Smart power switch

A smart power switch (VBAT) is a low-resistance switch that works with the power management system to implement power-saving mechanisms. It can be used to switch off all or some power domains to obtain the lowest power consumption possible.

However, if the MCXW71 is running on a battery with limited peak current, do not use the smart power switch constantly because the DC-DC introduces a high inrush current during the DC-DC startup, which can shorten the lifespan of the battery. Therefore, for battery-powered applications, it is recommended to use the smart power switch carefully when the system is powered off for an extended period. This switch can also be used for power distribution control of external loads on the board as load and voltage requirements are within the VBAT specifications. For some typical configurations for the smart power switch, see Section 3.

Figure 32 shows the smart power switch architecture in the MCXW71 MCU.

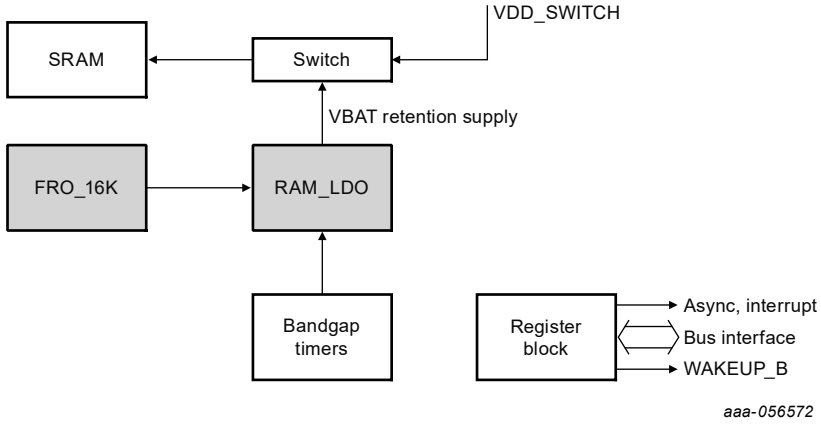


Figure 32. Smart power switch (VBAT) block diagram

6.1 Smart power switch hardware

The smart power switch not only can switch on/off a load, but also includes hardware embedded on it supplied by the independent power domain VDD-SWITCH. This hardware offers extra features to fulfill many application requirements for the MCXW71 MCU.

The following sections describe the smart power switch hardware and its capabilities.

6.1.1 VBAT FRO16K and band gap timers

The smart power switch has an internal 16.384 kHz oscillator that is supplied by the VDD- SWITCH power domain known as the VBAT FRO16K oscillator. FRO16K can remain active in all low-power modes. FRO16K is

used by the VBAT. However, some other peripherals in MCXW71 can also use it. For more information on this feature, refer to the *MCXW71 Reference Manual*.

In addition to the FRO16K oscillator, the smart power switch has two band gap timers:

- Band gap timer 0
- Band gap timer 1

Both band gap timers use FRO16K as a reference clock to determine its counter value and are supplied with the VDD-SWITCH power domain as well. Both band gap timers can turn on the smart power switch when the timer count expires and program the VBAT to switch off the system for a determined period. In the MCXW71 MCU, the band gap timer 0 timeout can be configured in the range of 7.8125 ms to 1 s, and the band gap timer 1 timeout ranges from 1 s to 65,535 s. Before starting any band gap timer, turn on the FRO16K (VBAT -> FROCTLA[FRO_EN] = 1) and enable the LDO RAM band gap bit (VBAT -> LDOCTLA[BG_EN] = 1).

6.1.2 VBAT LDO RAM retention and SRAM retention array

When the smart power switch controls all power domains, it is expected that the application running on the device resets the execution when the VBAT switches off and on. As a result, the application context is lost due to the loss of power on the system. To manage this use case, the smart power switch includes an LDO that can supply an 8 kB SRAM array dedicated to retain the application data when the VBAT is turned off. This feature enables quick recovery after the POR sequence of the device when the smart power switch turns on again.

In general, the LDO RAM retention regulator can be used to keep the power of the SRAM retention at any time or through any Low-power mode in which the application data is lost. However, all access to the SRAM retention address range is not allowed while the LDO RAM is powering this memory. Otherwise, any attempt to access the memory triggers a fault condition. The 8 kB SRAM retention array address range is from 0x2001_A000 – 0x2001_BFFF, which corresponds to the STCM5 in the MCXW71 device. STCM5 supports ECC in MCXW71 devices.

6.1.2.1 VBAT LDO RAM enable sequence

To enable the VBAT LDO RAM retention regulator, it is necessary to follow the below steps.

1. Enable the VBAT FRO16K oscillator: VBAT -> FROCTLA[FRO_EN] = 1
2. Enable the LDO RAM band gap bit: VBAT -> LDOCTLA[BG_EN] = 1
3. To achieve the lowest power consumption, set the LDO RAM in Low Power Refresh mode by enabling the following bit:
   VBAT -> LDOCTLA[REFRESH_EN] = 1
4. Enable the LDO RAM regulator: VBAT -> LDOCTLA[LDO_EN] = 1
5. Wait until the LDO_RDY flag is set, polling the VBAT -> STATUSA[LDO_RDY] bit

6.1.2.2 Powering the SRAM retention memory with VBAT LDO RAM regulator

By default, the SRAM retention memory is powered by the VDD_CORE domain. Therefore, if the application requires the use of a memory retention feature, the software must configure the proper registers to move the SRAM power supply from the VDD_CORE domain to the VBAT LDO RAM regulator. As explained in Section 6.1.2, any attempt to read or write the SRAM retention memory while it is supplied with the LDO RAM regulator results in a fault. Therefore, the application data must be saved in the SRAM address range before switching the memory power supply.

The following steps describe how to configure the VBAT LDO RAM regulator to supply the SRAM retention memory:

1. Enable the VBAT LDO RAM by following the steps described in the Section 6.1.2.1.
2. Configure VBAT -> LDORAMC[ISO] = 1.

3. Configure VBAT -> LDORAMC[SWI] = 1.

Once the VBAT turns on, the software must reverse these steps to switch the SRAM memory power to the VDD_CORE domain and be able to access the SRAM retention memory and load the application context.

1. Configure VBAT -> LDORAMC[SWI] = 0.
2. Configure VBAT -> LDORAMC[ISO] = 0.

6.1.3 VBAT on/off control

The smart power switch turns on by any of the following four methods:

1. After a VBAT power-on reset (POR), the internal wake-up logic turns on the smart power switch automatically. The VBAT POR occurs on a power cycle on the VDD_SWITCH. The VBAT POR resets the register of the smart power switch to the original state. It is the only way that the hardware can reset these values. After a VBAT POR, the smart power switch output is on by default. The VBAT POR is independent from the device POR.
2. Software can enable the VBAT to be turned on after a falling edge on the external SWITCH_WAKEUP_B pin, which is available in MCXW71. The SWITCH_WAKEUP_B pin is pulled up internally.
3. Software can program any of the two VBAT band gap timers embedded in the smart power switch before shutting down the smart power switch to wake up the VBAT after the programmed time.
4. The SPC can activate the switch through the SPC -> CFG MCU active settings when the smart power switch controls the activation of external loads on the board. The software writing the corresponding settings in the SPC -> CFG register deactivates the smart power switch. The SPC registers configure independent settings for the smart power switch on/off control when MCXW71 is in Active mode or in any Low-power mode as follows:
   a. MCXW7 MCU Active mode settings (MCU running and executing code):
   The SPC -> CFG active settings can enable/disable the smart power switch to drive external loads on the circuit. The SPC -> CFG register active settings must not be used to enable/disable the smart power switch when it controls the MCXW7 power supply.
   b. MCXW7 MCU Low-power mode settings:
   The SPC -> CFG low power settings provide configuration bits to deactivate the smart power switch automatically when the device enters in Low-power mode. It activates the smart power switch again once the MCU recovers from Low-power mode by the smart power switch SWITCH_WAKEUP_B button or the internal VBAT band gap timers. The smart power switch low power settings are used to control the MCXW71 power supply. Therefore, to disable the switch when it controls the main power supply of the device, the application software must configure the smart power switch low power settings first, and then execute the sequence to enter Low-power mode.

The SPC -> CFG register enable/disable settings in Active and Low-power modes are described below:

1. SPC->CFG[INTG_PWSWTCH_WKUP_ACTIVE_EN]: VBAT enable bit in Active mode
   Writing this bit to '1' enables the smart power switch when the MCU is in Active mode. Modifying this bit either to '1' or '0' when the MCU is in Active mode and VBAT is already enabled, does not affect. It is used to control external loads.
2. SPC->CFG[INTG_PWSWTCH_SLEEP_ACTIVE_EN]: VBAT disable bit in Active mode
   Writing this bit to '1' disables the smart power switch when the MCU is in Active mode. Modifying this bit either to '1' or '0' when the MCU is in Active mode and VBAT is already disabled, does not affect. It is used to control external loads.
3. SPC->CFG[INTG_PWSWTCH_WKUP_EN]: VBAT enable bit in Low-power mode
   Writing this bit to '1' enables the smart power switch when the MCU exits from any Low-power mode. It is used to enable the main power supply of the device through the smart power switch exiting from a Low-power mode.
4. SPC->CFG[INTG_PWSWTCH_SLEEP_EN]: VBAT disable bit in Low-power mode

Writing this bit to '1' disables the smart power switch when the MCU enters to any Low-power mode. It is used to disable the main power supply of the device through the smart power switch entering in a Low-power mode.

The application software must not enable "INTG_PWSWTCH_WKUP_ACTIVE_EN" and "INTG_PWSWTCH_SLEEP_ACTIVE_EN" at the same time, as it causes an invalid condition. To turn on the smart power switch while the MCU operates in Active mode, set INTG_PWSWTCH_WKUP_ACTIVE_EN =1 and INTG_PWSWTCH_SLEEP_ACTIVE_EN = 0. On the other hand, to turn off the VBAT, set INTG_PWSWTCH_WKUP_ACTIVE_EN = 0 and INTG_PWSWTCH_SLEEP_ACTIVE_EN = 1 simultaneously. If the application does not use the smart power switch in MCU Active mode, do not write these bits.

For VBAT low-power operation, the software can enable INTG_PWSWTCH_WKUP_EN and INTG_PWSWTCH_SLEEP_EN simultaneously to switch off the VBAT while MCXW71 is in Low-Power mode and turn it on again when the device exits from low power. It is possible to enable any of the VBAT control bits individually for the Low-Power modes depending on application requirements and the expected operation. If the application does not use the smart power switch in MCU Low-Power modes, do not write these bits.

If the software configures the smart power switch to wake up either through the SWITCH_WAKEUP_B external pin or from any of the programmable band gap timers, the software must clear the corresponding status flag. Then set INTG_PWSWTCH_WKUP_ACTIVE_EN = 1 and INTG_PWSWTCH_SLEEP_ACTIVE_EN = 0 to complete the smart power switch activation and prepare the hardware for the next smart power switch shutdown sequence in advance.

Section 7.3 provides some snippet code showing how to enable the main features of the smart power switch.

6.2 Smart power switch main configuration registers

This section summarizes the SPC and VBAT main registers involved in the configuration of the smart power switch in the MCXW71 MCU.

Table 24 shows the SPC registers that configure the DC-DC behavior. For the full peripheral description, refer to the *MCXW71 Reference Manual*.

SPC0 base address 4001_6000h

Table 24. SPC register

Offset	Register	Width (bits)	Access	Reset value
20h	SPC configuration register (CFG) This register controls the smart power switch on and off states in MCU Active and Low Power modes	32	RW	0000_0000h

Table 25 shows the VBAT registers that configure the DC-DC behavior.

VBAT0 base address 4002_B000h

Table 25. VBAT registers

Offset	Register	Width (bits)	Access	Reset value
10h	Status A (STATUSA) This register contains the status flags related with the VBAT turn-on events	32	W1C	0000_0001h
20h	Wake-up Enable A (WAKENA) This register enables/disables the smart power switch to turn-on source options	32	RW	0000_0001h
200h	FRO16K Control A (FROCTLA)	32	RW	0000_0001h

Table 25. VBAT registers...*continued*

Offset	Register	Width (bits)	Access	Reset value
	This register contains the enable/disable option for the internal 16 kHz VBAT oscillator			
300h	LDO_RAM Control A (LDOCTLA) This register contains the enablement options for the LDO RAM retention regulator	32	RW	0000_0000h
320h	RAM Control (LDORAMC) This register configures the power supply settings for the SRAM retention memory	32	RW	0000_0000h
330h	Bandgap timer 0 (LDOTIMER0) This register contains the enable and timeout settings for the bandgap timer 0	32	RW	0000_0000h
338h	Bandgap timer 1 (LDOTIMER1) This register contains the enable and timeout settings for the bandgap timer 1	32	RW	0000_0000h

6.2.1 SPC configuration register (CFG)

This register controls the smart power switch on and off states in MCU Active and Low-Power modes.

- **CFG[INTG_PWSWTCH_WKUP_ACTIVE_EN]:** VBAT enable bit in Active mode.
  Writing this bit to '1' enables the smart power switch when the MCU is in Active mode. Changing this bit to any other value when the MCU is in Active mode and VBAT is enabled, does not affect it. Ensure not to enable this bit to '1' when INTG_PWSWTCH_SLEEP_ACTIVE_EN = 1. It is used to control external loads.
- **CFG[INTG_PWSWTCH_SLEEP_ACTIVE_EN]:** VBAT disable bit in Active mode.
  Writing this bit to '1' disables the smart power switch when the MCU is in Active mode. Changing this bit to any other value when the MCU is in Active mode and VBAT is turned on, does not affect it. Ensure not to enable this bit to '1' when INTG_PWSWTCH_WKUP_ACTIVE_EN = 1. It is used to control external loads.
- **CFG[INTG_PWSWTCH_WKUP_EN]:** VBAT enable bit in Low-power mode.
  Writing this bit to '1' enables the smart power switch when the MCU exits any Low-power mode. It is used to enable the main power supply of the device through the smart power switch exiting a Low-power mode.
- **CFG[INTG_PWSWTCH_SLEEP_EN]:** VBAT disable bit in Low-power mode.
  Writing this bit to ‘1’ disables the smart power switch when the MCU enters any Low-power mode. It is used to disable the main power supply of the device through the smart power switch entering a Low-power mode.

6.2.2 Status A (STATUSA)

This register contains the status flags related with the VBAT turn-on events.

- **STATUSA[LDO_RDY]:** Read-only status bit.
  This bit can be checked to determine if the LDO RAM retention regulator is enabled and steady. This bit is set to '1' when the LDO RAM is enabled.
- **STATUSA[TIMER1_FLAG]:** Status bit for the bandgap timer 1.
  This bit is set to '1' to indicate that the bandgap timer 1 timeout has expired. Software must be responsible to clear this bit after the timeout event by writing a '1' on this bit.
- **STATUSA[TIMER0_FLAG]:** Status bit for the bandgap timer 0.
  This bit is set to '1' to indicate that the bandgap timer 0 timeout has expired. Software must be responsible to clear this bit after the timeout event by writing a '1' on this bit.
- **STATUSA[WAKEUP_FLAG]:** Status bit for the external SWITCH_WAKEUP_B pin on the device.
  This bit is set to '1' to indicate that the external wake-up pin has been pulled down. Software must be responsible to check and clear this bit after a wake-up button press event by writing a '1' on this bit.

- **STATUSA[POR_DET]:** Status bit for the VBAT power-on reset detection event.
  This bit is set to '1' after a VBAT POR. Software must be responsible to clear this bit after the VBAT POR event by writing a '1' on this bit.

6.2.3 Wakeup enable A (WAKENA)

This register enables/disables the smart power switch to turn-on source options.

- **WAKENA [TIMER1_FLAG]:** This bit can be enabled in '1' to switch on the smart power switch when the band gap timer 1 timeout has been reached. Writing this bit to '0' disables this feature.
- **WAKENA [TIMER0_FLAG]:** This bit can be enabled in '1' to switch on the smart power switch when the band gap timer 0 timeout has been reached. Writing this bit to '0' disables this feature.
- **WAKENA [WAKEUP_FLAG]:** This bit can be enabled in '1' to switch on the smart power switch when the external SWITCH_WAKEUP_B signal is pulled down. Writing this bit to '0' disables this feature.

6.2.4 FRO16K control A (FROCTLA)

This register contains the enable/disable option for the internal 16 kHz VBAT oscillator.

- **FROCTLA[FRO_EN]:** Writing this bit to '1' enables the VBAT FRO16K oscillator. This oscillator is enabled by default. Ensure that the FRO16K oscillator is enabled before using the band gap timers or the LDO RAM retention regulator.

6.2.5 LDO RAM control A (LDOCTLA)

This register contains the enablement options for the LDO RAM retention regulator.

- **LDOCTLA[REFRESH_EN]:** This bit enables the LDO RAM Refresh mode, which decreases the LDO power consumption. LDO RAM enters Refresh mode by setting this bit in '1'.
- **LDOCTLA[LDO_EN]:** This bit activates the LDO RAM. Before setting this bit to '1' to enable the LDO RAM regulator, it is required to follow the sequence described in Section 6.1.2.1.
- **LDOCTLA[BG_EN]:** This bit enables the LDO RAM band gap required as part of the LDO RAM enable sequence. Writing this bit to '1' enables the LDO RAM band gap.

6.2.6 RAM control (LDORAMC)

This register configures the power supply settings for the SRAM retention memory.

- **LDORAMC[SWI]:** This bit is used to select the SRAM retention memory power supply between the VDD_CORE domain and the VBAT LDO RAM. To select the LDO RAM, it is required to set SWI = 1. To select the VDD_CORE, SWI must be 0. Before selecting the VBAT LDO RAM as the power supply for the SRAM retention memory, it is required to set LDORAMC[ISO] = 1.
- **LDORAMC[ISO]:** This bit must be activated to '1' to isolate the SRAM memory power supply from the rest of the memory and place the array in Low-power retention mode before switching the SRAM supply to the VBAT LDO RAM.

6.2.7 Band gap timer 0 (LDOTIMER0)

This register contains the enable and timeout settings for the band gap timer 0.

- **LDOTIMER0[TIMEN]:** Write this bit to '1' to enable the band gap timer 0. The timer starts counting immediately after writing this bit. Therefore, this bit must be written lastly as a part of the band gap timer enable sequence. Before updating the VBAT timeout, ensure that this bit is disabled, TIMEN = 0.
- **LDOTIMER0[TIMCFG]:** This 3-bit bit field configures the band gap timer 0 timeout value.

Table 26 shows the timeout options.

Table 26. Band gap timer 0

LDOTIMER0[TIMCFG]	Band gap timer 0 timeout
000b	1 s
001b	500 ms
010b	250 ms
011b	125 ms
100b	62.5 ms
101b	31.25 ms
110b	15.625 ms
111b	7.8125 ms

6.2.8 Band gap timer 1 (LDOTIMER1)

This register contains the enable and timeout settings for the band gap timer 1.

- **LDOTIMER1[TIMEN]:** Write this bit to '1' to enable the band gap timer 1. The timer starts counting immediately after writing this bit. Therefore, this bit must be written lastly as a part of the band gap timer enable sequence. Before updating the VBAT timeout, ensure that this bit is disabled, TIMEN = 0.
- **LDOTIMER1[TIMCFG]:** This 24-bit bit field configures the band gap timer 1 timeout value. It can be configured in the range from 1 s to 65,535 s with a resolution of 1 s per increment in the TIMCFG value.

6.3 Smart power switch electrical characteristics

Table 27 summarizes the smart power switch core specifications. The SWITCH_WAKEUP_B pad is internally pulled up to the switch input through a resistor. It can be pulled down to wake up the smart power switch. To generate a valid internal wake-up signal successfully, the maximum value of the SWITCH_WAKEUP_B pulldown voltage is 0.7 V, and duration time must be larger than 1 µs.

Table 27. Smart power switch core specifications

Symbol	Description	Min	Typ	Max	Unit
V_SWITCH_IN	VDD_SWITCH input voltage	1.9	-	3.6	V
I_SWITCH_OUT	Smart power switch output load current	-	-	40	mA
Ron	Switch series resistance at the on state	-	-	3	Ω
I_leakage1	Typical leakage current when V_SWITCH_IN = 2.7 V at 25 °C	-	4	-	nA
I_leakage2	Maximum leakage current when V_SWITCH_IN = 3.3 V at 25 °C	-	-	1	µA

7 Application initialization requirements

This section provides some software examples to control the features and configurations of the power management modules reviewed in this document for MCXW71 MCUs.

7.1 DC-DC software enablement

This section provides two API examples that configure the DC-DC when the MCU runs in Active mode and Low-Power modes. It shows how to configure each voltage option, and how to set the drive strength mode to Normal, Low drive or Pulsed Refresh mode, considering the DC-DC restrictions.

7.1.1 DC-DC voltage and drive mode selection in Active mode

The following snippet code shows an API example configuring the DC-DC output voltage and drive strength mode in Active mode (MCU is in Active mode). The gApp_SetDCDCParametersActiveMode API has two inputs:

- DC-DC voltage
- DC-DC Drive Strength mode

The valid input parameters can be found in the enum prototypes for DC-DC voltage and drive strength mode. This API rejects the voltage and drive strength mode when the input parameters are not correct. In such a case, the DC-DC Configuration mode is not valid when DC-DC = 2.5 V in Low Drive Strength. This API is called during the application startup, after exiting from Low-power modes, or whenever adjustments to the DC-DC voltage or drive mode are required at execution time.

```
typedef enum
{
    gDCDCVoltage1P25,
    gDCDCVoltage1P35,
    gDCDCVoltage2P5,
    gDCDCVoltage1P8
}eDCDCVoltageLvl;

typedef enum
{
    gDCDCPulsedRefresh,
    gDCDCDriveStrengthLow,
    gDCDCDriveStrengthNormal
}eDCDCDriveStrengthMode;

void gApp_SetDCDCParametersActiveMode(eDCDCVoltageLvl
  gDCDC_Voltage, eDCDCDriveStrengthMode gDCDC_DriveStrength)
{
    uint32_t g_DcdcTempConfig;
    /* Return if the DCDC Voltage option is not valid */
    if(gDCDC_Voltage > gDCDCVoltage1P8)
    {
        return;
    }

    /* Return if the DCDC Drive strength option is not valid */
    if(gDCDCDriveStrengthLow > gDCDC_DriveStrength ||
       gDCDC_DriveStrength > gDCDCDriveStrengthNormal)
    {
        return;
    }

    /* Return if the DCDC voltage selection is 2.5V in low drive
       strength, this is not a valid configuration */
    if(gDCDCVoltage2P5 == gDCDC_Voltage &&
      (gDCDCDriveStrengthNormal != gDCDC_DriveStrength))
    {
        return;
    }
```

```
    /* To enable the DCDC option at 2.5V, it is necessary set
       VOUT2P5_SEL, otherwise, this bit must be disabled */
    if(gDCDCVoltage2P5 == gDCDC_Voltage)
    {
        SPC0->DCDC_CFG |= SPC_DCDC_CFG_VOUT2P5_SEL_MASK;
    }
    else
    {
        SPC0->DCDC_CFG &= ~SPC_DCDC_CFG_VOUT2P5_SEL_MASK;
    }

    /* To set the DCDC in low drive strength mode when DCDC is
       in active mode, it is necessary set the voltage selection in
       LP_CFG register as well */
    if(gDCDCDriveStrengthLow == gDCDC_DriveStrength)
    {
        g_DcdcTempConfig = SPC0->LP_CFG;
        g_DcdcTempConfig &= ~SPC_LP_CFG_DCDC_VDD_LVL_MASK;
        g_DcdcTempConfig |=
        SPC_LP_CFG_DCDC_VDD_LVL(gDCDC_Voltage);
        SPC0->LP_CFG = g_DcdcTempConfig;

        /* Wait the SPC to be steady */
        while(SPC0->SC & SPC_SC_BUSY_MASK);
    }

    /* Set the DCDC voltage and drive strength mode */
    g_DcdcTempConfig = SPC0->ACTIVE_CFG;
    g_DcdcTempConfig &= ~(SPC_ACTIVE_CFG_DCDC_VDD_LVL_MASK |
                          SPC_ACTIVE_CFG_DCDC_VDD_DS_MASK);
    g_DcdcTempConfig |=
         (SPC_ACTIVE_CFG_DCDC_VDD_LVL(gDCDC_Voltage) |
          SPC_ACTIVE_CFG_DCDC_VDD_DS(gDCDC_DriveStrength));
    SPC0->ACTIVE_CFG = g_DcdcTempConfig;

    /* Wait the SPC to be steady */
    while(SPC0->SC & SPC_SC_BUSY_MASK);
}
```

7.1.2 DC-DC voltage and drive mode selection in Low-power mode

The following snippet code shows an API example that configures the DC-DC output voltage and drive strength mode in Low-power mode (when the MCU is in any Low-power mode, such as, Sleep, Deep Sleep, Power Down). The gApp_SetDCDCParametersLowPowerMode API has two inputs:

- DC-DC voltage
- DC-DC Drive Strength mode

The valid input parameters can be found in the enum prototypes for DC-DC voltage and drive strength mode. This API rejects the voltage and drive strength mode when the input parameters are not correct. In such a case, the DC-DC Configuration mode is not valid when DC-DC = 2.5 V in Low Drive Strength. This API is called by the application only before going to low power.

```
typedef enum
{
    gDCDCVoltage1P25,
    gDCDCVoltage1P35,
    gDCDCVoltage2P5,
```

```
    gDCDCVoltage1P8
}eDCDCVoltageLvl;

typedef enum
{
    gDCDCPulsedRefresh,
    gDCDCDriveStrengthLow,
    gDCDCDriveStrengthNormal
}eDCDCDriveStrengthMode;

void gApp_SetDCDCParametersLowPowerMode(eDCDCVoltageLvl
      gDCDC_Voltage, eDCDCDriveStrengthMode gDCDC_DriveStrength,
      uint16_t gDCDC_PulseRefreshCnt)
{
    uint32_t g_DcdcTempConfig;

    /* Return if the DCDC Voltage option is not valid */
    if(gDCDC_Voltage > gDCDCVoltage1P8)
    {
        return;
    }

    /* Return if the DCDC Drive strength option is not valid */
    if(gDCDC_DriveStrength > gDCDCDriveStrengthNormal)
    {
        return;
    }

    /* Return if the DCDC voltage selection is 2.5V and DCDC
       is not in normal drive strength mode, this is not a valid
       configuration */
    if(gDCDCVoltage2P5 == gDCDC_Voltage &&
      (gDCDCDriveStrengthNormal != gDCDC_DriveStrength))
    {
        return;
    }

    /* To enable the DCDC option at 2.5V, it is necessary set
       VOUT2P5_SEL, otherwise, this bit must be disabled */
    if(gDCDCVoltage2P5 == gDCDC_Voltage)
    {
        SPC0->DCDC_CFG |= SPC_DCDC_CFG_VOUT2P5_SEL_MASK;
    }
    else
    {
        SPC0->DCDC_CFG &= ~SPC_DCDC_CFG_VOUT2P5_SEL_MASK;
    }

    /* Procedure to set the DCDC in Pulsed Refresh Mode. Only
       valid for Deep Sleep and Power Down Modes */
    if(gDCDCPulsedRefresh == gDCDC_DriveStrength)
    {
        /* Disable LVD and HVD in all power domains, this is
           required in Pulsed Refresh Mode */
        SPC0->LP_CFG &= ~(SPC_LP_CFG_IO_HVDE_MASK |
        SPC_LP_CFG_SYS_HVDE_MASK | SPC_LP_CFG_CORE_HVDE_MASK | \
        SPC_LP_CFG_IO_LVDE_MASK |
        SPC_LP_CFG_SYS_LVDE_MASK | SPC_LP_CFG_CORE_LVDE_MASK);

        /* Set the DCDC Pulse Refresh Counter Value */
```

```
        SPC0->DCDC_BURST_CFG = (SPC0->DCDC_BURST_CFG
           & ~SPC_DCDC_BURST_CFG_PULSE_REFRESH_CNT_MASK) |
           SPC_DCDC_BURST_CFG_PULSE_REFRESH_CNT(gDCDC_PulseRefreshCnt);
    }

    /* Set the DCDC voltage and drive strength mode */
    g_DcdcTempConfig = SPC0->LP_CFG;
    g_DcdcTempConfig &= ~(SPC_LP_CFG_DCDC_VDD_LVL_MASK |
             SPC_LP_CFG_DCDC_VDD_DS_MASK);
    g_DcdcTempConfig |= (SPC_LP_CFG_DCDC_VDD_LVL(gDCDC_Voltage) |
             SPC_LP_CFG_DCDC_VDD_DS(gDCDC_DriveStrength));
    SPC0->LP_CFG = g_DcdcTempConfig;

    /* Wait the SPC to be steady */
    while(SPC0->SC & SPC_SC_BUSY_MASK);
}
```

7.2 LDO core and LDO system software enablement

This section provides two API examples that configure the LDO-CORE and LDO-SYS when the MCU runs in Active mode and Low-power modes. It shows how to configure each voltage option and set the drive strength mode to Normal or Low Drive considering the restrictions of each LDO.

7.2.1 LDO voltage and drive mode selection in Active mode

The following snippet code shows an API example configuring the LDO output voltage and drive strength mode in Active mode (MCU is in Active mode). The gApp_SetLDOParametersActiveMode API has three inputs:

- LDO core voltage
- LDO system voltage
- LDO system Drive Strength mode

The valid input parameters can be found in the enum prototypes. This API rejects the voltage and drive strength mode when the input parameters are not correct. In such a case, the LDO Configuration mode is not valid. This API is called during the application startup, after exiting from Low-power modes, or whenever the DC-DC voltage or drive mode must be adjusted at execution time.

```
typedef enum
{
    gLDOCoreVoltage1P0 = 1,
    gLDOCoreVoltage1P1,
    gLDOCoreVoltage1P15
}eLDOCoreVoltageLvl;

typedef enum
{
    gLDOSysVoltage1P8,
    gLDOSysVoltage2P5
}eLDOSysVoltageLvl;

typedef enum
{
    gLDOSysDriveStrengthLow,
    gLDOSysDriveStrengthNormal
}eLDOSysDriveStrengthMode;

void gApp_SetLDOParametersActiveMode(eLDOCoreVoltageLvl
        gLDOCore_Voltage, eLDOSysVoltageLvl gLDOSys_Voltage,
```

```
        eLDOSysDriveStrengthMode gLDOSys_DriveStrength)
{
    uint32_t g_LDOTempConfig;

    /* Return if the LDO Core Voltage is out of the range */
    if(gLDOCoreVoltage1P0 > gLDOCore_Voltage || gLDOCore_Voltage
       > gLDOCoreVoltage1P15)
    {
        return;
    }

    /* Return if the LDO Sys Voltage is out of the range */
    if(gLDOSys_Voltage > gLDOSysVoltage2P5)
    {
        return;
    }

    /* Return if the LDO Sys Drive strength option is not valid */
    if(gLDOSys_DriveStrength > gLDOSysDriveStrengthNormal)
    {
        return;
    }

    /* Return if the LDO Sys voltage selection is 2.5V and LDO
       Sys is not in normal drive strength mode, this is not a valid
       configuration */
    if(gLDOSysVoltage2P5 == gLDOSys_Voltage &&
      (gLDOSysDriveStrengthNormal != gLDOSys_DriveStrength))
    {
        return;
    }

    /* It is required to disable the LVD and HVD in all power
       domains to set the LDO low drive strength mode */
    if(gLDOSysDriveStrengthLow == gLDOSys_DriveStrength)
    {
        /* Disable LVD and HVD in all power domains, this is
           required for LDO Low Drive Strength mode */
        SPC0->ACTIVE_CFG &= ~(SPC_ACTIVE_CFG_IO_HVDE_MASK |
          SPC_ACTIVE_CFG_SYS_HVDE_MASK | SPC_ACTIVE_CFG_CORE_HVDE_MASK |
          SPC_ACTIVE_CFG_IO_LVDE_MASK | SPC_ACTIVE_CFG_SYS_LVDE_MASK |
          SPC_ACTIVE_CFG_CORE_LVDE_MASK);
    }

    /* Set the LDO voltage drive strength mode */
    g_LDOTempConfig = SPC0->ACTIVE_CFG;
    g_LDOTempConfig &= ~(SPC_ACTIVE_CFG_CORELDO_VDD_LVL_MASK
      | SPC_ACTIVE_CFG_SYSLDO_VDD_LVL_MASK |
        SPC_ACTIVE_CFG_SYSLDO_VDD_DS_MASK);
    g_LDOTempConfig |=
      (SPC_ACTIVE_CFG_CORELDO_VDD_LVL(gLDOCore_Voltage)
      | SPC_ACTIVE_CFG_SYSLDO_VDD_LVL(gLDOSys_Voltage) |
      SPC_ACTIVE_CFG_SYSLDO_VDD_DS(gLDOSys_DriveStrength));
    SPC0->ACTIVE_CFG = g_LDOTempConfig;

    /* Wait the SPC to be steady */
    while(SPC0->SC & SPC_SC_BUSY_MASK);
}
```

7.2.2 LDO voltage and drive mode selection in Low-power mode

The following snippet code shows an API example configuring the LDO output voltage and Drive Strength mode in Low-power mode (when the MCU is in any Low-power mode, such as, Sleep, Deep Sleep, Power Down). The gApp_SetLDOParametersLowPowerMode API has three inputs:

- LDO core voltage
- LDO core Drive Strength mode
- LDO system Drive Strength mode

The valid input parameters can be found in the enum prototypes. This API rejects the voltage and Drive Strength mode when the input parameters are not correct. In such a case, the LDO Configuration mode is not valid. This API is called by the application only before going to low power.

```
typedef enum
{
    gLDOCoreVoltage1P0 = 1,
    gLDOCoreVoltage1P1,
    gLDOCoreVoltage1P15
}eLDOCoreVoltageLvl;

typedef enum
{
    gLDOCoreDriveStrengthLow,
    gLDOCoreDriveStrengthNormal
}eLDOCoreDriveStrengthMode;

typedef enum
{
    gLDOSysDriveStrengthLow,
    gLDOSysDriveStrengthNormal
}eLDOSysDriveStrengthMode;

void gApp_SetLDOParametersLowPowerMode(eLDOCoreVoltageLvl
          gLDOCore_Voltage, eLDOCoreDriveStrengthMode
          gLDOCore_DriveStrength, eLDOSysDriveStrengthMode
          gLDOSys_DriveStrength)
{
    uint32_t g_LDOTempConfig;

    /* Return if the LDO Core Voltage is out of the range */
    if(gLDOCoreVoltage1P0 > gLDOCore_Voltage || gLDOCore_Voltage
       > gLDOCoreVoltage1P15)
    {
        return;
    }

    /* Return if the LDO Core Drive strength option is not valid */
    if(gLDOCore_DriveStrength > gLDOCoreDriveStrengthNormal)
    {
        return;
    }

    /* Return if the LDO Sys Drive strength option is not valid */
    if(gLDOSys_DriveStrength > gLDOSysDriveStrengthNormal)
    {
        return;
    }
```

```
    /* To update the LDO Core voltage, it is mandatory set the
       LDO Core in Normal Drive Strength */
    SPC0->LP_CFG |= SPC_LP_CFG_CORELDO_VDD_DS_MASK;

    /* Wait the SPC to be steady */
    while(SPC0->SC & SPC_SC_BUSY_MASK);

    /* The procedure to update the LDO Core voltage depends on
       the selected drive strength mode */
    if(gLDOCoreDriveStrengthLow == gLDOCore_DriveStrength)
    {
        /* Disable LVD and HVD in all power domains, this is
           required for LDO Low Drive Strength mode */
        SPC0->LP_CFG &= ~(SPC_LP_CFG_IO_HVDE_MASK |
          SPC_LP_CFG_SYS_HVDE_MASK | SPC_LP_CFG_CORE_HVDE_MASK |
          SPC_LP_CFG_IO_LVDE_MASK | SPC_LP_CFG_SYS_LVDE_MASK |
          SPC_LP_CFG_CORE_LVDE_MASK);

        /* To update the LDO Core voltage in low drive strength,
           ACTIVE and LP registers should have the same LDO Core
           voltage value */

        /* Set the LDO Core voltage in the ACTIVE_CFG register */
        g_LDOTempConfig = SPC0->ACTIVE_CFG;
        g_LDOTempConfig &= ~SPC_ACTIVE_CFG_CORELDO_VDD_LVL_MASK;
        g_LDOTempConfig |=
          SPC_ACTIVE_CFG_CORELDO_VDD_LVL(gLDOCore_Voltage);
        SPC0->ACTIVE_CFG = g_LDOTempConfig;

        /* Wait the SPC to be steady */
        while(SPC0->SC & SPC_SC_BUSY_MASK);

        /* Set the LDO Core voltage and drive strength mode in
           the LP_CFG register */

        /* Set the LDO Sys drive mode */
        g_LDOTempConfig = SPC0->LP_CFG;
        g_LDOTempConfig &= ~(SPC_LP_CFG_CORELDO_VDD_LVL_MASK
           | SPC_LP_CFG_CORELDO_VDD_DS_MASK |
           SPC_LP_CFG_SYSLDO_VDD_DS_MASK);
        g_LDOTempConfig |=
           (SPC_LP_CFG_CORELDO_VDD_LVL(gLDOCore_Voltage) |
           SPC_LP_CFG_CORELDO_VDD_DS(gLDOCore_DriveStrength) |
           SPC_LP_CFG_SYSLDO_VDD_DS(gLDOSys_DriveStrength));
        SPC0->LP_CFG = g_LDOTempConfig;

        /* Wait the SPC to be steady */
        while(SPC0->SC & SPC_SC_BUSY_MASK);
    }
    else
    {
        /* It is required to disable the LVD and HVD in all power
           domains to set the LDO Sys low drive strength mode */
        if(gLDOSysDriveStrengthLow == gLDOSys_DriveStrength)
        {
            /* Disable LVD and HVD in all power domains, this is
               required for LDO Low Drive Strength mode */
            SPC0->LP_CFG &= ~(SPC_LP_CFG_IO_HVDE_MASK |
             SPC_LP_CFG_SYS_HVDE_MASK | SPC_LP_CFG_CORE_HVDE_MASK |
             SPC_LP_CFG_IO_LVDE_MASK | SPC_LP_CFG_SYS_LVDE_MASK |
```

```
                SPC_LP_CFG_CORE_LVDE_MASK);
        }

        /* If LDO Core is configured in normal drive, it is only
           necessary set the LDO Core voltage */

        /* Set the LDO Sys drive mode */
        g_LDOTempConfig = SPC0->LP_CFG;
        g_LDOTempConfig &= ~(SPC_LP_CFG_CORELDO_VDD_LVL_MASK |
          SPC_LP_CFG_SYSLDO_VDD_DS_MASK);
        g_LDOTempConfig |=
          (SPC_LP_CFG_CORELDO_VDD_LVL(gLDOCore_Voltage) |
          SPC_LP_CFG_SYSLDO_VDD_DS(gLDOSys_DriveStrength));
        SPC0->LP_CFG = g_LDOTempConfig;

        /* Wait the SPC to be steady */
        while(SPC0->SC & SPC_SC_BUSY_MASK);
    }
}
```

7.3 Smart power switch software enablement

This section provides two API examples that configure the smart power switch to wake from the external SWITCH_WAKEUP_B pin and the band gap timer.

7.3.1 Shut down and wake-up from SWITCH_WAKEUP_B pin

The following snippet code shows an API example to configure the smart power switch to wake up from the SWITCH_WAKEUP_B pin and disable the switch in the low-power entry sequence.

The gApp_VBATShutdownExit API is required to complete the wake-up sequence and clear the VBAT flags. The application calls gApp_VBATShutdownExit in the recovery sequence after the loss of power.

The gApp_VBATShutdownEntrySwitchWakeupB API is used to program the smart power switch to be disabled automatically once the device enters in Low-power mode. The application calls gApp_VBATShutdownEntrySwitchWakeupB right before initiating the low-power entry sequence. A successful low-power entry sequence disables the switch.

```
void gApp_VBATShutdownExit(void)
{
  /* Clear all status flags */
  VBAT0->STATUSA |= (VBAT_STATUSA_POR_DET_MASK | VBAT_STATUSA_WAKEUP_FLAG_MASK
 |
           VBAT_STATUSA_TIMER0_FLAG_MASK | VBAT_STATUSA_TIMER1_FLAG_MASK);
  VBAT0->WAKENA &= ~(VBAT_WAKENA_POR_DET_MASK | VBAT_WAKENA_WAKEUP_FLAG_MASK |
           VBAT_WAKENA_TIMER0_FLAG_MASK | VBAT_WAKENA_TIMER1_FLAG_MASK);

  /* Disable Bandgap timers if any is in use to prevent be triggered */
  VBAT0->LDOTIMER0 &= ~VBAT_LDOTIMER0_TIMEN_MASK;
  VBAT0->LDOTIMER1 &= ~VBAT_LDOTIMER1_TIMEN_MASK;

  /* Complete the VBAT turn on sequence */
  SPC0->CFG = SPC_CFG_INTG_PWSWTCH_WKUP_ACTIVE_EN_MASK;

}

void gApp_VBATShutdownEntrySwitchWakeupB(void)
{
```

```
  /* Set the SWITCH_WAKEUP_B pin as VBAT wakeup source */
  VBAT0->WAKENA |= VBAT_WAKENA_WAKEUP_FLAG_MASK;

  /* Prepare VBAT to be disabled in low power and enabled in device wake up */
  SPC0->CFG = SPC_CFG_INTG_PWSWTCH_SLEEP_EN_MASK |
         SPC_CFG_INTG_PWSWTCH_WKUP_EN_MASK;

}
```

7.3.2 Shut down and wake-up from the band gap timer

The following snippet code shows an API example to configure the smart power switch to wake up after the band gap timer 1 timeout expires and disable the switch in the low-power entry sequence.

The gApp_VBATShutdownExit API is required to complete the wake-up sequence and clear the VBAT flags. The application calls gApp_VBATShutdownExit in the recovery sequence after the loss of power.

The gApp_VBATShutdownEntryBandgapTmr1 API is used to program the smart power switch to be disabled automatically once the device enters in Low-power mode. The application calls gApp_VBATShutdownEntryBandgapTmr1 right before initiating the low-power entry sequence. A successful low-power entry sequence disables the switch.

```
void gApp_VBATShutdownExit(void)
{
  /* Clear all status flags */
  VBAT0->STATUSA |= (VBAT_STATUSA_POR_DET_MASK | VBAT_STATUSA_WAKEUP_FLAG_MASK
 |
        VBAT_STATUSA_TIMER0_FLAG_MASK | VBAT_STATUSA_TIMER1_FLAG_MASK);
  VBAT0->WAKENA &= ~(VBAT_WAKENA_POR_DET_MASK | VBAT_WAKENA_WAKEUP_FLAG_MASK |
        VBAT_WAKENA_TIMER0_FLAG_MASK | VBAT_WAKENA_TIMER1_FLAG_MASK);

  /* Disable Bandgap timers if any is in use to prevent be triggered */
  VBAT0->LDOTIMER0 &= ~VBAT_LDOTIMER0_TIMEN_MASK;
  VBAT0->LDOTIMER1 &= ~VBAT_LDOTIMER1_TIMEN_MASK;

  /* Complete the VBAT turn on sequence */
  SPC0->CFG = SPC_CFG_INTG_PWSWTCH_WKUP_ACTIVE_EN_MASK;

}

void gApp_VBATShutdownEntryBandgapTmr1(uint16_t gVBAT_BandgapTimeout)
{
  /* Set the Bandgap Timer 1 as VBAT wakeup source */
  VBAT0->WAKENA |= VBAT_WAKENA_TIMER1_FLAG_MASK;

  /* Enable FRO16K oscillator */
  VBAT0->FROCTLA |= VBAT_FROCTLA_FRO_EN_MASK;

  /* Enable LDO RAM bandgap in refresh mode */
  VBAT0->LDOCTLA |= VBAT_LDOCTLA_BG_EN_MASK | VBAT_LDOCTLA_REFRESH_EN_MASK;

  /* Configure the Bandgap Timer 1 timeout and start the timer */
  VBAT0->LDOTIMER1 = ((VBAT0->LDOTIMER1 & ~VBAT_LDOTIMER1_TIMCFG_MASK) |
         VBAT_LDOTIMER1_TIMCFG(gVBAT_BandgapTimeout));
  VBAT0->LDOTIMER1 |= VBAT_LDOTIMER1_TIMEN_MASK;

  /* Prepare VBAT to be disabled in low power and enabled in device wake up */
  SPC0->CFG = SPC_CFG_INTG_PWSWTCH_SLEEP_EN_MASK |
        SPC_CFG_INTG_PWSWTCH_WKUP_EN_MASK;
```

```
}
```

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9 Revision history

Table 28 summarizes the revisions to this document.

Table 28. Revision history

Document ID	Release date	Description
AN14387 v.2.0	05 September 2025	Updated VDD_SWITCH minimum voltage in Table 4
AN14387 v.1.0	10 September 2024	Initial public release

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