AN14033

DSI3 communication procedure recommendations for FXPS7140X

Rev. 1 — 5 December 2023 Application note

Document information

Information	Content
Keywords	DSI3, automotive pressure, satellite pressure, passive safety, airbag
Abstract	This application note describes the DSI3 power up, initialization, and normal mode procedures for the FXPS7140X absolute pressure sensor.

1 Introduction

The purpose of this document is to describe the DSI3 power up, initialization, and normal mode procedures for the FXPS7140X absolute pressure sensor.

2 Applicable parts

This document applies to the following NXP sensors:

FXPS71407ST1	DSI3 compatible pressure sensor	HQFN16, 4 mm × 4 mm × 1.98 mm, DSI3 pressure sensor

3 FXPS7140X application schematic

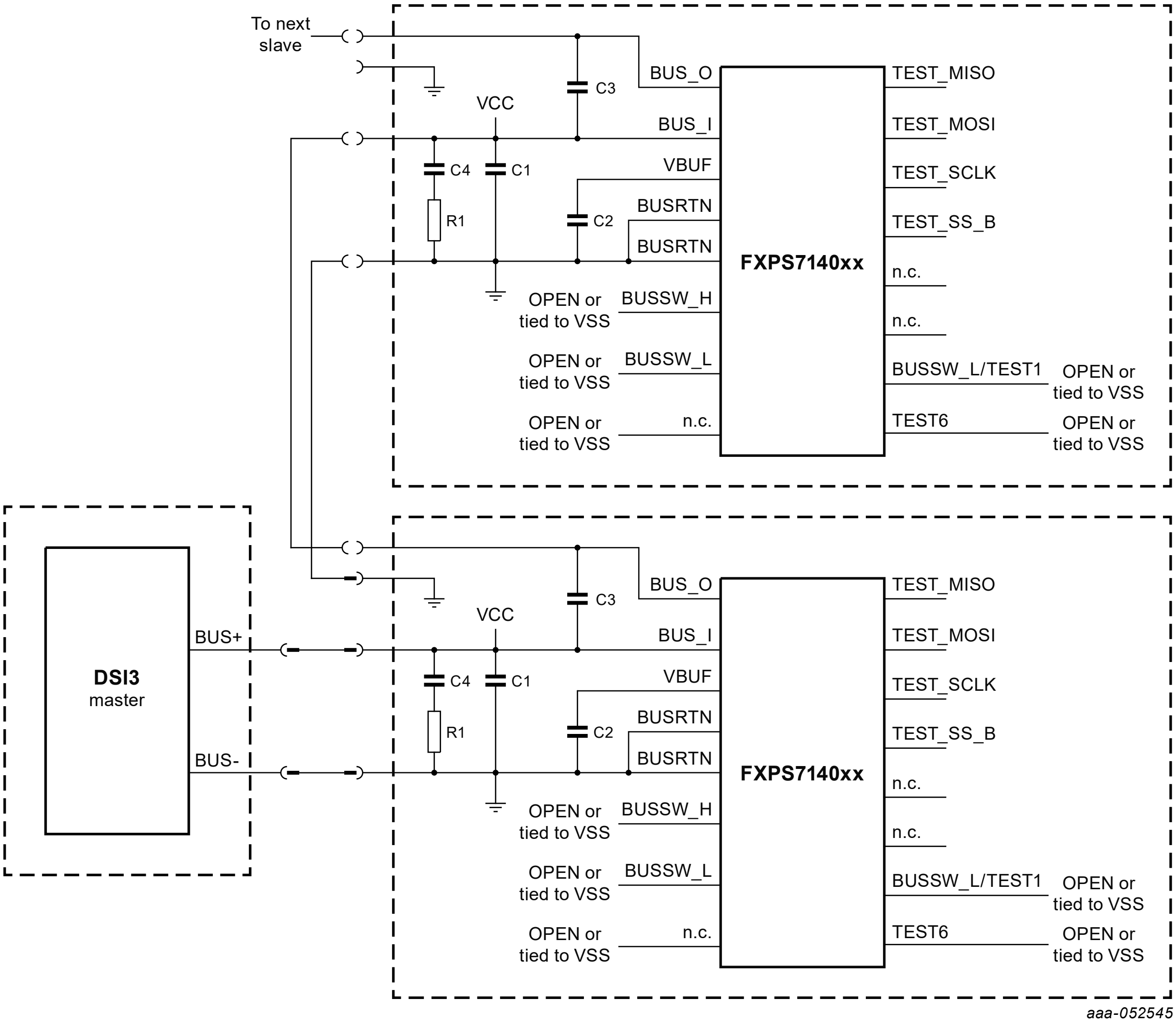

Figure 1. FXPS7140X application schematic

Table 1. Recommended external components for DSI3 mode

Reference designator	Component type	Description	Comment
R1	general purpose	330 Ω, 5 %, 200 ppm	The system level communication and electromagnetic compatibility (EMC) testing determine the optimal value of this component.
C1	ceramic	220 pF, 10 %, 50 V minimum, X7R	The system level communication and EMC testing determine the optimal value of this component.
C2	ceramic	0.47 µF, 10 %, 10 V minimum, X7R	Based on the system level microcut immunity requirement the optimal value of this component is determined. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22 µF. The maximum specified value including all tolerances is 2 µF.
C3	ceramic	1000 pF, 10 %, 50 V minimum, X7R	The system level communication and EMC testing determine the optimal value of this component.
C4	ceramic	2200 pF, 10 %, 50 V minimum, X7R	The system level communication and EMC testing determine the optimal value of this component.

4 Apply power to the FXPS7140X

Power must be applied to the FXPS7140X with the ramp rates specified in the operating range – DSI/PSI5 table in the product data sheet. The device is verified to start up properly with ramp rates from 10 V/s to 10 V/µs. See Figure 2.

The device is available for command and response mode (CRM) commands within 13.5 ms of power-on reset (POR) release. If discovery mode is used for physical address assignment, the supply ramp time must be fast enough to allow the device to participate in discovery mode. From the satellite perspective, the discovery mode window is from 5.0 ms to 13.5 ms of POR release. From the controller perspective, this time must be known with reasonable accuracy.

The time from the controller enabling the bus until the satellite POR release results in a time skew between the controller and the satellite interpretation of the discovery mode window start time. With a slow supply ramp time, relative to the discovery mode window start time (< 5 V/ms), the time skew between the controller and satellite could result in the satellite missing the discovery mode transmissions from the controller.

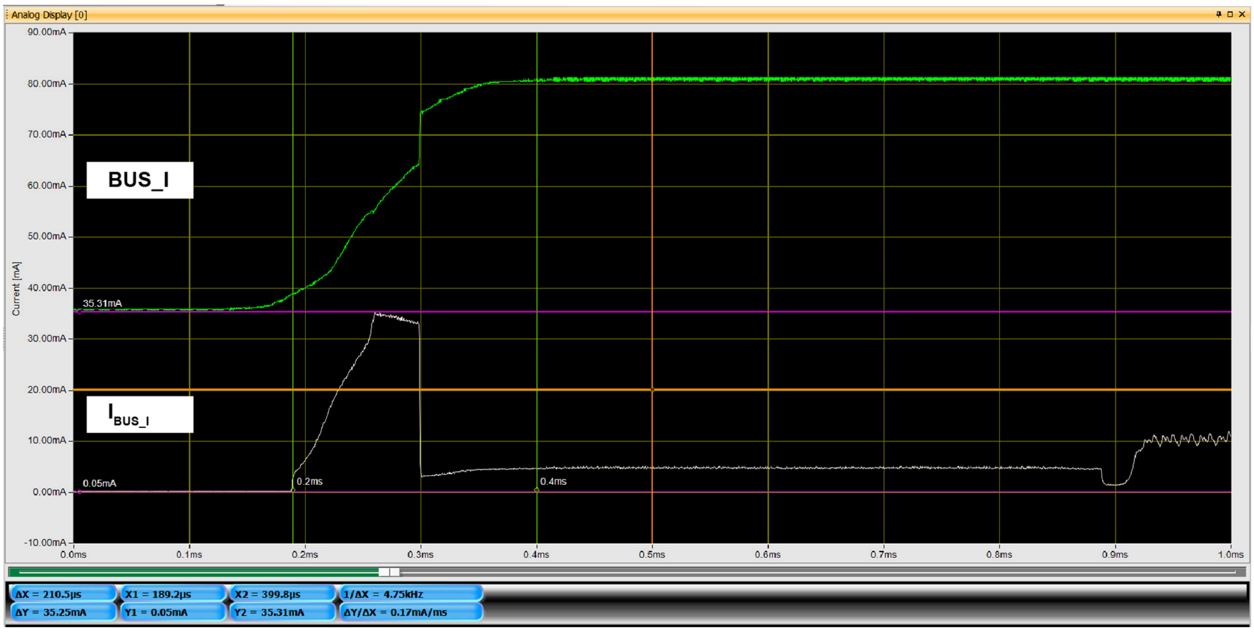

Figure 2. Example DSI3 supply ramp

5 Assign addresses to the satellites

The device supports all three address assignment methods described in the DSI3 standard. They are single, parallel connected, and daisy chain satellites as described in the following sections.

5.1 Single device network

DSI3 supports the capability to connect one satellite to a controller in a point-to-point connection. With this connection method, the physical address of the satellite must be either 0x00 or be known by the controller as described in Section 5.1.1 and Section 5.1.2.

5.1.1 Unprogrammed physical address (0x00)

A single device network with an unprogrammed physical address can be initialized using either of the following two methods:

- Discovery mode as described in Section 5.3 "Multiple satellite system connected in a resistor connected daisy chain"
- CRM

The following CRM procedure is necessary to complete the address assignment of an unprogrammed satellite with a physical address of 0x00.

Delay a minimum of 13.5 ms after applying power (the maximum value of t_{START_DISC}).

Using CRM, send a global write command to the physical address register (PHYSADDR), setting the physical address to a nonzero value. The example in Figure 3 shows the command necessary to program the physical address to 0x1. The physical address register is 0x18 and the data written is 0x01.

Description	Satellite address (hex)	Command (hex)	Register address (hex)	Register data (hex)	Full message (hex)
Command	0	8	18	01	0x08180112
Response	1	8	00	01	0x18000152

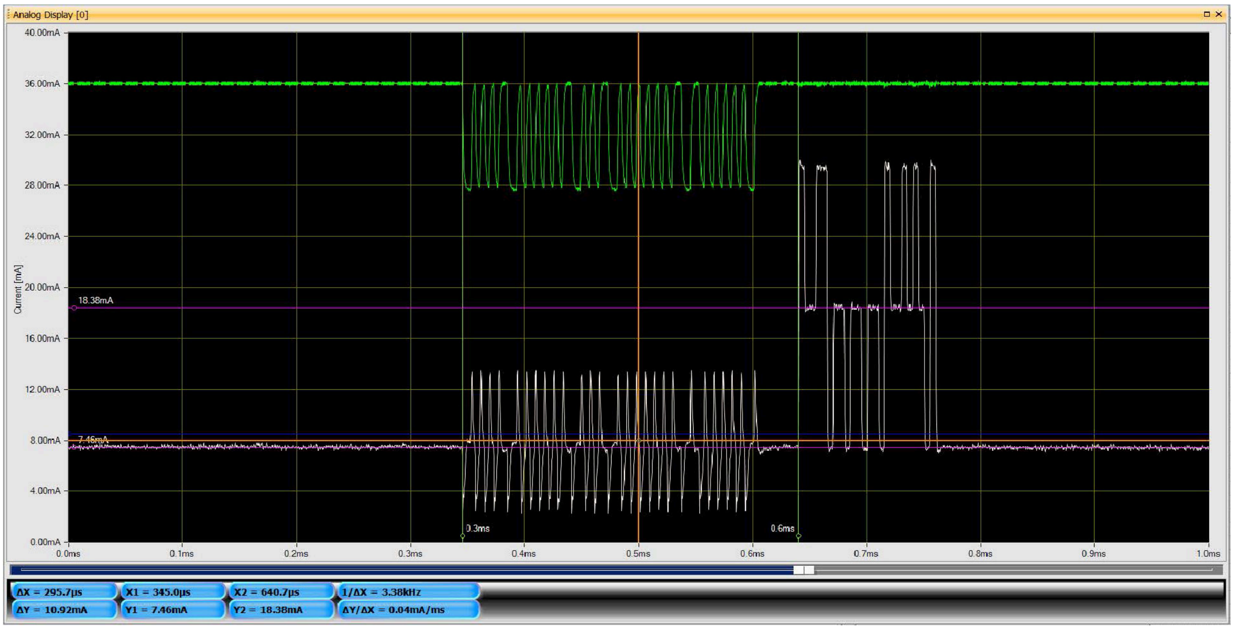

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Figure 3. Controller and satellite signals for the global write to the PHYSADDR register

5.1.2 Preprogrammed physical address

No action is necessary if the single satellite device has a preprogrammed address. Proceed to Section 6 "Initialize and configure the devices".

5.2 Multiple satellite system connected in parallel

DSI3 supports the capability to connect multiple satellites to a controller in a parallel or start connection. With this connection method, the physical addresses of the satellites must be known by the controller. No other action is necessary for address assignment. Proceed to Section 6 "Initialize and configure the devices".

5.3 Multiple satellite system connected in a resistor connected daisy chain

Discovery mode follows the sequence listed below. Figure 4 shows a timing diagram of the discovery protocol for a four satellite segment.

1. The controller powers up the bus segment to a known state.
2. The controller transmits the discovery command.

3. After a predetermined delay ($t_{START\_DISC\_RSP}$), all satellites without a physical address activate a current ramp to the 2 × response current at a ramp rate of i_{DISC_RAMP}.
4. Each satellite monitors the current through its sense resistor (Δi_{SENSE}).
   a. If the current is above i_{RESP}, the satellite disables its response current, increments its physical address counter, and waits for the next discovery command.
   b. If the current is low (Δi_{SENSE} less than i_{RESP}), the satellite continues to ramp its response current to 2 × i_{RESP} in time $t_{DISC\_RAMP\_RSP}$, and maintains the current at 2 × i_{RESP} for time $t_{DISC\_IDLE\_RSP}$.
   c. After time $t_{DISC\_IDLE\_RSP}$, if a satellite has not detected a current through its current sense resistor of i_{RESP}, the satellite accepts the physical address '1' and disables its response current.
5. After a predefined period (t_{PER_DISC}), the controller transmits another discovery command.
6. If the sense current is low, steps 3 and 4 are repeated, with the satellite accepting the address in its address assignment counter.
7. The controller repeats step 5 until it has transmitted discovery commands for all the satellites it expects on the bus.

Device initialization can now begin using CRM. Proceed to [Section 6 "Initialize and configure the devices"](#).

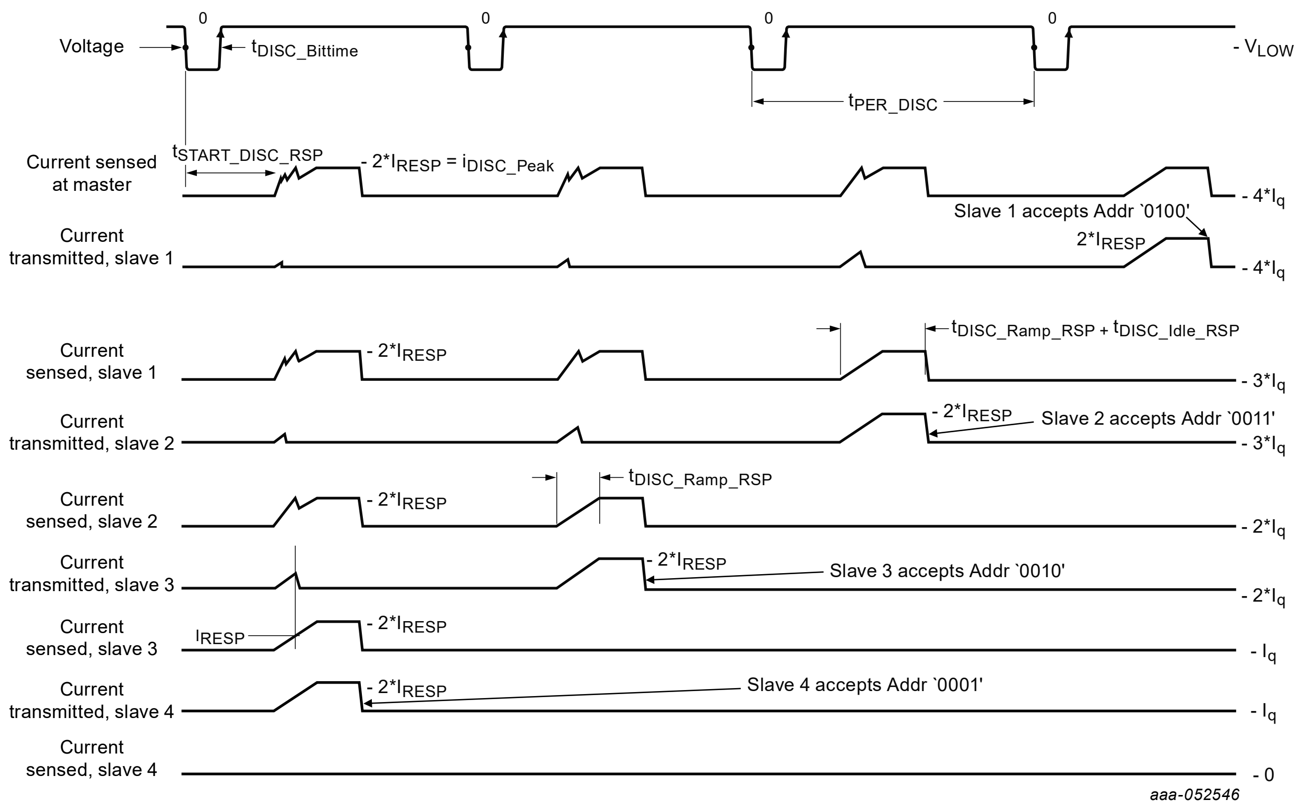


Figure 4. Four (4) device discovery mode process

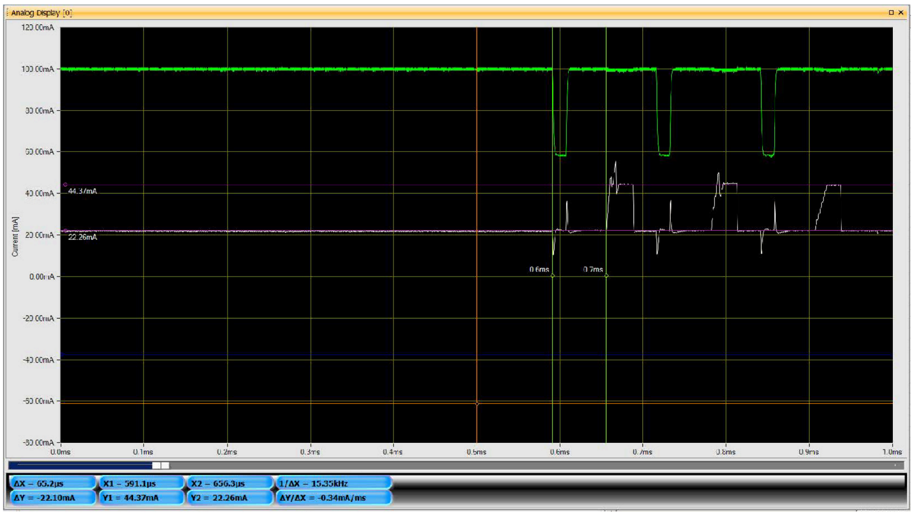


Figure 5. Example 3 satellite discovery mode

5.4 Multiple satellite system connected in a high side switch connected daisy chain

DSI3 supports the capability to connect multiple satellites to a controller in a daisy chain connected by high side bus switches. Discovery mode is preferred to this connection method and therefore the switch connected daisy chain is not covered by this application note.

6 Initialize and configure the devices

Once all satellites on the bus have a unique physical address, the controller can initialize and configure the satellites as desired for the application. The following sections describe the recommended CRM commands to initialize, configure, and test a bus with two FXPS7140X devices.

Figure 6 shows an example timing diagram for DSI3 startup and initialization and how it compares to P0 startup.

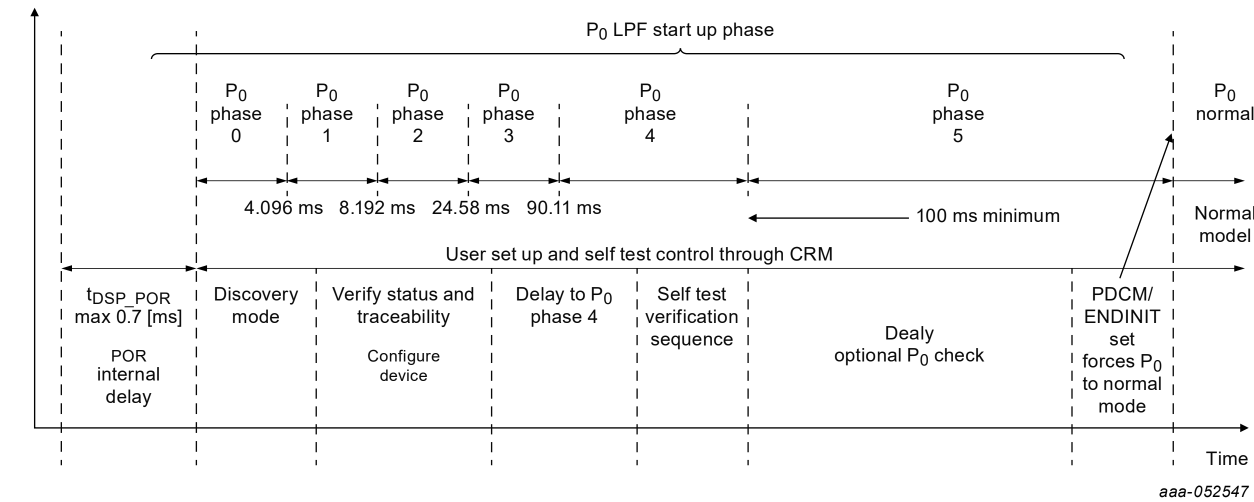
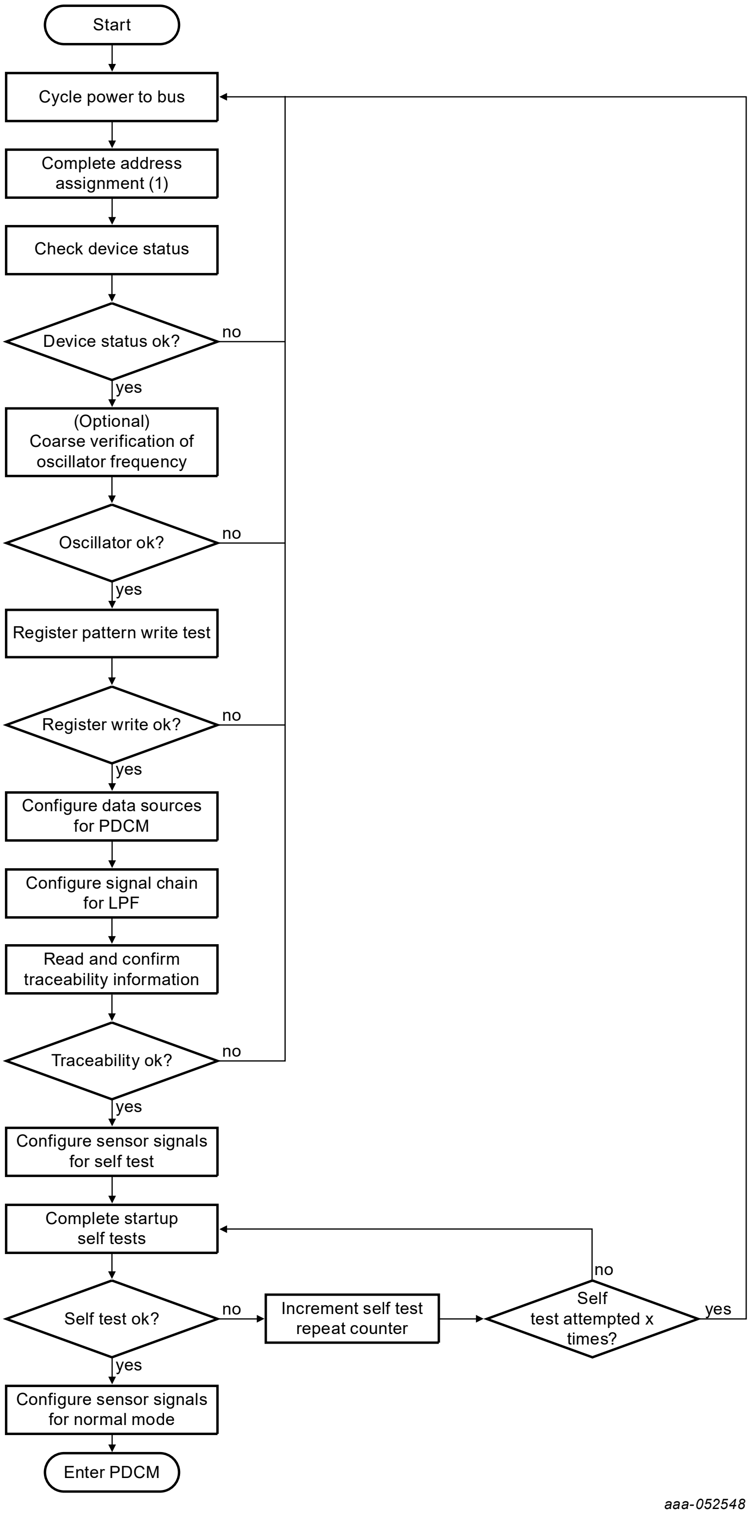


Figure 6. Example DSI3 initialization timing diagram

Table 2 shows a timing table for the procedure used in this application note. Figure 7 shows a high-level flowchart for the procedure used in this application note.

Table 2. FXPS7140X initialization timing

Function	Start time	End time	Unit
POR	0.00	5.94	ms
Discovery end	5.94	6.07	ms
CRM start	6.07	26.97	ms
Device status	26.97	28.12	ms
Oscillator	29.97	57.97	ms
Device status	57.97	58.62	ms
Register pattern write	58.97	66.62	ms
Configuration #1	66.97	71.62	ms
Traceability	71.97	76.62	ms
Delay to P_0 phase 4	76.62	101.47	ms
Common mode self-test	101.47	174.62	ms
Fixed pattern self-test	174.97	178.62	ms
Digital self-test	178.97	211.12	ms
Device status	313.97	314.62	ms
Enter periodic data collection mode (PDCM) (set ENDINIT)	314.97	-	ms



(1) Complete address assignment (Section 5)

Figure 7. High-level DSI3 flowchart for the FXPS7140X

6.1 Confirm device status

The first step after address assignment is to confirm proper CRM communication and the expected status of each device. This can be accomplished by reading the DEVSTAT registers of each device as shown in Figure 8. The DEVSTAT register mapping is shown in Figure 9.

Optionally, the user can also complete a course verification of the satellite oscillators as shown.

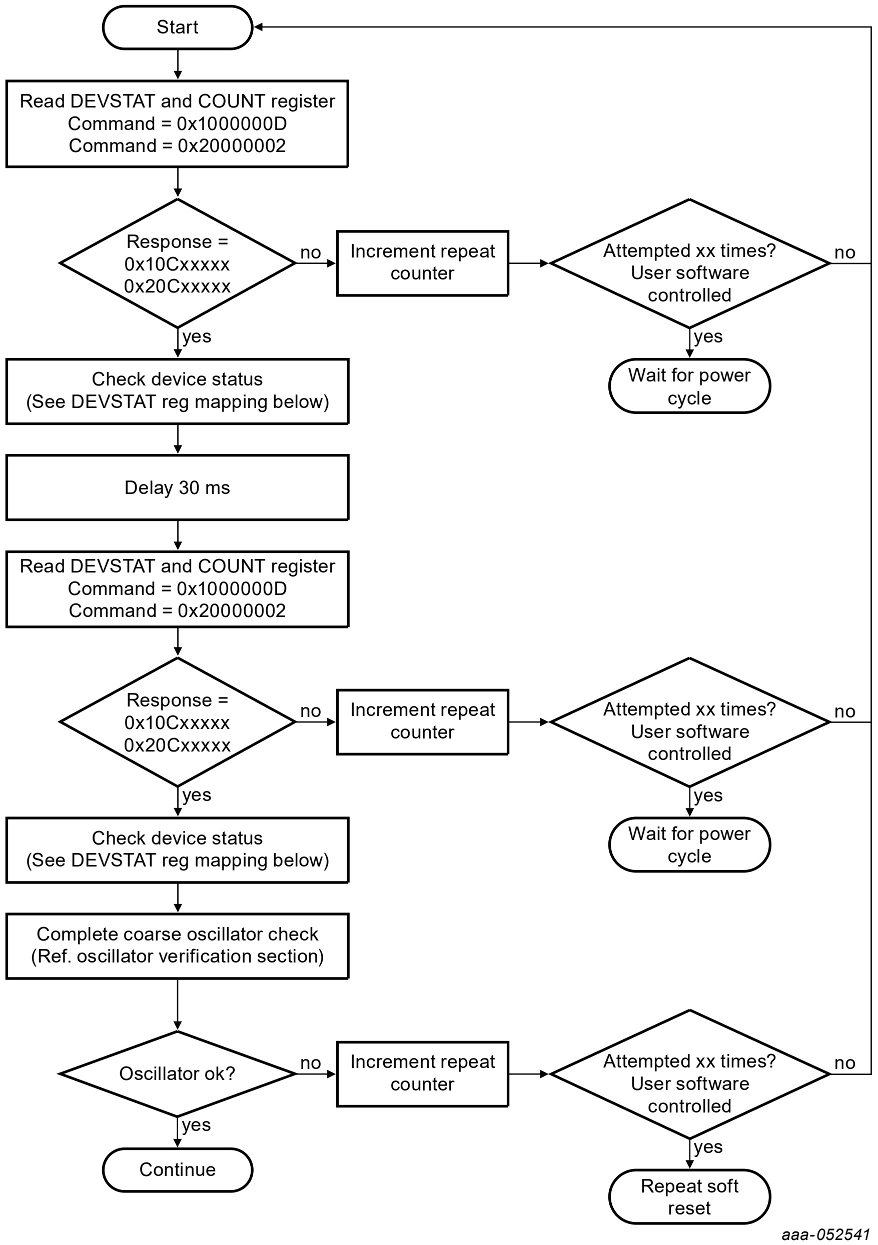


Figure 8. Confirm device status

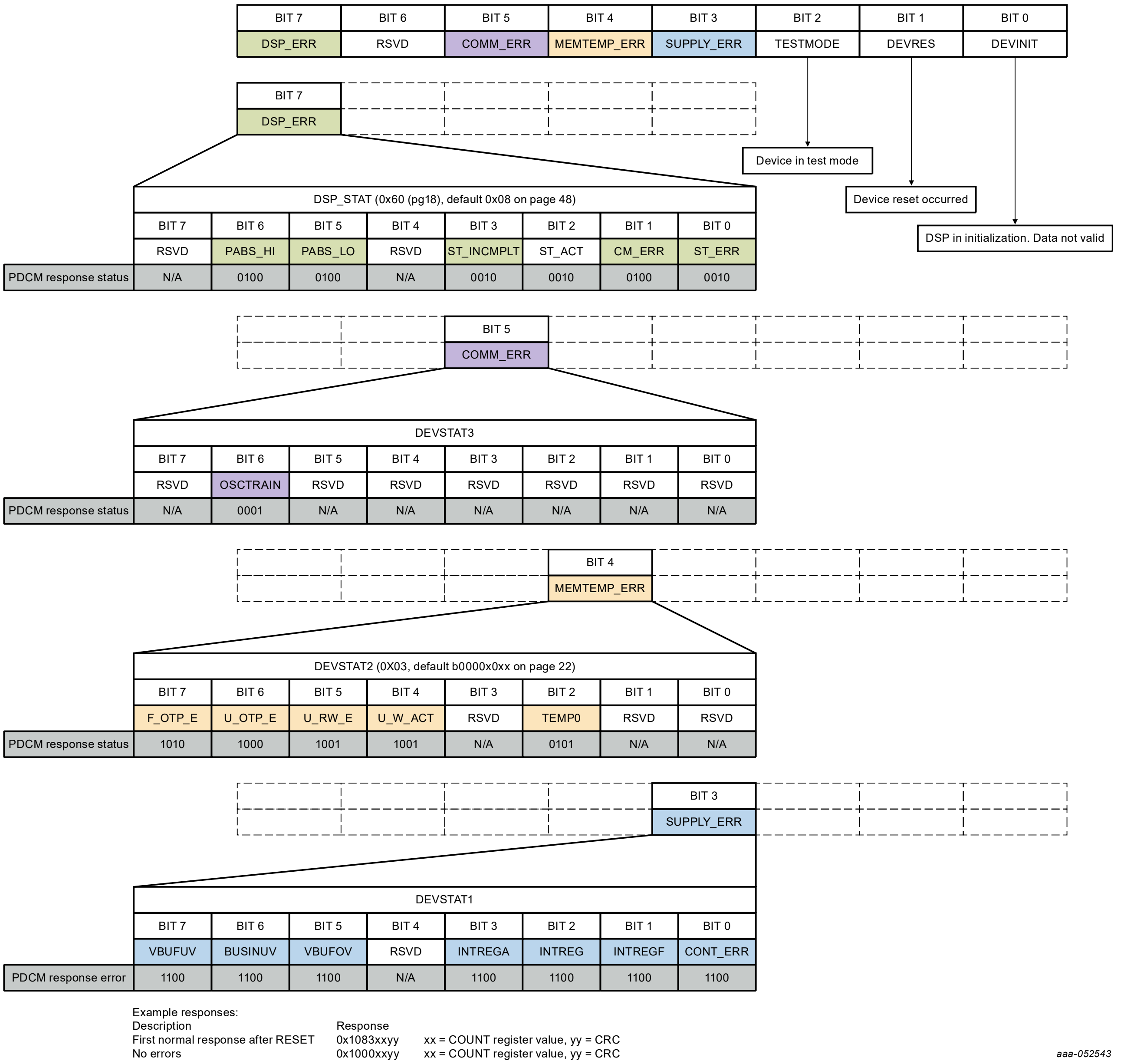


Figure 9. DEVSTAT register mapping

Note: *Figure 9 shows more status details, which are user optional.*

6.2 Optional complete register pattern write verification

The next step is to complete a register pattern write verification. This step is optional and not required to meet the diagnostic coverage as documented in the failure modes, effects, and diagnostic analysis (FMEDA).

The recommended procedure for register pattern write verification is shown in Figure 10. In this example, the PDCM_RSPST0_L register is used for pattern writing. Other registers can be used as long as the function for the register written to is considered.

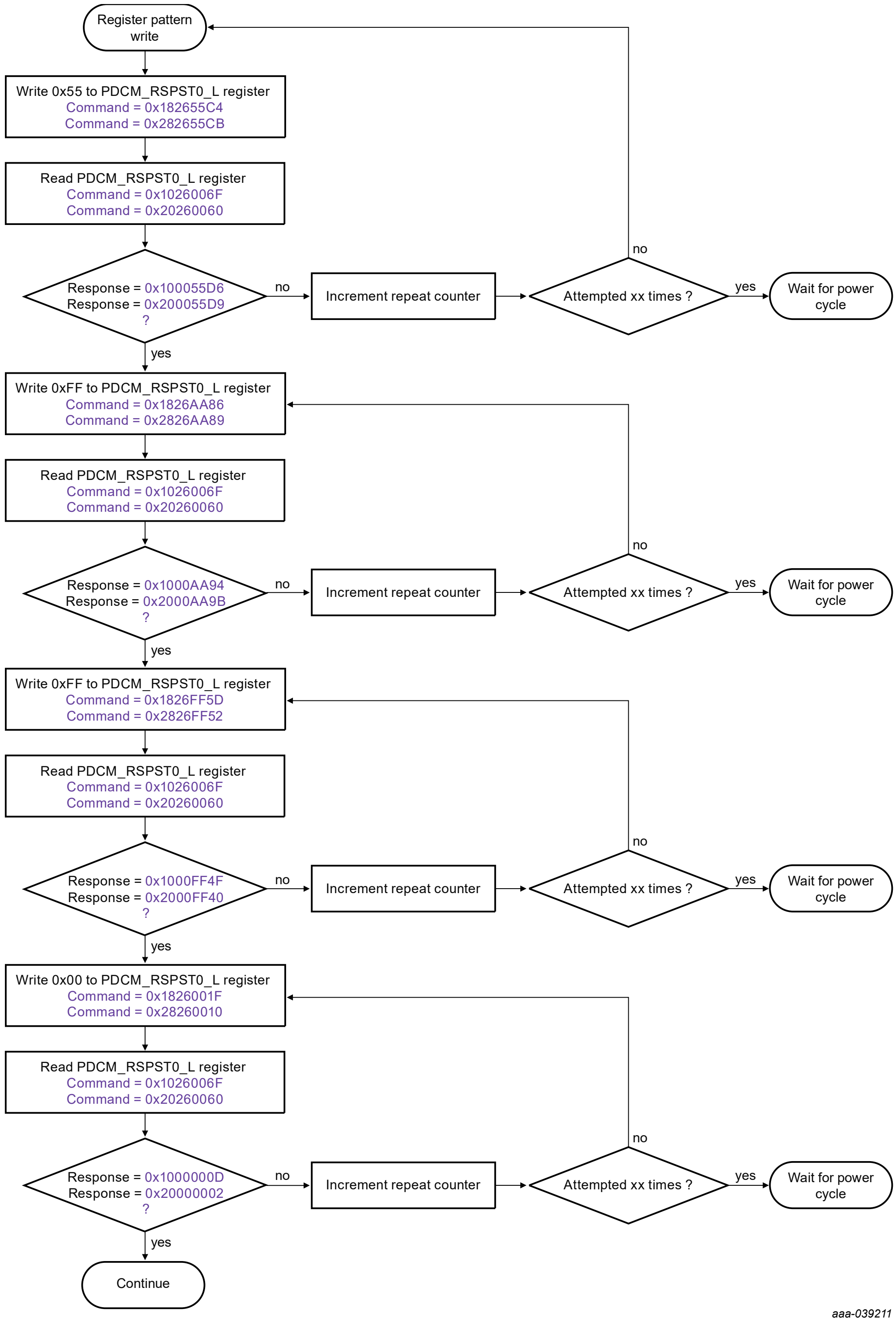


Figure 10. Complete register pattern write verification

6.3 Configure the data sources

The next step is to configure the devices for the desired data sources (that is relative pressure) and source identifiers for PDCM.

Figure 11 shows an example configuration for a 2 satellite bus with one data source for each satellite. Set the keep alive counter (KAC) to 2 with status of 4 and 10 bit data.

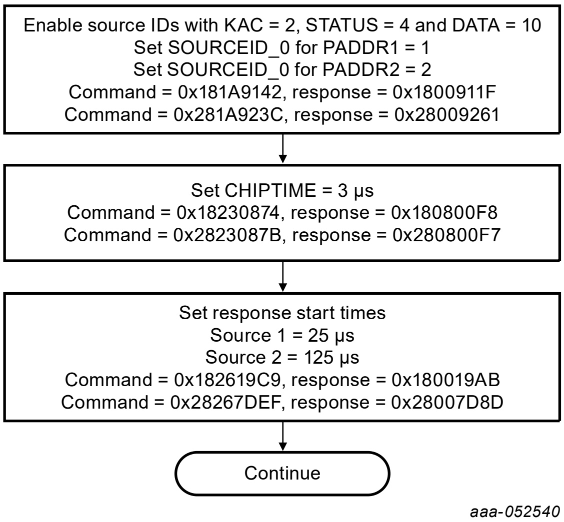


Figure 11. Configure the data sources

The FXPS7140X device has the capability for two independently configurable data sources. Figure 12 shows a pictorial mapping of the sources to their source identifiers and associated data.

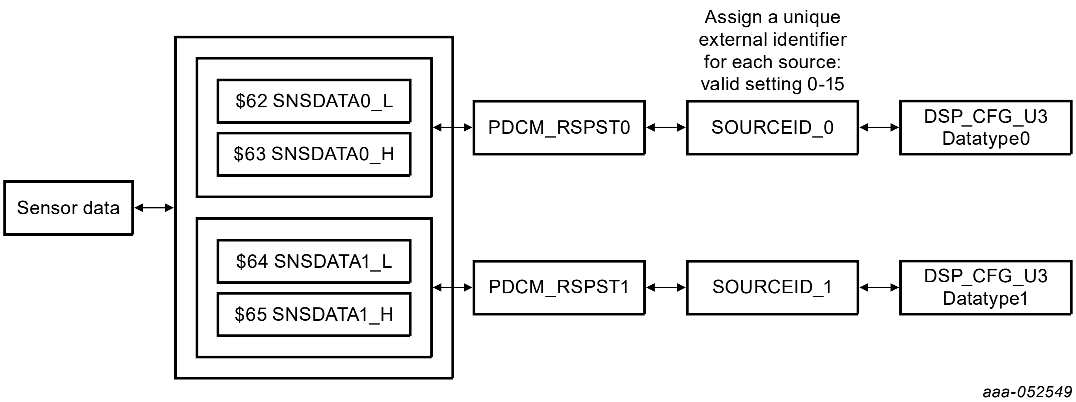


Figure 12. Data source mapping diagram

The sources are enabled and the associated source identifiers are set using the registers listed in the following table.

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Register address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
$1A	SOURCEID_0	SID0_EN enable source 0, datatype 0 (relative pressure)	PDCM_FORMAT[2:0] = 1 In this application note, the PDCM format is set to a 28-bit length: • D[27:24] = source ID • D[23:22] = source counter • D[21:18] = 4-bit device status • D[17:8] = 10-bit sensor data • D[7:0] = cyclic redundancy check (CRC)			SOURCEID_0[3:0] system level source identifier for datatype 0 ***Note:*** *Each source identifier value for the device must be unique or the device transmits error messages for the repeated identifier.*			
$1B	SOURCEID_1	SID1_EN enable source 1, datatype 1 (absolute pressure P_{ABS})	reserved	reserved	reserved	SOURCEID_1[3:0] system level source identifier for datatype 1 ***Note:*** *Each source identifier value for the device must be unique or the device transmits error messages for the repeated identifier.*			

6.4 Configure the sensor signal chain

The next step is to configure the sensor signal chain. Figure 13 shows an example configuration setting of the low-pass filter (LPF), pressure range C with data type to relative pressure.

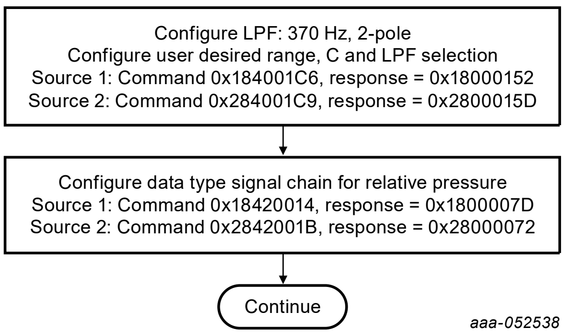

Figure 13. Configure the sensor signal chain

6.4.1 Signal chain low-pass filter selection

The signal chain low-pass filter is selected by a combination of the LPF bits to the desired filter type in the DSP_CFG_U1 register as shown in the product data sheet. The LPF selection table is shown in Table 3.

Table 3. Signal chain low-pass filter selection

LPF[3]	LPF[2]	LPF[1]	LPF[0]	Low-pass filter type
0	0	0	0	370 Hz, 2-pole
0	0	0	1	400 Hz, 3-pole
0	0	1	0	1000 Hz, 4-pole
0	0	1	1	800 Hz, 4-pole

Table 3. Signal chain low-pass filter selection...*continued*

LPF[3]	LPF[2]	LPF[1]	LPF[0]	Low-pass filter type
0	1	0	0	reserved
0	1	0	1	reserved
0	1	1	0	reserved
0	1	1	1	reserved
1	X	X	X	reserved

6.4.2 Absolute pressure range selection

The signal chain pressure range settings are shown in Table 4.

Table 4. Pressure range selection

USER_RANGE[1:0]		Absolute pressure range
0	0	range B[1]
0	1	range C[1]
1	0	reserved
1	1	reserved

[1] Part number dependent.

6.4.3 Signal chain data type configuration

Each source enabled (as described in Section 6.3 "Configure the data sources") must have its data type configured. Data type configuration is described in the product data sheet and shown in Table 5.

Table 5. Signal chain data type selection

DATATYPEx[1:0]		DSI3 sensor data description
0	0	relative pressure data
0	1	absolute pressure (P_{ABS}) data
1	0	filtered absolute pressure (P0) data
1	1	temperature data

6.5 Confirm device traceability information

The next step is to confirm the device level traceability information. To confirm that the proper device is connected read the IC type, IC manufacturer ID, IC part number, and IC serial number.

Note: *Responses to the read commands in Figure 14 are representative only and actual responses differ on a per device basis.*

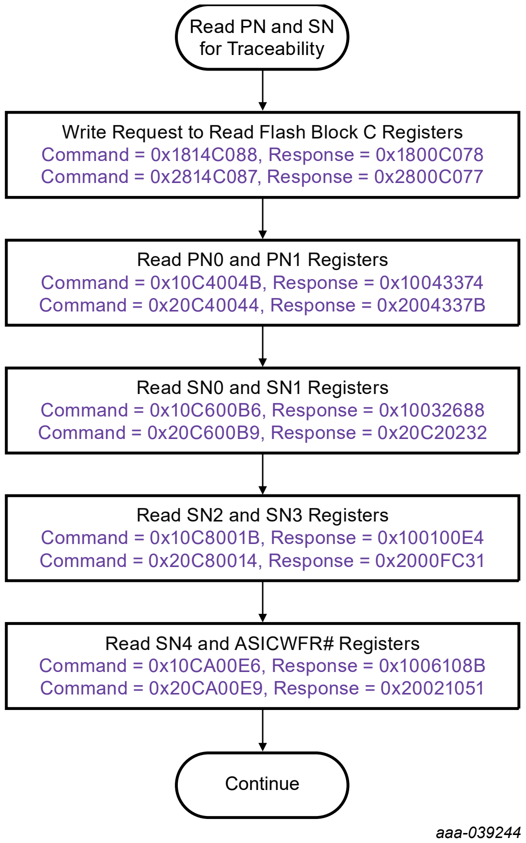

Figure 14. Confirm device traceability information

6.6 Complete self-test (self-test overview)

The next step is to complete some or all self-test functions available in the device. Figure 15 shows an overview of a procedure for completing a self-test. Test repeats on failure are not shown in the diagrams. The user determines the number of test repeats for each test type based on the application. Typically test repeats are included at a minimum for the analog self-test procedures to provide immunity to potential misuse inputs that are common during startup.

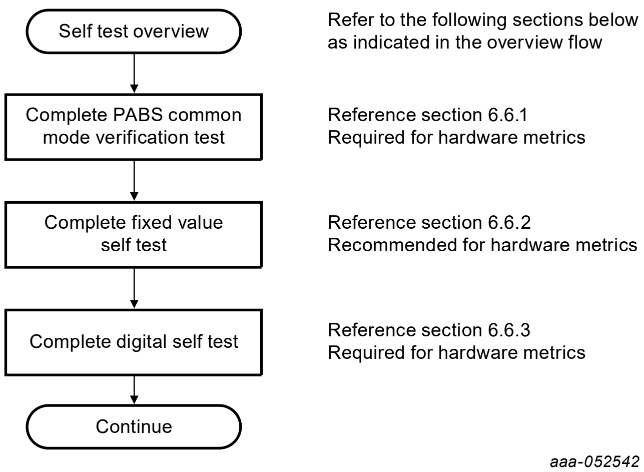

Figure 15. Self-test overview

6.6.1 Complete P_{ABS} common mode self-test

The next step is to complete a P_{ABS} common mode self-test verification for each device. When the P_{ABS} common mode self-test is selected, the ST_ACTIVE bit is set, the ST_ERROR is cleared, and the device begins an internal measurement of the common mode signal of the P-cells and compares the result against a predetermined limit. If the result exceeds the limit, the ST_ERROR bit is set.

The P_{ABS} common mode self-test repeats continuously every t_{ST_INIT} when the ST_CTRL bits are set to the specified value. Once the test is disabled, the ST_ERROR bit is updated with the final test result within t_{ST_INIT} of disabling the test. The ST_ACTIVE bit remains set until the final test result is reported. Figure 16 is an example of a user-controlled self-test procedure.

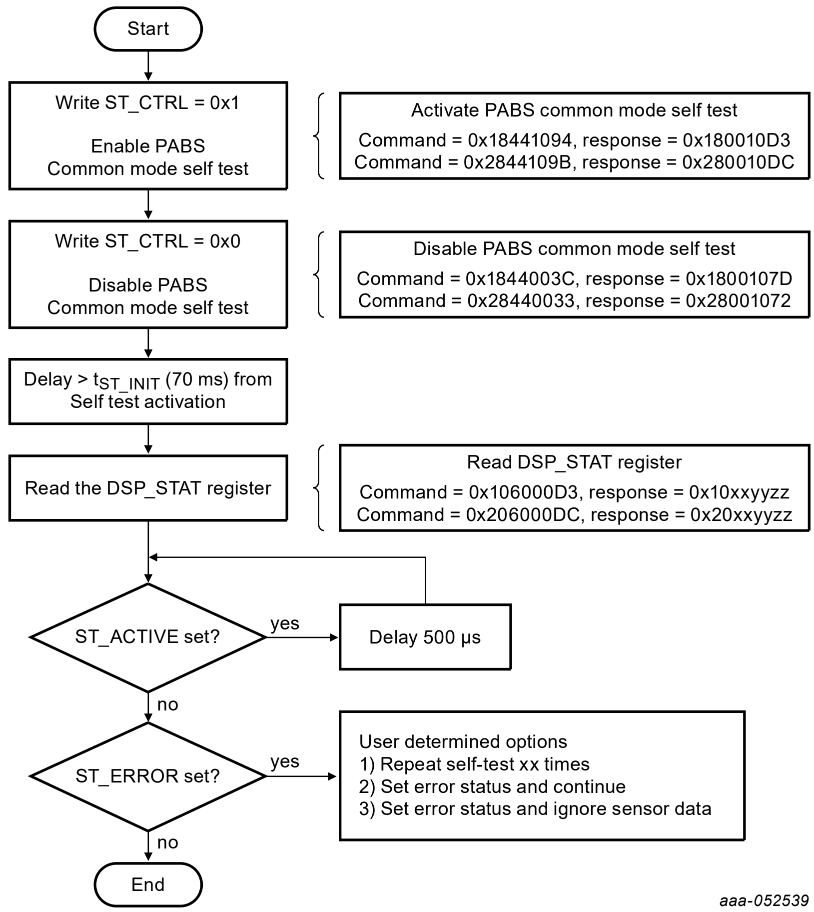

Figure 16. Complete P_{ABS} common mode self-test

6.6.2 Complete fixed value self-test

The next step is to complete a fixed value self-test verification for each device. The purpose of the fixed value self-test is to confirm that the output data register and communication block have no stuck bit conditions. Figure 17 shows an example procedure for completing a self-test with 2 fixed values. The example alternates 0x5555 and 0xAAAA to confirm both states of each bit in the data field and to maximize verification of sensor data. Expected responses are included for each self-test request.

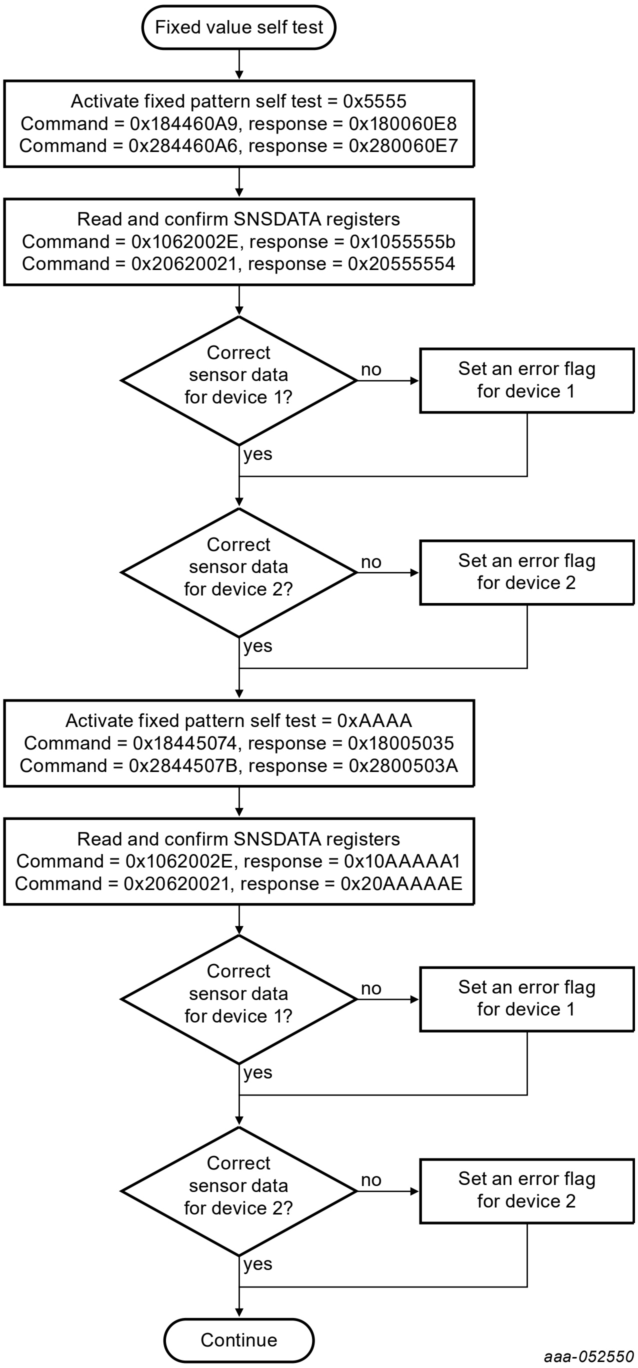

Figure 17. Complete fixed value self-test

6.6.3 Complete digital self-test

The next step is to complete a digital self-test verification for each device. The purpose of the digital self-test is to complete a more accurate verification of the digital signal chain. The digital self-test forces a known value into the input of the digital signal chain. After a defined time interval, dependent on the low-pass filter selected, the signal chain output can be verified against an expected value. The digital self-test values listed from the product data sheet are provided in Section 6.6.3.1 "Digital self-test limit calculation".

Figure 18 shows an example flow procedure for completing a self-test of one digital value (digital self-test 0xF), confirming the expected output value and finally reconfiguring the devices datatype to relative pressure and checking the status before entering PDCM.

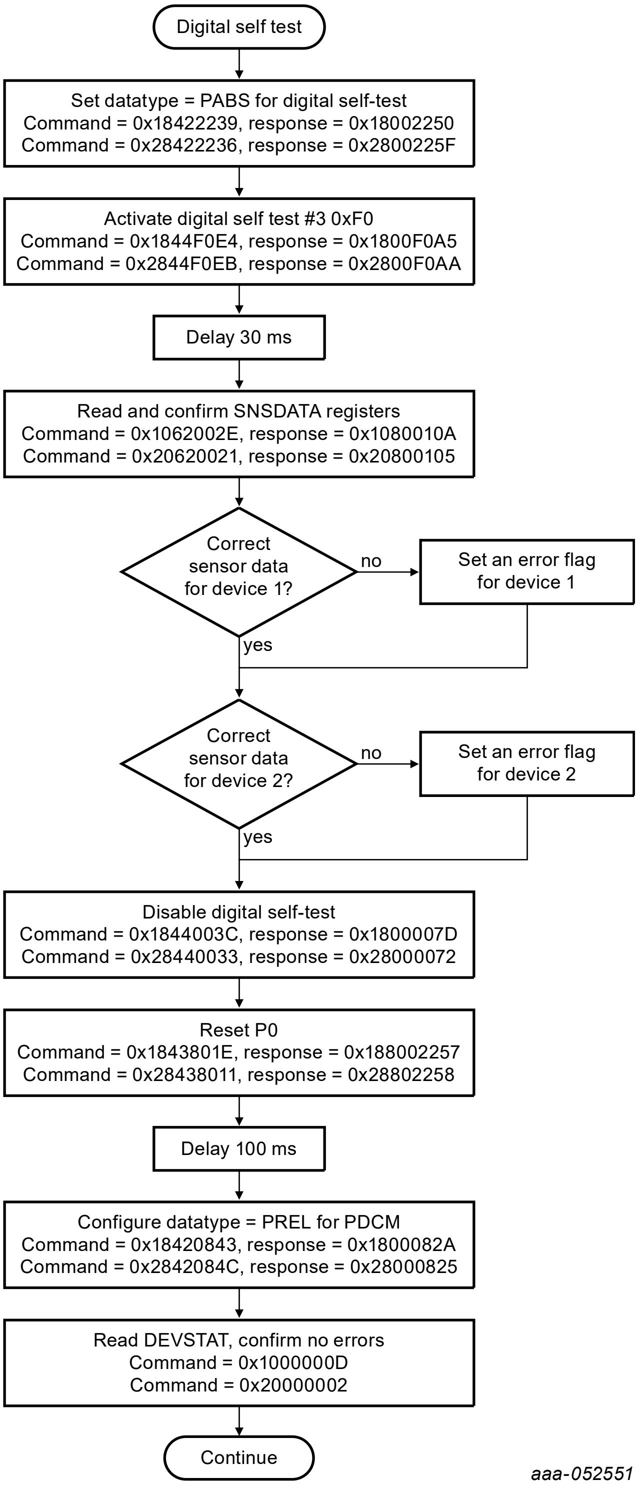

Figure 18. Complete digital self-test

6.6.3.1 Digital self-test limit calculation

The digital self-test provides a constant value to the sensor data output. The values listed in Table 6 are only valid if the absolute pressure (P_{ABS}) signal is selected by the associated DATATYPEx bits. When any of these self-test functions are selected, the ST_ACTIVE bit is set.

Table 6. Data sheet digital self-test values

Self-test ST_CTRL[3:0]	Function	SNS_DATAx register contents	
		Range B	Range C
		Absolute pressure	Absolute pressure
0xC	digital self-test #1	0x8171	0x8171
0xD	digital self-test #2	0x6C95	0x6C95
0xE	digital self-test #3	0x807A	0x807A
0xF	digital self-test #4	0x78AC	0x78AC

6.7 Transition to periodic data collection mode (PDCM)

Once all self-test procedures are completed and verified, the system can transition the device from CRM to PDCM. This can be done by two methods:

1. Send a CRM command to each device setting the ENDINIT bit.
2. Send the global Enter PDCM command.

The example in this application note uses the global Enter PDCM command. For the CRM, a single command packet is followed by at most one response packet. There is no response packet for a global command.

Figure 19 shows the global command to enter PDCM and the normal PDCM sequence.

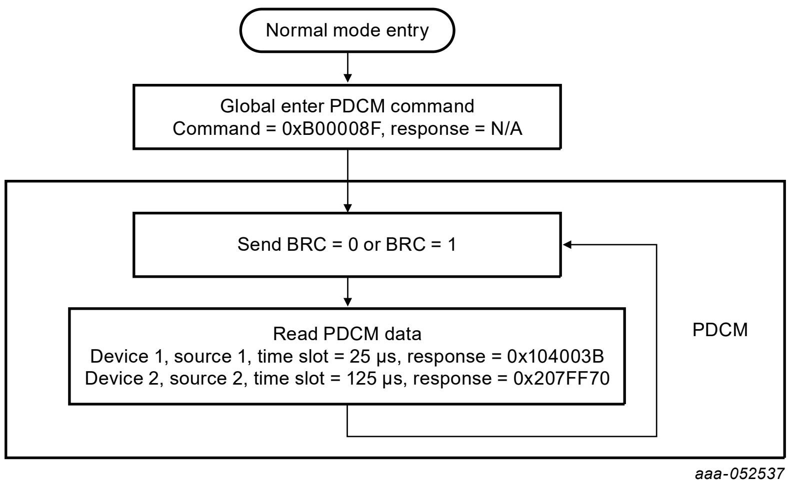

Figure 19. Transition to PDCM

7 Optional user diagnostics

This section describes some additional system-level diagnostics that are recommended to improve the safety performance of the device in its intended application. These diagnostics are not inherent in the device and, if used, must be conducted externally.

7.1 Startup configuration register verification

Before entering PDCM, all registers that impact the communication or signal chain configuration can be read to confirm the expected values. This is not necessary if the response to all register write command is verified for the correct values. The response to a register write does read back the register value before transmission and is equivalent to a register read.

8 Summary and conclusion

This application note describes the recommended procedures for initializing and configuring FXPS7140X devices on a DSI3 bus, completing self-test on the devices and finally, transitioning the devices to normal mode. These recommended procedures are important to meet the functional safety requirements of the intended system.

9 Further assistance

For further assistance, contact your local sales representative.

10 Abbreviations and definitions

Table 7. Abbreviations and definitions

Term	Definition
BRC	broadcast read command; the broadcast read command is a single bit command enabling the time division multiple access (TDMA) satellite transmissions in periodic data collection mode (PDCM)
CRM	DSI3 command and response mode; a bidirectional communication method enabling communication between a single controller and a single satellite or multiple satellites; this mode is optimized for programming and control of satellite devices and is primarily used for register reads and writes with the FXPS7140X devices
Digital self-test	A method to test the digital portion of the signal chain by forcing a value or a sequence of values at the output of the analog-to-digital converter and measuring the device output.
Discovery mode	DSI3 Discovery mode; an automatic addressing scheme to provide physical addressing by location to a single controller, multiple-satellite bus
DSI3	distributed system interface, third generation; a single controller, multiple-satellite communication interface that provides both satellite power and communication on a 2-wire bus
DSP	digital signal processor
PDCM	DSI3 periodic data collection mode; a bidirectional communication method enabling communication between a single controller and a single satellite or multiple satellites; this mode is optimized for high-speed sensor data transfers from multiple satellites to a single controller; satellite responses are time division multiplexed; this mode is used for periodic relative pressure data transfers on the FXPS7140X device
POR	power-on reset
PSI5	peripheral sensor interface, fifth generation; a single controller, multiple-satellite communication interface that provides both satellite power and communication on a 2-wire bus

11 References

[1] FXPS7140X product data sheet, latest revision: PSAT data sheet

[2] DSI3 Standard, Revision 1.0, February 16, 2011

[3] PSI5 Technical Specification Version 2.1, October 8, 2012

12 Revision history

Table 8. Revision history

Document ID	Release date	Description
AN14033 v.1	5 December 2023	initial version

13 Appendix

13.1 DSI3 state transition diagram

Figure 20 shows a state transition diagram for the internal DSI3 controller.

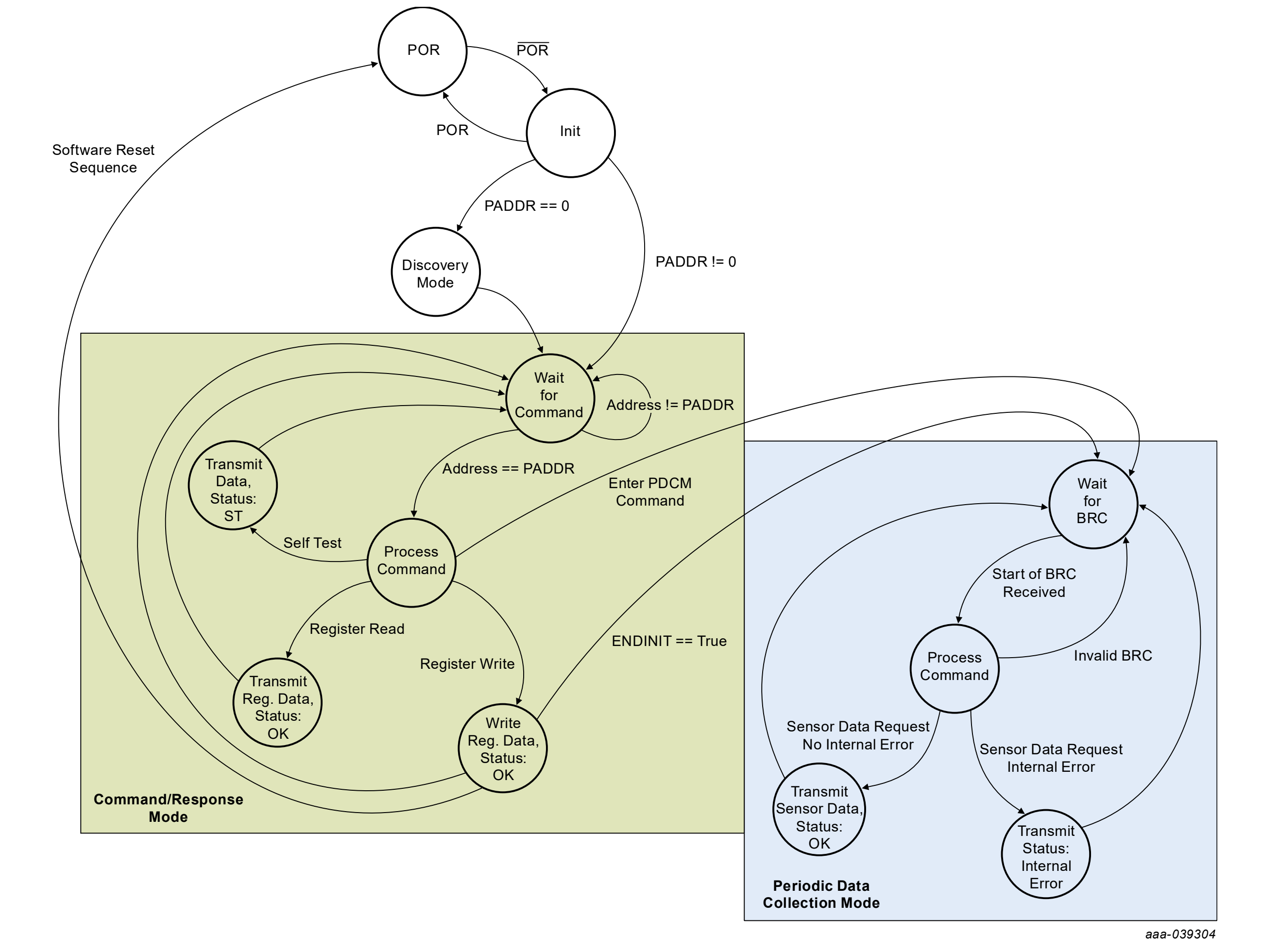

Figure 20. DSI3 state transition diagram

13.2 CRC calculation example: 8-bit CRC

The codeblock below shows some example visual basic to calculate the DSI3 8-bit CRC.

- Function DSICRMCRC(Data32 As String, Poly As String, SEED As String) As String
  - Data32 is the 24-bit message in binary to be verified with 8 zeros appended in place of the CRC
    Example: Command = 0x0106200xx: Data32 = 0001 0000 0110 0010 0000 0000 0000 0000
  - Poly is the 9-bit CRC polynomial in binary
    Example: Polynomial = $X^8 + X^5 + X^3 + X^2 + X + 1$ Poly = 1 0010 1111
  - SEED is the 8-bit CRC initial value in binary
    Example: SEED = 0xFF SEED = 1111 1111

In this example, the CRC = 0x2E

```
Function DSICRMCRC(Data32 As String, Poly As String, SEED As String) As String
Dim i As Integer
Dim m As Integer
Dim n As Integer
Dim k As Integer
Dim bit As Integer
i = 1
m = 1
n = 1
k = 1
bit = 0
Dim CRC(1 To 8) As String
Dim CRC_old(1 To 8) As String
For i = 1 To 8
    CRC(i) = Mid(SEED, i, 1)
    CRC_old(I) = Mid(SEED, i, 1)
Next i

For n = 1 To 32
    bit = Mid(Data32, n, 1)
    For k = 1 To 8
        CRC_old(k) = CRC(k)
    Next k
    For m = 1 To 8
        If Mid(Poly, m + 1, 1) = 0 Then
            If m = 8 Then
                CRC(m) = bit
            Else
                CRC(m) = CRC_old(m + 1)
            End If
        Else
            If m = 8 Then
                If CRC_old(1) = 1 Then
                    If bit = 1 Then
                        CRC(m) = 0
                    Else
                        CRC(m) = 1
                    End If
                Else
                    If bit = 1 Then
                        CRC(m) = 1
                    Else
                        CRC(m) = 0
                    End If
                End If
            Else
                If CRC_old(1) = 1 Then
                    If CRC_old(m + 1) = 1 Then
                        CRC(m) = 0
                    Else
                        CRC(m) = 1
                    End If
                Else
                    If CRC_old(m + 1) = 1 Then
                        CRC(m) = 1
                    Else
                        CRC(m) = 0
                    End If
                End If
            End If
        End If
    Next m
Next n
DSICRMCRC = CRC(1) & CRC(2) & CRC(3) & CRC(4) & CRC(5) & CRC(6) & CRC(7) & CRC(8)
End Function
```

Legal information

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Tables

Figures

Contents

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