AN13714

LPC553x/LPC55S3x High-Speed Comparator - Evaluation of Advanced Features

Rev. 1 — 25 September 2023 Application note

Document Information

Information	Content
Keywords	HSCMP, Window mode, Sample mode
Abstract	This application note describes the advanced comparator features, such as Window mode and Sample mode

1 Introduction

This application note describes the advanced comparator features of LPC55S3x devices. It presents possibilities how to set-up and evaluate High-Speed Comparator (HSCMP) for real-time control applications. For basic HSCMP features, see *LPC553x/LPC55S3x High-Speed Comparator - Evaluation of Basic Features* (document AN13540).

This document lists instruction for people who want to discover internal peripheral interconnection possibilities and use cases of HSCMP with other peripheral modules, especially timers or Pulse Width Modulation (PWM) module. Going through this manual can save you time and effort.

Note: *This application note has an associated software package with an example for NXP MCUXpresso IDE. FreeMASTER real-time debugger is used for application control.*

1.1 Introduction to HSCMP

The HSCMP module provides a circuit for comparing two analog input voltages. It comprises a Comparator (CMP), 8-bit Digital to Analog Converter (DAC), and an analog mux for each CMP input.

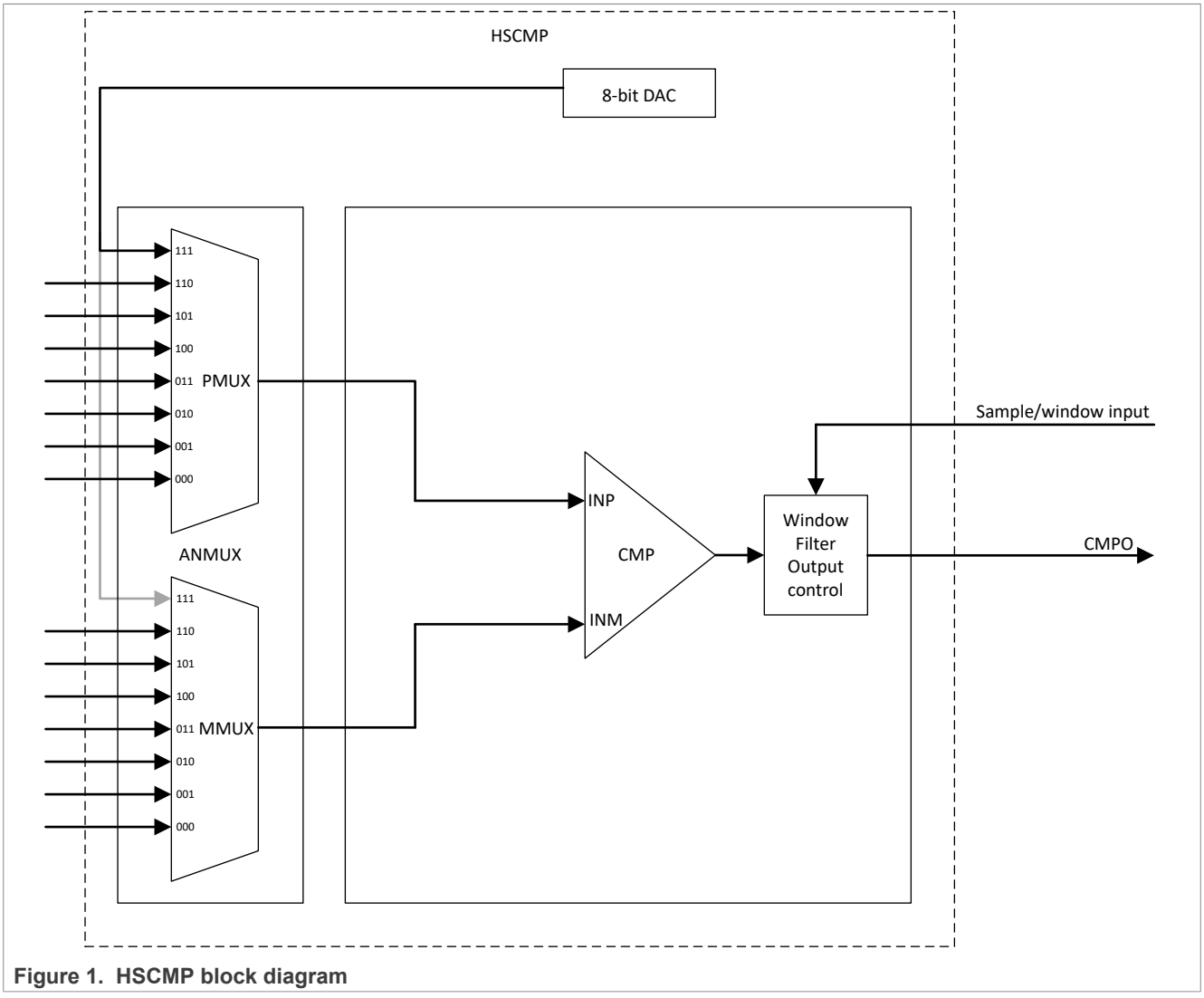

Figure 1. HSCMP block diagram

The CMP can operate across the full range of the supply voltage, known as rail-to-rail operation. DAC is a 256-tap resistor ladder network that provides a selectable voltage reference for applications requiring a voltage reference. The 256-tap resistor ladder network divides the supply reference, Vin, into 256 voltage levels. An 8-bit digital signal input selects the output voltage level, which varies from Vin to Vin/256. Vin can be selected from two voltage sources, vrefh0 and vrefh1. The HSCMP's internal DAC output is available as an on-chip internal signal only. Internal 8-bit DAC is connected to both input muxes. It is also possible to connect 12-bit DAC, which is available on specific input channels, see Table 1 for more details.

1.2 HSCMP features

The feature of the HSCMP module includes the following:

- Two muxes to select input signal from eight channels.
- Multiple operation modes to produce a wide range of outputs, such as:
  - Sampled.
  - Windowed, which is ideal for specific PWM zero-crossing-detection applications.
  - Digitally filtered.
- Advanced feature for window and sample:
  - Window / Sample signal can be inverted.
  - Window can be closed by `COUT` rising, falling, or both edges.
  - User can define `COUT` level, when window is closed.
- Selectable performance levels: Nano-power mode, Low-power (speed) mode, and, High-power (speed) mode.
- Programmable hysteresis control.
- Selectable inversion on comparator output.
- External hysteresis can be used at the same time that the output filter is used for internal functions.
- Interrupt and DMA support.
- Trigger mode.
- Includes an 8-bit resolution DAC.
- Selectable supply reference source for DAC.
- Configurable Low-power mode or High-power mode for DAC.

HSCMP is intended for real-time control of applications and use cases, such as overcurrent detection. There is possible to propagate HW compare event to disable the PWM so HSCMP act as HW overcurrent protection. It could be used for level-crossing detection of signals for synchronization of various applications, such as power converters. HSCMP compare event is also capable to restart PWM module and send compare event to various peripherals.

2 Pin configuration

Pin configuration is done in the MCUXpresso pin tool. For more details, see "I/O Pin Configuration (IOCON)" chapter of *LPC553x Reference Manual* (document LPC553xRM).

Table 1 summarize all the HSCMP pins on LPC55S3x and their availability on HSCMP input mux.
Inputs and indexes are identical for both positive and negative mux, registers `HSCMP_CCR2_MSEL` and `HSCMP_CCR2_PSEL`.

Table 1. HSCMP inputs

Input mux index	HSCMP0	HSCMP1	HSCMP2
0	HSCMP0_IN0 PIO0_24	HSCMP1_IN0 PIO0_7	HSCMP2_IN0 PIO0_17
1	HSCMP0_IN1 PIO1_12	HSCMP1_IN1 DAC0_OUT PIO1_22	HSCMP2_IN1 PIO1_23

Table 1. HSCMP inputs*...continued*

Input mux index	HSCMP0	HSCMP1	HSCMP2
2	Unconnected	Unconnected	Unconnected
3	HSCMP0_IN3 PIO1_5	HSCMP1_IN3 PIO1_10	Unconnected
4	HSCMP0_IN4 OPAMP0_OUT PIO1_9	OPAMP1_OUT	OPAMP2_OUT
5	DAC0_OUT PIO1_22	HSCMP1_IN5 DAC1_OUT PIO1_19	DAC2_OUT
6	Reserved	Reserved	Reserved
7	HSCMP0 internal DAC	HSCMP1 internal DAC	HSCMP2 internal DAC

3 Operational modes

This application note is focused on advanced operational modes of HSCMP, such as Window mode and Sample mode. Operational modes must utilize additional peripheral modules as a window / sample event source. HSCMP has dedicated `INPUTMUX` for this signal/event. For more details, see chapter "Input Multiplexing (INPUTMUX)" and sub-chapter "Input connections for HSCMP0 (HSCMP0_TRIG)" of *LPC553x Reference Manual* (document LPC553xRM).

3.1 Sample mode

Enable the Operational mode:

1. Set Sample mode bit in `CCR1` register.
2. Set filter sample count `FILT_CNT` to 1.

It is necessary to utilize external sources, such as a timer, to define sample events. For this example, the `CTIMER0` module is used with the event match 3.

Sample event means the rising edge of the source signal. Figure 2 shows the scheme of the presented Sample mode example.

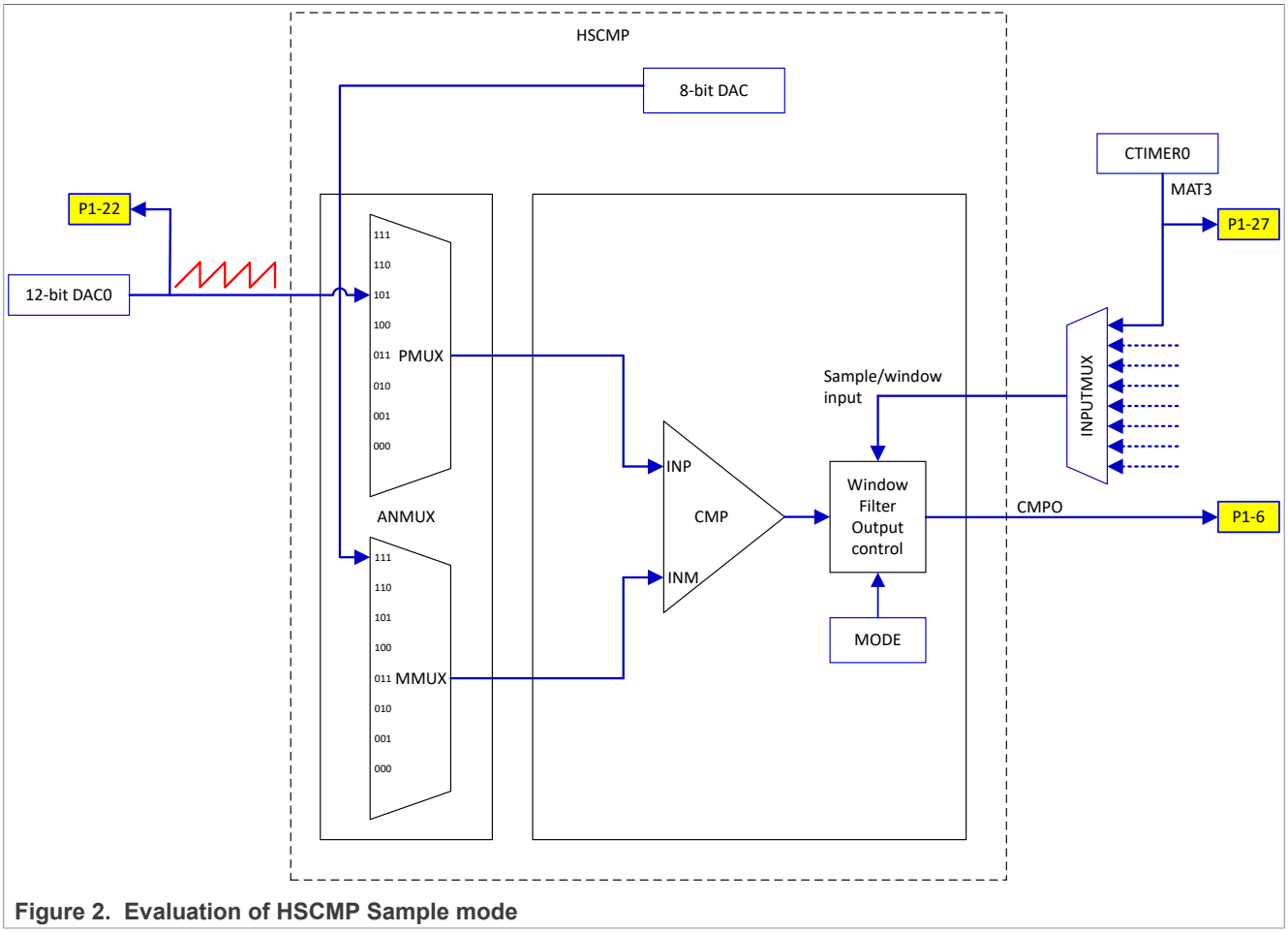

Figure 2. Evaluation of HSCMP Sample mode

In practice, the comparator is still continuously working, but the comparator output value is sampled and sent to HSCMP main output when the sample event occurs. Both DACs simulate signals for comparison:

- HSCMP 8-bit internal DAC creates the reference threshold level.
- 12-bit DAC and a simple periodic software routine create the saw wave signal.

To evaluate the example, connect the scope probes on EVK to observe and understand the operation.

Note: *GND is available on the multiple positions of EVK.*

See Table 2 for the predefined available signals on connectors.

Table 2. EVK signals for scope

EVK connector	Signal	Description
J10-11	HSCMP0 OUT	Comparator output
J92-2	CTIMER0 MAT3	CTimer match3 output
J10-9	DAC0 OUT	12-bit DAC output

Figure 3 shows the default example:

- Blue line is the 12-bit DAC output.
- Green line is the CTIMER output that is the source for the sample event input of HSCMP.
- Red line is the HSCMP output.

- The HSCMP internal 8-bit DAC is not available on the MCU pin, but in the example, it is used as a reference level for comparison with the 12-bit DAC.
- In default, 8-bit reference is set to the middle of the range so the internal compare event is in the middle of the Blue line.
- Sample event is the rising edge of CTIMER signal, shown as Green line.

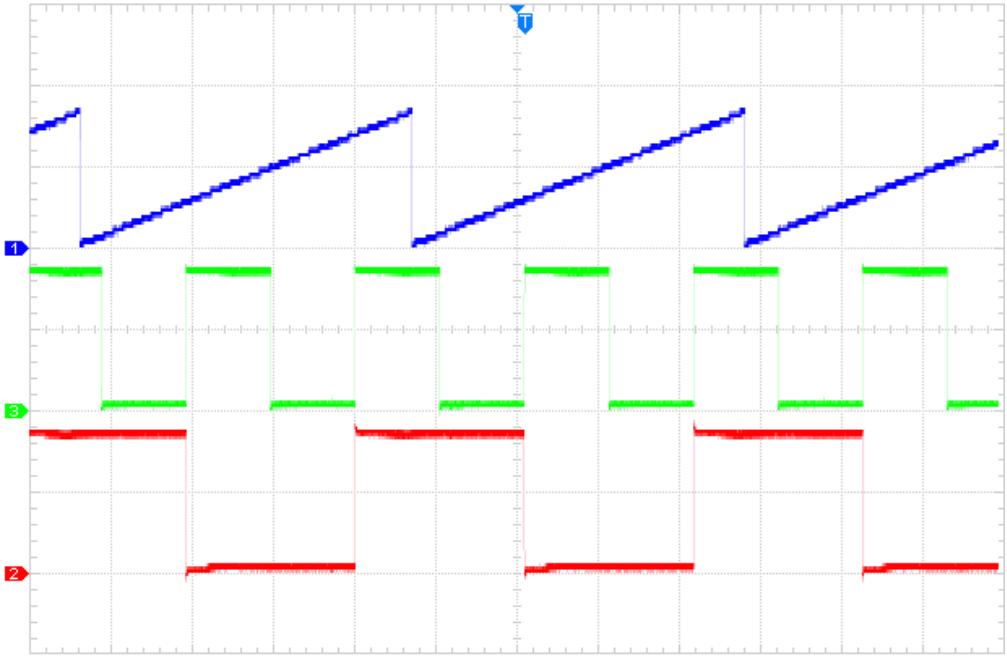

Figure 3. Sample mode waveforms

3.2 Window mode

Enable the Window mode:

1. Set Window mode bit in CCR1 register.
2. Set filter sample count FILT_CNT to 0.

It is necessary to utilize some external source, such as a timer, to define the window area. For this example, the CTIMER0 module is used with the event match 3. The drawback of this window implementation is that if some analog compare event occurs before the Window and is still valid in the window area, then it is taken as an event linked with the beginning of the window. The scheme of the Window mode is practically identical to the Sample mode, except for the setup of the window function in HSCMP registers.

Figure 4 shows the default example waveform:

- Window is active when CTIMER green signal is high.
- Internal signal state is copied to HSCMP output.
- Window polarity could be inverted by WINDOW_INV bit in CCR1.
- Comparator output could be inverted by COUT_INV bit.

The window could be closed by COUT if there is the enabled WINDOW_CLS bit where EVT_SEL defines an event (rising, falling, both edges) for closing the window.

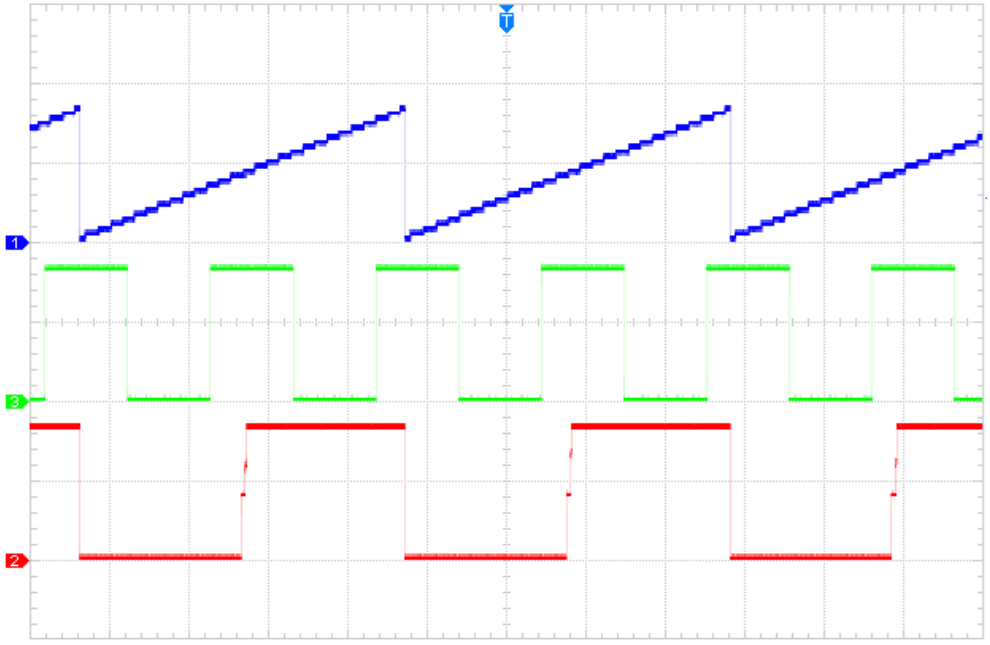

Figure 4. Window mode waveform

3.3 Enhanced Window mode

To enable this operation, the HSCMP runs in Continuous mode. Optionally it is useful to enable HSCMP internal filter to ignore short compare events.

It is necessary to utilize external sources, such as a timer, to create a short pulse from the rising edge of HSCMP output; for debug purposes, this pulse width is longer for better observation of scope. For this purpose CTIMER0 module is used, match 3 in PWM mode. The drawback of the default window implementation described in Section 3.2 is fixed in this implementation. If some analog compare event occurs out of the window, it is not acknowledged. Figure 5 show the diagram of the presented enhanced Window mode example.

The window function is done outside of HSCMP in And-Or-Invert (AOI) module.

- Submodule 0 is used as the PWM out.
- Submodule 1 PWM is used as the window signal.

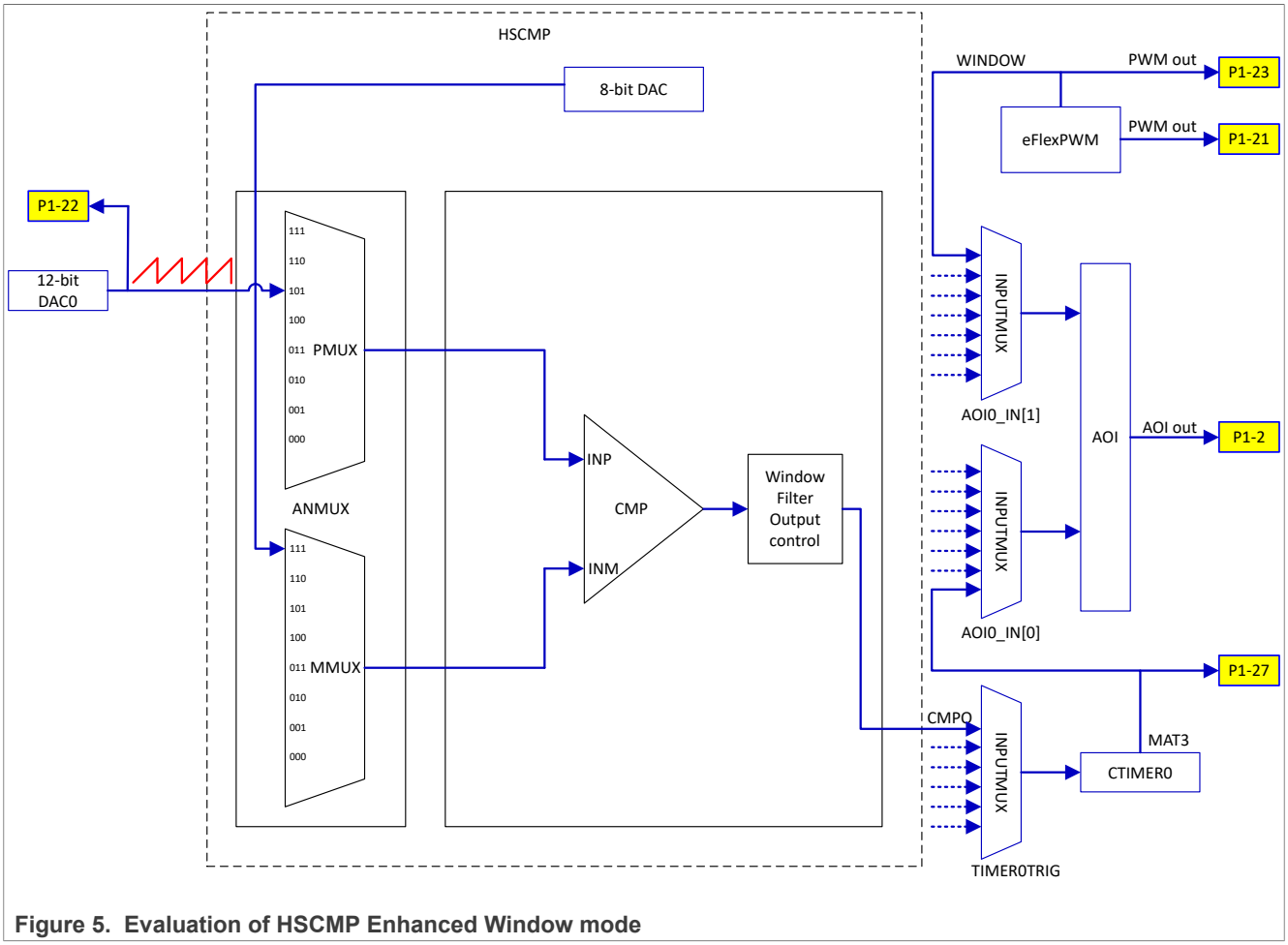

Figure 5. Evaluation of HSCMP Enhanced Window mode

4 Evaluation software

This example uses compared simulated values by DACs without needing any additional HW connection on EVK. MCUXpresso, LPC553x/LPC55S3x SDK package, and the FreeMASTER tool must be installed. Signals are available on EVK headers. For more details please see EVK schematic and users guide.

To run the SDK HSCMP example, perform the following steps:

1. Unzip the examples to your local machine.
2. Import the example into the MCUXpresso IDE.
3. Build the example.
4. Flash the example.
5. Start the FreeMASTER HSCMP project.
6. Click "Run".
7. Set the variables (for example, threshold value or Window) in the runtime using the FreeMASTER real-time debugger. The result can be monitored using an oscilloscope.

5 Revision history

Table 3 summarizes the changes done to this document.

Table 3. Revision history

Revision number	Release date	Description
1	25 September 2023	Updated software examples and description. Diagram corrections.
0	2 December 2022	Initial release

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