AN13453

Card coil design notes for MIFARE Ultralight AES

Rev. 1.2 — 20 April 2022

Application note
COMPANY PUBLIC

Document information

Information	Content
Keywords	Contactless, MIFARE Ultralight AES, ISO/IEC 14443, Resonance, Frequency, Coil, Inlay
Abstract	This document provides guidance for engineers designing loop antenna coils for MIFARE Ultralight AES.

Revision history

Revision history

Rev	Date	Description
1.2	20220420	Corrected typos, editorial changes, removed unnecessary figure
1.1	20220218	Security status changed to "Company public"
1.0	20220208	Initial version

1 Introduction

MIFARE Ultralight AES (later called PICC, Proximity Integrated Circuit Card), a passive device (without battery) is powered by magnetic field generated by a PCD (Proximity Coupling Device). To get the magnetic flux cut by the PICC, it also requires a loop antenna. A PICC with connected coil antenna is also called transponder.

This document describes some notes to the design of such loop antennas for MIFARE Ultralight AES.

The detail loop antenna design is explained in [1]. Although such antennas are relatively straightforward in principle and look very similar when comparing various contactless smartcards, experience proves that their parameters do have a noticeable impact on performance.

In this document, some examples are attached for your reference, but it is recommended to verify them before starting production. In addition, customers who want to reuse existing MIFARE product-based card coil antenna design or design a completely new antenna can also get information as to what considerations to make.

1.1 How to use this document

In this document only the hints and notes specific to MIFARE Ultralight AES are explained. All the basics and design details are explained in [1]. Please use [1] as the base document and apply wherever requires the notes mentioned here.

1.2 Terms and abbreviations

Table 1. Abbreviations

Acronym	Description
AES	Advanced Encryption Standard
PCD	Proximity Coupling Device
PICC	Proximity IC Card

2 Card Coil design notes for MIFARE Ultralight AES

There are different classes of antennas defined in the ISO/IEC 14443-1 / Amd. 1, which feature different antenna sizes. These antenna classes may be used in contactless application for the MIFARE Ultralight AES PICC. For different antenna classes, the design of PICC coils is different. Even different application requirements also lead to different antenna designs.

Basically, three parameters are important for the card coil design: coil area, coil quality factor, and the resonance frequency of the transponder under loaded conditions.

2.1 Different classes of antennas according to ISO/IEC 14443-1

In Figure 1 different antenna sizes according to ISO/IEC 14443-1[2010] are shown.

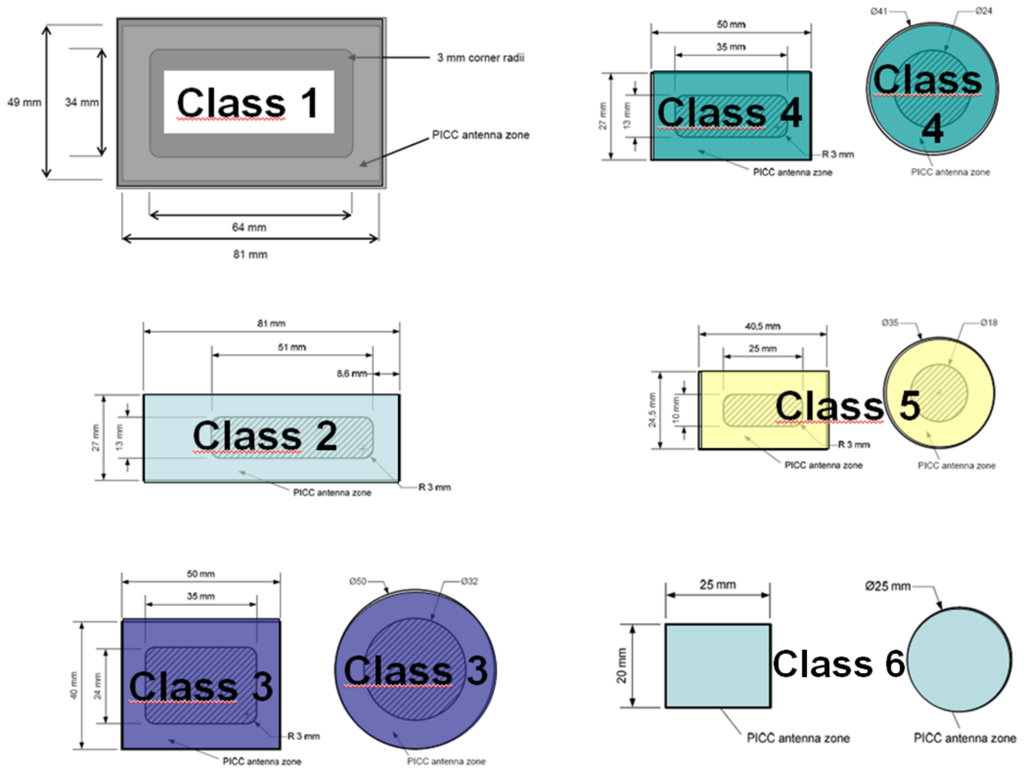

Figure 1. Different Coil antenna sizes according to ISO/IEC 14443-1

2.2 Card coil area

Make the card coil area as large as possible. Bending corners are better than sharp corners.

2.3 Coil Q-factor

To get optimum performance and to cover manufacturing tolerances, for MIFARE Ultralight AES, the recommended coil Q values are given in Table 2.

2.3.1 Measurement of Coil Q-factor

There are different ways to measure the Q-factor of the coil, which may end up with different results. It is recommended to follow the way described in the Card Coil Design Guide [1] or get help from your NXP technical support.

2.4 Definition for “unloaded” and “loaded” conditions.

“***loaded conditions***”, or just “loaded”, means that the MIFARE Ultralight AES chip gets enough power to be able to fully operate. With the NXP setup used (defined in [2]), those conditions are achieved, when the power at the network analyzer output is set to the value of +10 dBm.

“***unloaded conditions***”, or just “unloaded”, means that the MIFARE Ultralight AES chip does not get enough power in order to even start to operate. With the NXP setup used (defined in [2]), those conditions are achieved, when the power at the network analyzer output is set to the value of -30 dBm.

Both conditions were created with an NXP dedicated measurement setup, which is described in [2]. All measurement results presented further down in this document have been obtained with this setup and under “loaded” and “unloaded” conditions as defined earlier in this paragraph.

2.5 Loaded resonance frequency of the transponder

The loaded resonance frequency of the transponder is the resulting resonance frequency, if the IC is operated under loaded conditions.

In general, the appropriate resonance frequency of the transponder depends on the card ICs and applications. To get optimum performance and to cover manufacturing tolerances, for MIFARE Ultralight AES, use the recommended loaded resonance frequency given in Table 2.

2.5.1 Measurement of loaded resonance frequency of the transponder

There are different ways to measure the resonance frequency of the transponder, which may end up with different results. It is recommended to follow the way described in the Card Coil Design Guide [2] or get help from your NXP technical support.

2.6 NXP recommendation for PICC coil design

Table 2 summarizes the recommendations for the PICC coil design.

Note the following points applicable to the 17 pF chip version:

- MIFARE Ultralight AES works best between 13.56 - 16 MHz loaded fres.
- For maximum operating distance, the loaded fres is ideally close to 14.5 MHz.
- A loaded fres too close at 13.56 MHz (e.g 14.00 MHz) might detune the reader antenna and result in reading issues on some PCDs.

Table 2. PICC coil design recommendation

Antenna class	Recommended variant of MIFARE Ultralight AES	Recommended loaded transponder resonance frequency (f_R)	Recommended Coil Q	Comments
Class 1	17 pF	13.56 MHz < fR < 16 MHz	> 30	Transponder optimum loaded resonance frequency for single card operation is close to 14.5 MHz. Transponder optimum loaded resonance frequency for stacked 2 cards operation is close to 15.5 MHz.
Class 2	50 pF	13.56 MHz < fR < 14.50 MHz	> 40	The optimum loaded resonance frequency is slightly above 13.56 MHz.
Class 3	50 pF	13.56 MHz < fR < 14.50 MHz	> 40	The optimum loaded resonance frequency is slightly above 13.56 MHz.
Class 4	50 pF	13.56 MHz < fR < 14.50 MHz	> 40	The optimum loaded resonance frequency is slightly above 13.56 MHz.
Class 5	50 pF	13.56 MHz < fR < 14.50 MHz	> 40	The optimum loaded resonance frequency is slightly above 13.56 MHz.
Class 6	50 pF	13.56 MHz < fR < 14.10 MHz	> 40	The optimum loaded resonance frequency is slightly above 13.56 MHz.

Those recommended quality factor values for the coil are important to get a good power transfer and to increase the so called power range of the transponder.

For class 1 antennas (17 pF IC version), a minimum Coil Q-factor of 30 is recommended. The resulting transponder Q-factor under “unloaded” conditions is similar to this value. Once the PICC starts to operate, its (loaded) Q-factor is decreasing and this is leading to a loaded Q-factor in the range of 8-9. This value is in the middle of the range of 6-15, which results in a good performance.

All those considerations are valid for class 2 to class 6 antennas (50 pF IC version) a minimum coil Q-factor of 40 is recommended.

Please check Section 2.9.1 in this document for further reference on this topic.

2.7 Antenna design hints and recommendations for 17 pF chip

2.7.1 ID1-sized wired antennas

Hints for antenna design

- Within the confines of the application and the card manufacturing processes used, try to maximize the antenna size. The outermost turn of the antenna coil should be placed as close as possible to the edge of the area represented by an 81 x 49 mm rectangle. Class 1 antenna examples (with two different parameters) are shown in Figure 2.
- **Note:** International standards and industry specifications may restrict the choice of the maximum allowed antenna coil size.

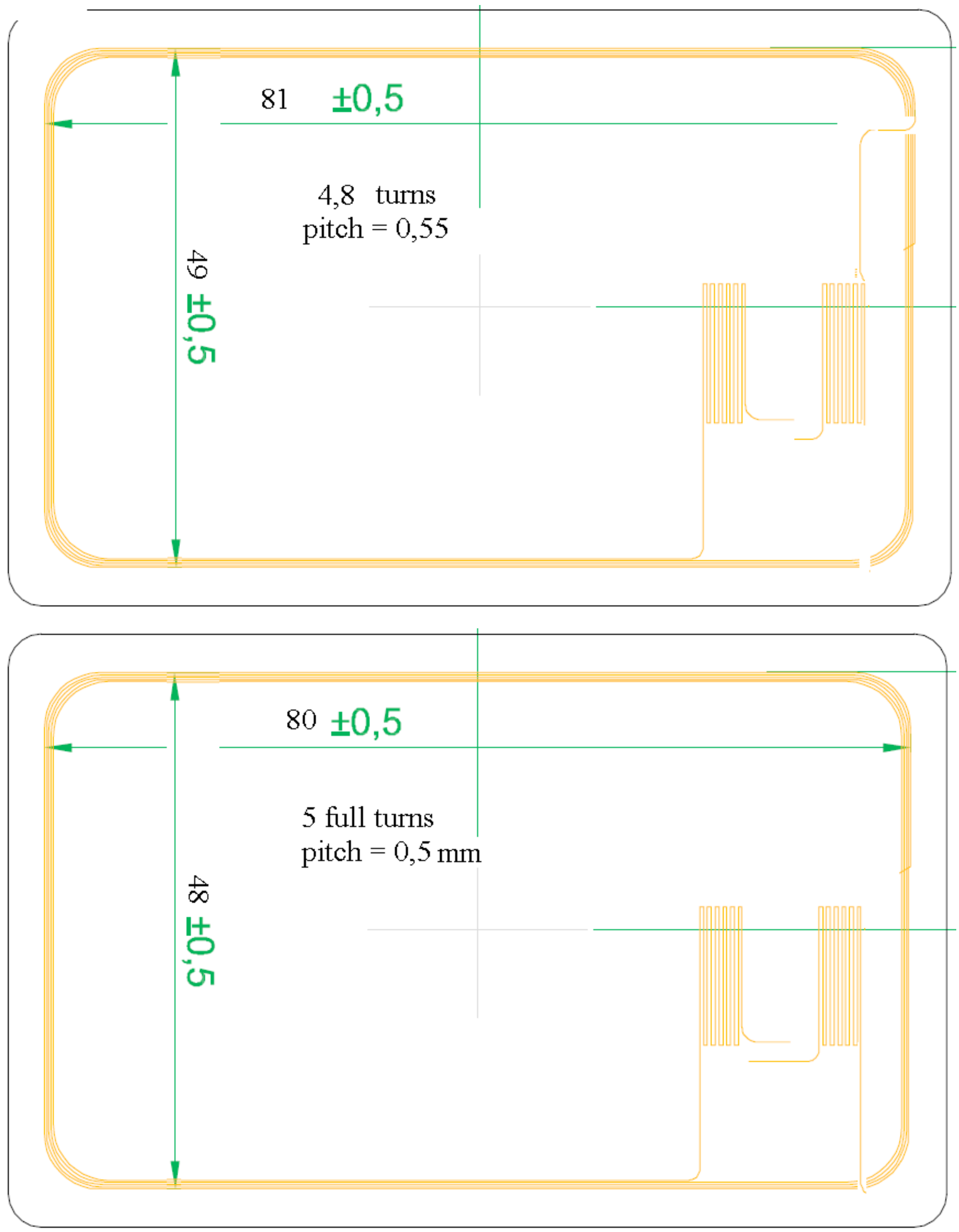

Figure 2. Class 1 antenna examples (with two different parameters)

For ID1 size (class 1) antennas, the 17 pF chip version is recommended. For all other classes, the usage of the 50 pF version of the MIFARE Ultralight AES PICC is recommended.

2.7.2 ID1-sized etched antennas

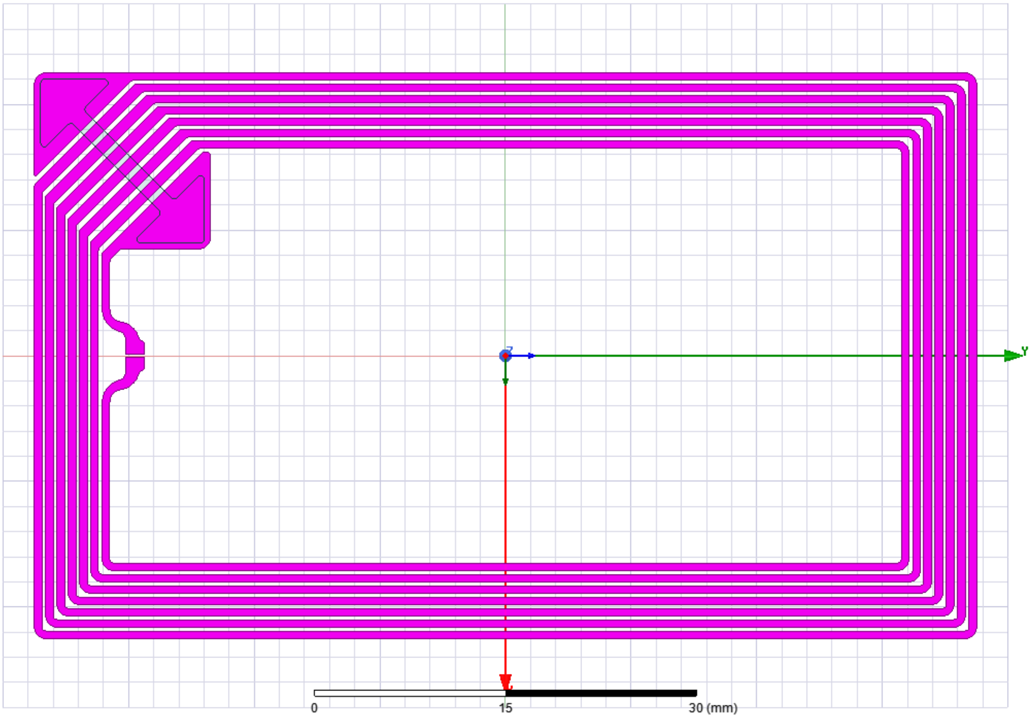

Figure 3. ID-1 sized etched antenna

An etched antenna coil (typical made of copper/aluminium on polyester) may be used as well. Figure 3 shows a 7-turn antenna with a dimension of 75 x 45 mm.

- Track width, w = 0,6 mm
- Gap between tracks, g = 0,3 mm
- Track thickness (coil): t_coil = 0,03 mm
- Track thickness (bridge): t_coil = 0,01 mm
- Number of Turns, *N* = 7
- Carrier Material: Polyester
- Carrier Thickness: 0.038 mm
- Carrier Er: 3.2

Above mentioned parameters will together with a MIFARE Ultralight AES 17 pF result in a loaded $f_{RES}$of ~15.0 MHz.

2.8 Practical design hints and recommendations for 50 pF chip

For class 2 and up to class 6 antennas, it is recommended to use 50 pF chip version.

2.8.1 Round etched antennas

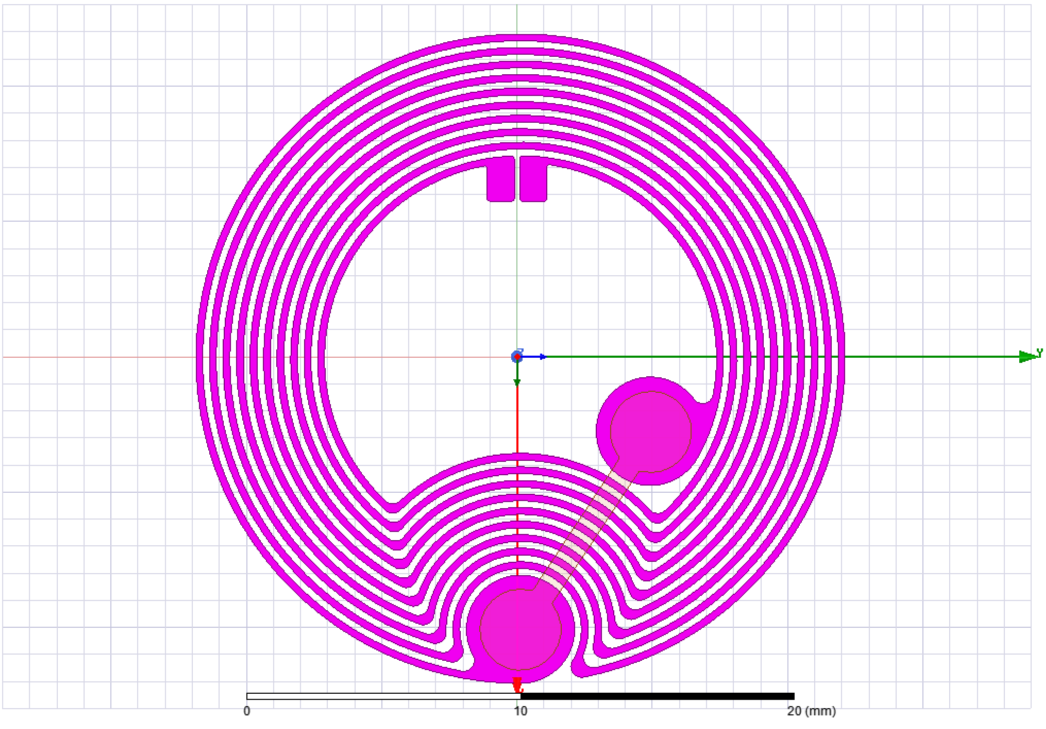

Figure 4. Round (d=24 mm) etched antenna

Figure 4 shows a small antenna design for the MIFARE Ultralight AES 50 pF.

- Track width, w = 0,25 mm
- Gap between tracks, g = 0,25 mm
- Track thickness (coil): t_coil = 0,03 mm
- Track thickness (bridge): t_coil = 0,01 mm
- Number of Turns, *N* = 10
- Carrier Material: Polyester
- Carrier Thickness: 0.038 mm
- Carrier Er: 3.2

Above mentioned parameters will together with a MIFARE Ultralight AES 50 pF result in a loaded $f_{RES}$of ~14.0 MHz.

2.9 Antenna coil design considerations for unloaded and loaded conditions

2.9.1 Quality factor and bandwidth of the transponder

The quality factor of a transponder Q_T is an important parameter defined at air interface. The value of Q_T has to be properly chosen in order to guarantee sufficient performance for both power and data transmission.

The quality factor of the transponder results from the quality factor values of its' both components, the antenna (Q_A) and the chip (Q_C). It is determined by the component with lower Q-factor, in this case by the Q_C. Taking into account that both chip electrical parameters (capacitance C_C and resistance R_C) are power and frequency dependent, it is obvious that the Q_T also changes with power and frequency. This point is relevant when considering Q_T both under "loaded" and "unloaded" conditions.

For a transponder resonant LCR circuit, Q_T can be determined in frequency domain. Q_T is related to the bandwidth, which can be measured from the resistance curve as shown in Figure 5. [3].

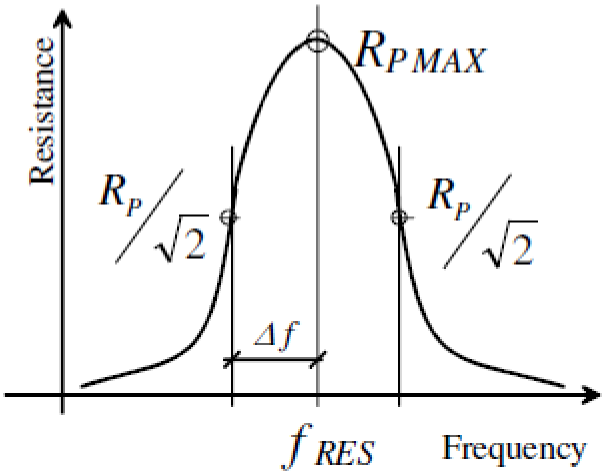

Figure 5. Resistance curve for determining the transponder bandwidth

Q_T can be calculated by using formula Equation 1.

$$Q_T = \frac{f_{res}}{2 \cdot \Delta f} = \frac{f_{res}}{B} \quad (1)$$

Where f_{res} is a transponder resonance frequency and Δf is defined in Figure 5.

2.10 Required transponder bandwidth for (PICC -> PCD) data transfer

The demand for data transfer sets requirements on the transponder bandwidth B, which limits the transponder quality factor Q_T. The needed bandwidth is related to the modulation scheme, coding and data rates used.

The theoretical required bandwidth for 106 kbit/s is 1.8 MHz . Detailed explanation can be found in [4].

Important remark: If a transponder bandwidth is smaller than theoretically required, it does not automatically mean that the communication will not be possible. What will happen is that the sideband levels of the card answer will be damped more than 3 dB (which was accepted for a classical definition of bandwidth), but might be still sufficient for successful communication.

Note for higher antenna classes (class 2 to class 6): With coil size reduction the inductance of the coil decreases. Additionally, there is a recommendation to utilize the 50 pF IC version together with antennas smaller than class 1. This results in the increase of the transponder Q_T factor (QT = Rp * sqrt(**Cp** / L)). It is recommended to check the resulting Q_T or bandwidth B of a newly designed transponder, to enable successful communication.

2.11 Operation with stacked cards

If more than one card is on the reader, then the system resonance frequency will reduce, which causes the energy transfer between cards and reader to be reduced. Therefore the reading distance will get reduced as well. In order to compensate for that, one can tune the card to a higher resonance frequency. However, this will result in a worse performance in single card operation.

For the stacked card use case, it is recommended to tune the card to around 16.5 MHz to allow the resonance frequency of the stacked card system not to fall significantly below 13.56 MHz and therefore optimize for stacked cards operation. Attention: Hmin for single card operation will be higher if the resonance frequency is at 16.5 MHz.

3 References

[1] AN11093 Card Coil Design Guide, available in Secure Files on NXP.com, secure files number: AN0117**[1]

[2] PICC and VICC Resonance Frequency Measurement

[3] M. Gebhart, Air Interface, Antennas and Signals in Contactless Near-Field Communication 2nd lecture in Selected Topics of Advanced Analog Chip Design, 439.224

[4] ISO/IEC 14443-3 Identification cards — Contactless integrated circuit cards — Proximity cards - Part 3: Initialization and anticollision

---

[1] ** document version number

4 Legal information

4.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

4.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

4.3 Licenses

ICs with DPA Countermeasures functionality

NXP ICs containing functionality implementing countermeasures to Differential Power Analysis and Simple Power Analysis are produced and sold under applicable license from Cryptography Research, Inc.

4.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

DESFire — is a trademark of NXP B.V.

MIFARE — is a trademark of NXP B.V.

MIFARE Plus — is a trademark of NXP B.V.

MIFARE Ultralight — is a trademark of NXP B.V.

Tables

Figures

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 20 April 2022
Document identifier: AN13453