

# Using the M68HC05 Family On-Chip Voltage Regulator

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## INTRODUCTION

Two 1993 additions to the M68HC05 Family of microcontrollers (MCUs) are the MC68HC705V8 and the MC68HC05V7. These two MCUs, manufactured with a state-of-the-art mixture of ultra-high voltage CMOS (UHVCMOS) and bipolar analog processing, each include an integrated 12-volt (nominal) to 5-volt voltage regulation system. This voltage regulation circuit, which is enabled via mask option, can provide the 5 volts necessary for powering the MCU in an application.

This on-chip voltage regulator is specified for normal operation over an input voltage range of 8 V to 16 V, optimizing it for use in the automotive environment. In automotive applications, either of these two devices can be connected directly to the vehicle's battery via the  $V_{BATT}$  pin, thus eliminating the external voltage regulator normally required to provide the 5-V supply for the MCU. In addition to supplying the 5 volts for internal use, this integrated regulator also can supply additional current off chip, powering other application components.

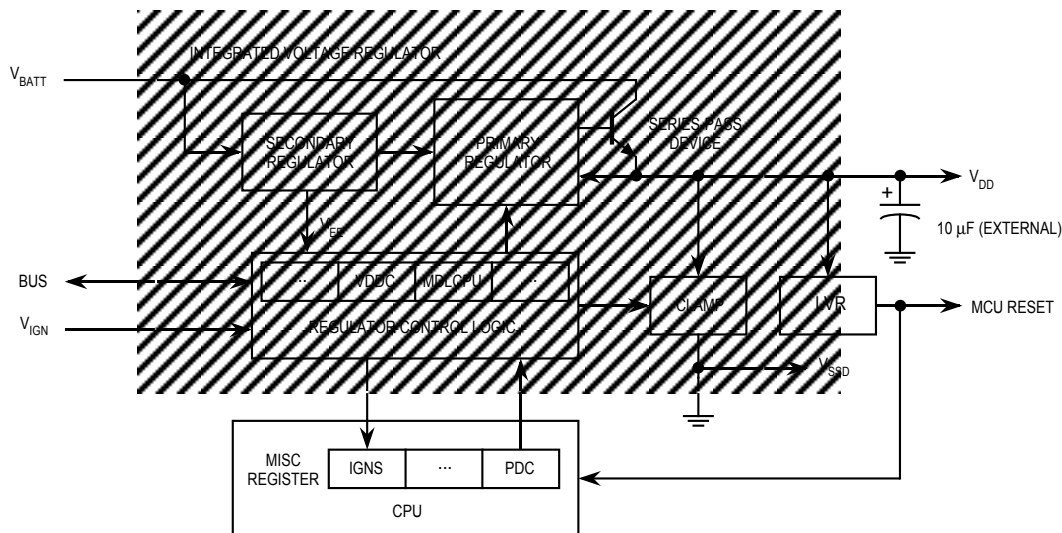
Although designed to operate over a normal input voltage range of 8 volts to 16 volts, this voltage regulator is specified for correct operation with an input voltage of up to 26.5 volts for a few minutes. This ensures that the device will operate during double-battery situations, such as during a jump start from a wrecker. In addition, the regulator's design and processing enable it to survive many of the severe electrical transients common in an automotive electrical system, such as the load dump voltage spikes which can occur in a vehicle's 12-volt supply when the battery becomes disconnected while the engine is running.

This application note provides the user with an overview of the voltage regulator architecture and an outline of the external components and software necessary for correct operation of this regulator as it has been implemented on the above mentioned devices. Although this voltage regulator currently is available on two M68HC05 MCUs only, Freescale is likely to make this regulator available on more devices. In addition, the maximum operating specifications described in this application note apply to the MC68HC705V8 and the MC68HC05V7 and may be modified and expanded in future designs.

## POWER SUPPLY ARCHITECTURE

The M68HC05 Family's integrated voltage regulation circuit consists of three main parts: the primary regulator, the secondary regulator, and the power supply control logic. (See Figure 1.) A low-voltage reset (LVR) circuit also has been included on the MC68HC705V8 and MC68HC05V7 to prevent unpredictable operation of the MCU in the event the 5-volt supply level drops below the specified operating level.





**Figure 1. On-Chip Voltage Regulator Block Diagram**

The primary voltage regulator circuit is a classic three terminal design using an integrated series-pass transistor. The output of the pass transistor is fed into an error amplifier in the primary regulator where it is compared to a reference voltage produced by a band-gap reference circuit. The output of the error amplifier, in turn, controls the current through the pass transistor. As the load on the regulator output increases or decreases, the output of the error amplifier changes proportionally, increasing or decreasing the current through the pass transistor. This enables the regulator to maintain a stable 5-volt output under changing load conditions.

The 5-volt output of the primary regulator supplies power directly to the digital logic portion of the MCU. The primary regulator output also is connected to the  $V_{DD}$  pins to allow for easy connection to external decoupling capacitors and the 10  $\mu$ F supply stabilization capacitor. Connection of the power supply output to the  $V_{DD}$  pins also allows 5 volts to be passed externally to the analog circuitry of the MCU and to other components in an application. Should a short circuit occur between the  $V_{DD}$  and  $V_{SSD}$  pins, an over-current protection circuit has been included to prevent damage to the primary voltage regulator. Refer to the MC68HC05V7 and MC68HC705V8 general release specifications Freescale document numbers HC705V7GRS/D and HC705V8GRS/D, for the maximum supply current available from the voltage regulator on each MCU.

The secondary voltage regulator has two functions. The first is to supply  $V_{EE}$  to the small amount of power supply control logic necessary for enabling and disabling the primary voltage regulator. The secondary regulator's other function is to act as a "pre-regulator" for the input voltage supplied to the primary regulator. This helps reduce the variation in the input voltage seen by the primary regulator, improving the line rejection specification of the primary regulator output with respect to changes in the input voltage.

### NOTE

The primary voltage regulator can be enabled only if the mask option enabling the internal voltage regulation system is selected. However, the secondary regulator and the power supply control logic will always be enabled whenever the supply voltage to the  $V_{BATT}$  pin is above the minimum operating voltage specified for correct regulator operation.

The power supply control logic enables the primary voltage regulator to be put into the power-conserving standby mode through software, then to be re-enabled whenever the appropriate external conditions are detected by the MCU. This enabling and disabling of the primary regulator is referred to as **power moding**. Although the power supply control logic is always enabled, the small amount of circuitry requires a minimal amount of current for normal operation, typically less than 100  $\mu$ A. This ensures that the MCU's current consumption is held to a minimum when the primary regulator is put into standby mode to conserve power.

The mask option-selectable LVR circuit, when enabled, allows the MCU to be held in a reset state whenever the voltage at the  $V_{DD}$  pins, whether supplied internally or externally, drops below the specified threshold. This helps prevent incorrect operation during power-up, power-down, or brown-out situations.

## POWER SUPPLY EXTERNAL CONFIGURATION AND CONTROL

Several MCU pins are directly involved in the operation of the integrated voltage regulator. In addition, a few external components are recommended to help ensure stable operation of the voltage regulator. These MCU pins and the external components recommended for proper operation are described below. Figure 2 illustrates the hardware configuration and external components outlined in the description below. The pin designations in Figure 2 refer to the MC68HC705V8 in the 68-pin plastic leaded chip carrier (PLCC) package. This hardware description assumes the voltage regulator circuit has been properly configured internally.

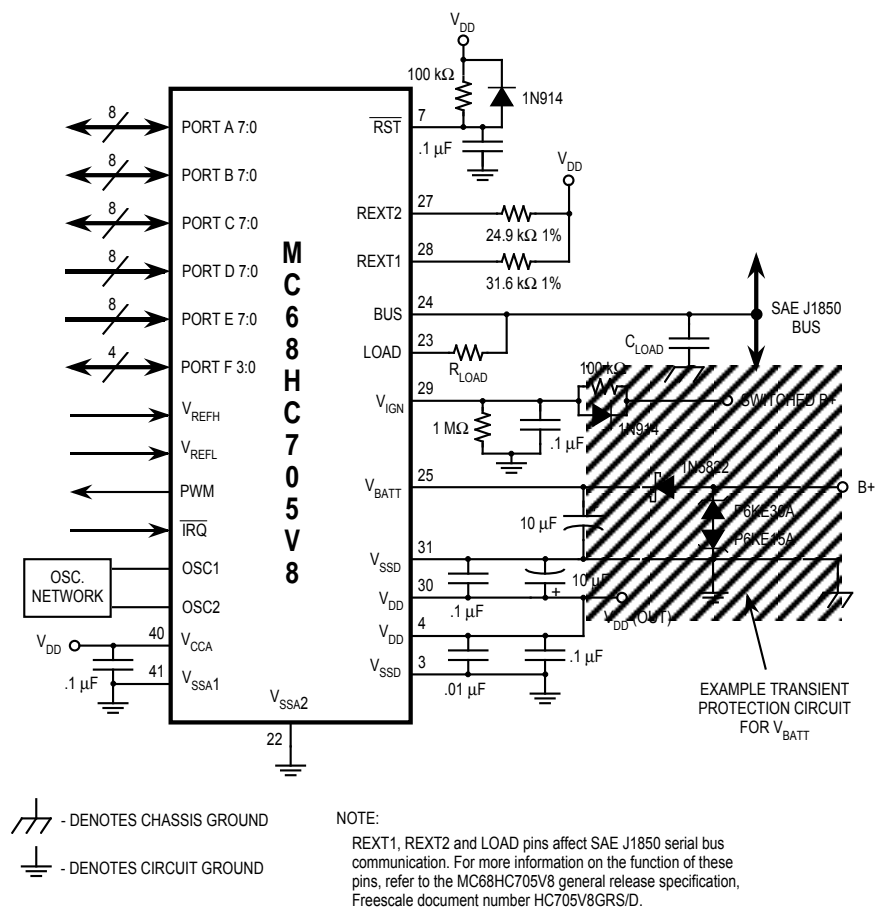
### Voltage Regulator Input

The  $V_{BATT}$  pin (pin 25) is the 12-volt input to the internal voltage regulator, with the ground return provided through the two  $V_{SSD}$  pins (pins 3 and 31). In automotive applications, the  $V_{BATT}$  pin can be connected directly to the vehicle's battery, allowing the internal regulator to provide the 5-volt supply for the MCU. However, voltage transients exceeding the maximum specifications of the  $V_{BATT}$  pin are sometimes encountered in automotive applications. For this reason, additional components may be necessary to ensure the  $V_{BATT}$  pin is not damaged if such a situation occurs. The circuit in Figure 2 includes an example transient protection network between the vehicle's battery and the  $V_{BATT}$  pin to protect against this. To help reduce the effects of temporary fluctuations in the 12-volt supply caused by noise and by changes in loading on the vehicle's electrical system, a large capacitor (10  $\mu$ F or greater) can be placed between the 12-volt supply and ground. If high frequency noise on the 12-volt supply is a problem, the user also can add decoupling capacitors between  $V_{BATT}$  and  $V_{SSD}$ . Ceramic or polystyrene capacitors should be used to provide noise rejection over a wide frequency range. If decoupling capacitors on the 12-volt supply are used, they should be placed as close to the MCU pins as possible.

The  $V_{IGN}$  pin (pin 29) is used to tell the power supply control logic when to enable the primary regulator. The  $V_{IGN}$  pin is an input pin designed to operate over an input voltage range equal to the supply voltage at the  $V_{BATT}$  pin. If a rising edge is detected at the  $V_{IGN}$  pin and the primary regulator is in standby mode, the primary regulator will transition to the normal operating mode, powering up the MCU. This feature can be useful in those applications where a component or module is required to remain powered up but inactive for long periods. This is common in the automotive environment, where a system may be required to operate whether the vehicle ignition is switched on or not. In this type of application, the  $V_{BATT}$  pin can be connected to a constant 12-volt supply while the  $V_{IGN}$  pin is connected to a switched 12-volt supply. Once the switched supply is turned off, the application software can put the primary regulator into standby mode, powering the MCU down to conserve energy until operation is again required. When the switched supply is turned back on, the rising edge at the  $V_{IGN}$  pin will cause the primary regulator to exit standby mode and reactivate the MCU. This type of operation allows the MCU to conserve energy when activity is not required, but to be reactivated immediately when necessary.

In applications where a switched power supply is not available or constant power to the MCU is not necessary, the same 12-volt supply can be connected to both the  $V_{BATT}$  pin and the  $V_{IGN}$  pin. If this is done, whenever the 12-volt supply is connected, the rising edge occurring at the  $V_{IGN}$  pin will cause the primary regulator to exit the standby mode and become fully activated. In these applications, it is recommended that some type of power-on reset (POR) delay circuit be used to connect the power supply to the  $V_{IGN}$  pin. This delay should be timed to allow the power supply at the  $V_{BATT}$  pin to reach the minimum specified operating level before the rising edge is detected at the  $V_{IGN}$  pin. In the future, a  $V_{IGN}$  POR circuit may be integrated onto these devices to further reduce the number of external components required. Although the example circuit in Figure 2 has  $V_{IGN}$  connected to a switched 12-volt supply, an example POR circuit has been included.

A rising edge detected at the BUS pin (pin 24) also can cause the primary regulator to exit the standby mode and become fully active, if this mask option is selected. The BUS pin is a serial multiplex interface pin which allows the MCU to communicate with other components over a serial multiplex communication network using the SAE standard J1850 communication protocol. Activity detected at the BUS pin could be due to another node on the serial network transmitting a message or simply due to noise appearing on the serial bus.



### Figure 2. Automotive Voltage Regulator Circuit Example

## Voltage Regulator Output

As described in POWER SUPPLY ARCHITECTURE, in addition to supplying 5 volts to the digital circuitry of the MCU internally, the output of the on-chip voltage regulator is connected to the two  $V_{DD}$  pins (pins 30 and 4) of the MCU to allow external stabilization and decoupling of the power supply output. To ensure a stable 5-volt supply from the primary voltage regulator on the MC68HC705V8 and MC68HC05V7, a 10  $\mu$ F tantalum or electrolytic bulk capacitor should be connected between pins 30 and 31 ( $V_{DD}$  and  $V_{SSD}$ , respectively). This capacitor should be placed between this pair of  $V_{DD}/V_{SSD}$  pins since they are physically closer to the output of the voltage regulation circuit on the device than the other pair of  $V_{DD}/V_{SSD}$  pins (pins 4 and 3, respectively). This capacitor should be positioned as close to the  $V_{DD}/V_{SS}$  pins as possible to maximize its effect.

High frequency decoupling capacitors (ceramic or polystyrene) should be placed between both pairs of  $V_{DD}/V_{SSD}$  pins, also positioned as close to the MCU as possible (even closer than the bulk capacitor at pins 30 and 31). These are necessary to help reduce radiated RF emissions as well as to reduce high frequency noise on the 5-volt supply. The example in Figure 2 has .1  $\mu$ F capacitors between each pair of  $V_{DD}/V_{SSD}$  pins for external decoupling. Because pin 4 is connected internally to the output of the primary voltage regulator through a resistance of approximately 40  $\Omega$  and the inductance of the bond wire at each pin is approximately 4 nH, the self-resonance of the decoupling network between pins 3 and 4 may be too low. In this case, a smaller capacitor (470 pF to .01  $\mu$ F) can be added in parallel to the .1  $\mu$ F between these pins to increase the bandwidth of the decoupling network. If so, the smaller capacitor should be placed closest to the MCU. **Remember: The farther these capacitors are from the MCU pins, the less effect they will have in reducing electrical noise in the system.**

The  $V_{SSD}$  pins should be connected in the application to ensure an adequate low-impedance ground return for the system. The effect of not connecting the  $V_{DD}$  pins is not yet known, and it is currently recommended that they be connected as well.

In the example circuit in Figure 2, the 5 volts available from the  $V_{DD}$  pins are connected to the  $V_{CCA}$  pin (pin 40) to supply 5 volts to the analog circuitry. In both the MC68HC705V8 and the MC68HC05V7, the analog and digital supplies are not connected internally, so the 5 volts for the analog circuitry must be supplied externally. As with any externally supplied power source, an appropriate decoupling capacitor has been placed between  $V_{CCA}$  and the adjacent A/D subsystem analog ground return ( $V_{SSA1}$ , pin 41). A separate ground return ( $V_{SSA2}$ , pin 22) is provided for the SAE J1850 analog subsystem.

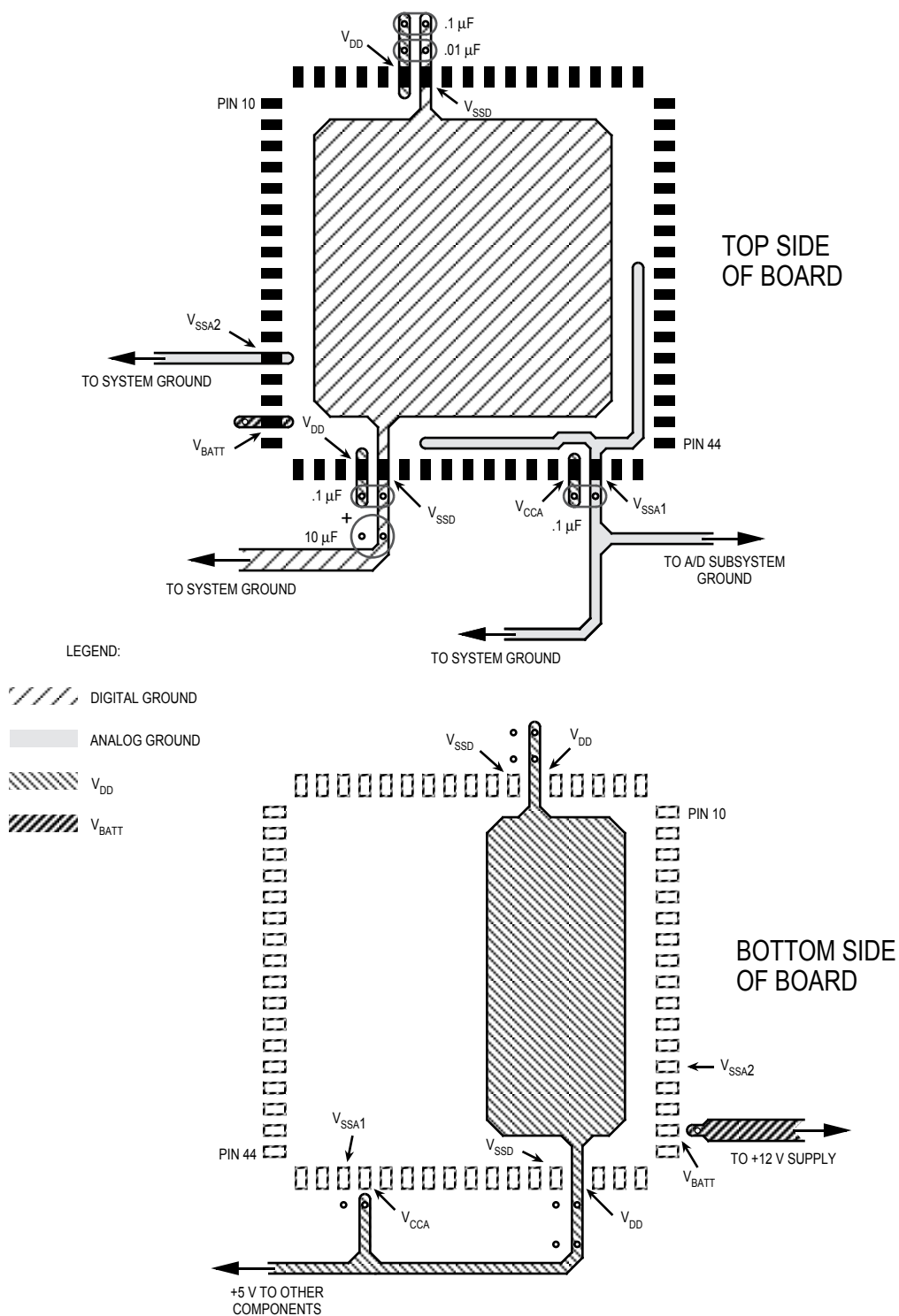
To power additional external circuitry from the on-chip regulator, either of the  $V_{DD}$  pins can be used as the source of 5 volts. However, when possible, the  $V_{DD}$  pin closest to the on-chip regulator (pin 30) should be used as a 5-volt source for external components. This improves the regulator's response to the additional fluctuations in the 5-volt supply loading caused by supplying the external components.

Also shown in Figure 2 is a simple power-on reset (POR) circuit connected to the reset pin ( $\overline{RST}$ , pin 7) to provide a time delay between full activation of the primary regulator and external release of the  $\overline{RST}$  pin. Although an external POR circuit is not required when the LVR mask option is selected, it does allow time for the  $V_{DD}$  supply to stabilize before the  $\overline{RST}$  pin is released externally. If the LVR option is not selected, the user should certainly consider some sort of external POR/LVR circuitry to prevent unpredictable operation during power-up, power-down, and brown-out situations.

## Printed Circuit Board Considerations

When designing the application printed circuit board (PCB), appropriate PCB layout techniques should be used when routing power and ground to help reduce electromagnetic interference (EMI) problems. These techniques can include the use of four (or more) layer boards, single-point grounds and micro-islands. While ground and power planes can significantly reduce noise on a board, using them is not always an option. Figure 3 illustrates one example of a 2-sided PCB power and ground layout for the MC68HC705V8 in a 68-pin PLCC package. On the top layer (viewed from the top), the two  $V_{SSD}$  pins are tied together through a low-impedance path and the  $V_{SSD}$ ,  $V_{SSA1}$ , and  $V_{SSA2}$  grounds are all routed back to the main system ground using the single-point ground technique. The 12-volt and 5-volt supply lines are routed on the bottom layer (here viewed from the bottom), including the low-impedance path connecting the two  $V_{DD}$  pins. The  $V_{CCA}$  supply is provided by the internal regulator output at pin 30. The preferred locations for the 5-volt supply output stabilization and decoupling capacitors also are shown. The layout in Figure 3 is intended as an example only, not as the only correct layout solution for all applications.

For more information on various techniques for reducing EMI problems in PCB layout, refer to Freescale Application Notes AN1050/D *Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers* and AN-1258/D *Proper Layout Techniques for Noise Reduction in MCU-Based Systems*.



**Figure 3. An Example of a 2-Sided PCB Layout for the MC68HC705V8**



# INTERNAL CONFIGURATION AND CONTROL OF THE POWER SUPPLY

The voltage regulation circuit on the MC68HC705V8 and MC68HC05V7 is controlled by the user through several mask options and through one control bit and one status bit in a user register on each MCU. A description follows of the mask options and the user register bits and how they affect the voltage regulator operation. This description assumes the user is familiar with the implementation of user registers and mask option registers on the M68HC05 Family.

## Mask Options

Three mask options on the MC68HC705V8 and MC68HC05V7 affect the operation of the on-chip voltage regulator. These mask options include voltage regulator enable/disable, enabling a  $V_{DD}$  to  $V_{SSD}$  clamp when the primary regulator is in standby mode and re-enabling the primary regulator from standby mode when a rising edge is detected at the BUS pin. An additional mask option is available to enable the LVR circuit. The mask options are user-programmable on the EPROM-based MC68HC705V8 via the mask option register (MOR, address \$3C00) and are customer-selected at the time of ROM pattern submission on the ROM-based MC68HC05V7. Each option is described here as programmed by the user on the MC68HC705V8. For an illustration of the placement of the bits in the MOR register, refer to Figure 4.

		Bit 7	6	5	4	3	2	1	Bit 0
MOR \$3C00	Read:	0	REGEN	VDDC	MDLCPU	LVR	STOPEN	IRQ	COPEN
	Write:								
	Reset:	Unaffected by reset							
		<div></div> = Unimplemented							

### NOTES:

1. Bit 7 of the MOR is not implemented on the MC68HC705V8.
2. Bits 2-0 are mask options which do not affect operation of the on-chip voltage regulator or the LVR circuitry.

Figure 4. MC68HC705V8 Mask Option Register

The REGEN bit (bit 6) in the MOR of the MC68HC705V8 is used to enable the on-chip voltage regulation system. If this bit is programmed to a logic one, the primary voltage regulator will be enabled whenever the minimum specified voltage necessary for proper regulator operation is applied to the  $V_{BATT}$  pin and the appropriate external conditions are detected by the MCU. In addition to the primary regulator, the REGEN bit also enables the power moding function of the power supply control logic. If the REGEN bit is programmed to a logic zero, the primary voltage regulator never will be enabled. In this case, the user must supply 5 volts to both  $V_{DD}$  pins of the MCU from an external power source. The secondary regulator always will be enabled whenever the supply voltage to the  $V_{BATT}$  pin is above the minimum operating voltage specified for correct regulator operation, regardless of the state of the REGEN bit.

If the VDDC bit (bit 5) in the MOR is programmed to a logic one, an active device clamping  $V_{DD}$  to  $V_{SSD}$  will be enabled whenever a logic zero is written to the PDC bit in the MISC register. (See Figure 5.) This helps ensure that no devices (including the MCU) powered by the on-chip voltage regulator will be active as long as the primary regulator remains in standby mode. The  $V_{DD}$  to  $V_{SSD}$  clamp will be released whenever the external conditions necessary to enable the primary regulator are detected by the MCU (rising edge on  $V_{IGN}$  pin or optionally on BUS pin). If the VDDC bit is programmed to a logic zero, the active  $V_{DD}$  to  $V_{SSD}$



clamp will never be enabled. Although this option is available on the MC68HC705V8 even if the REGEN mask option is not selected, the user should be very careful about using it if an external power supply is used to provide 5 volts to the MCU. On the MC68HC05V7, it is not possible currently to select the VDDC mask option without selecting the REGEN mask option.

The MDLCPU bit (bit 4) in the MOR determines whether the primary regulator can be enabled from standby mode by a rising edge on the BUS pin. If the MDLCPU bit is programmed to a logic one, a rising edge detected at either the  $V_{IGN}$  pin or the BUS pin will cause the primary regulator, if in standby mode, to be enabled and the  $V_{DD}$  to  $V_{SSD}$  clamp, if active, to be released. This allows the user to put the primary regulator into standby mode to conserve power but still be able to activate the MCU and re-establish communication over the SAE J1850 serial bus once network communication resumes. If the MDLCPU bit is programmed to a logic zero, only a rising edge on the  $V_{IGN}$  pin will cause the primary regulator to exit standby mode and the  $V_{DD}$  to  $V_{SSD}$  clamp to be released. If the REGEN mask option is not selected, the MDLCPU mask option can still be used to control the operation of the  $V_{DD}$  to  $V_{SSD}$  clamp, provided the supply voltage to the  $V_{BATT}$  pin is above the specified minimum operating voltage.

The LVR bit (bit 3) in the MOR is used to activate the low voltage reset circuitry on the MCU. If this bit is programmed to a logic one, the LVR circuit will be enabled, causing the MCU to be held in a reset state internally whenever the voltage at the  $V_{DD}$  pins drops below the specified LVR inhibit voltage level ( $V_{LVRI}$ ). The device will remain in the reset state as long as the voltage at the  $V_{DD}$  pins remains between the LVR recovery voltage level ( $V_{LVRR}$ ) and the minimum specified  $V_{DD}$  voltage level. Below this level, the MCU operation becomes unspecified.

Once the voltage at the  $V_{DD}$  pins rises above  $V_{LVRR}$ , the MCU will be held in reset internally for 4064 CPU bus clock cycles. After this internal reset delay, the MCU will exit the reset state and re-enter the active state. (Refer to the MC68HC705V8 and MC68HC05V7 general release specifications, Freescale document numbers HC705V7GRS/D and HC705V8GRS/D, for the LVR inhibit and recovery voltage specifications.) If the LVR bit is programmed to a logic zero, the LVR circuit will not be enabled. The LVR mask option is available regardless of whether the REGEN mask option is selected.

## Miscellaneous Register

The miscellaneous register (MISC, address \$002F) is an MCU user register containing two bits which are used to control operation of the voltage regulator circuit. These bits allow the user to put the primary regulator into standby mode and to determine the status of the  $V_{IGN}$  pin. The following descriptions of these two bits and their operation are applicable to both the MC68HC705V8 and the MC68HC05V7. For an illustration of the MISC register, refer to Figure 5.

		Bit 7	6	5	4	3	2	1	Bit 0
MISC \$002F	Read:	IGNS	OCE	0	0	0	0	0	PDC
	Write:		OCE						PDC
Reset:		U	0	U	U	U	U	U	U
		= Unimplemented				U = Unaffected			

### NOTES:

- Bits 5-1 are unimplemented on the MC68HC705V8 and MC68HC05V7 and always read as zeros.
- Bit 6 does not affect the operation of the voltage regulator or the LVR circuitry.

**Figure 5. Miscellaneous Register on the MC68HC705V8/05V7**

The power-down control bit (PDC, bit 0) in the MISC register is used to put the primary regulator into the power-conserving standby mode whenever it is determined that the MCU should enter a low-power state. Whenever a logic zero is written to the PDC bit, the primary regulator immediately will enter standby mode and the active  $V_{DD}$  to  $V_{SSD}$  clamp will be enabled, if that mask option is selected. A logic zero can be written to the PDC bit at any time, regardless of the current level of the  $V_{IGN}$  pin or BUS pin. Writing a logic one to the PDC bit while the primary voltage regulator is enabled will have no effect on the operation of the primary regulator.

### NOTE

While writing a logic one to the PDC bit when the primary regulator is enabled will have no effect on regulator operation, it is highly recommended that the user do so after the primary regulator exits standby mode. Since this bit is not automatically set to a logic one when the primary regulator is enabled, doing so in software will ensure that any subsequent read/modify/write instructions involving other MISC register bits will not inadvertently put the primary regulator into standby mode by reading and then writing a logic zero to the PDC bit. Any full byte writes to the MISC register should, of course, have a logic one in the PDC bit position, if the user does not wish the primary regulator to be put into standby mode.

The ignition sense bit (IGNS, bit 7) in the MISC register is a read-only bit which simply reflects the state of the  $V_{IGN}$  pin. For example, in automotive “switched battery” applications where the 12-volt supply to the  $V_{BATT}$  pin is always available but the 12-volt supply to the  $V_{IGN}$  pin is switched by the vehicle ignition, the IGNS bit can be read by the CPU to determine when the automobile's ignition has been switched off. Since there is no hysteresis or digital filtering on the  $V_{IGN}$  pin, the user should utilize software filtering to verify that changes in the state of the  $V_{IGN}$  pin are not caused by transients on the switched 12-volt supply line. For more information on the operation of the  $V_{IGN}$  pin, refer to the Voltage Regulator Input section. As long as the supply voltage at the  $V_{BATT}$  pin is above the specified minimum operating voltage, the IGNS bit will reflect the level of the  $V_{IGN}$  pin, regardless of whether the REGEN mask option has been selected.

## POWER SUPPLY OPERATION

The software necessary for correct operation of the on-chip voltage regulator is minimal. Once the user has selected the desired external circuitry and MCU mask options, the only remaining software tasks are to initialize the regulator following power-up, put the primary regulator into standby mode when desired, and reinitialize the regulator once standby mode is exited.

The following operational descriptions are based on the example in Figure 2. In this example circuit, the  $V_{BATT}$  pin of the MC68HC705V8 is connected directly to the vehicle battery, the  $V_{IGN}$  pin is connected to switched battery, and the BUS pin is connected to the SAE J1850 serial communication network. The mask options selected for the following descriptions include the on-chip voltage regulator enabled (REGEN set), LVR circuit enabled (LVR set),  $V_{DD}$  to  $V_{SSD}$  clamp enabled when primary regulator disabled (VDDC set), and primary regulator enabled on a rising edge on the SAE J1850 network (MDLCP set).

### Voltage Regulator Initialization

In the example circuit in Figure 2, once the vehicle battery voltage applied to the  $V_{BATT}$  pin reaches the minimum specified operating level, the secondary voltage regulator will be enabled immediately and the primary regulator will enter the standby mode. The primary regulator will remain in the standby mode until either a rising edge (caused by the vehicle ignition being switched on) is detected at the  $V_{IGN}$  pin or activity on the SAE J1850 network is detected at the BUS pin. Once either of these events occurs, the primary

regulator will enter the normal operating mode and the regulator's 5-volt output will be applied internally to the digital portion of the MCU circuitry and externally to the  $V_{DD}$  pins. When the output voltage of the primary regulator reaches the specified minimum  $V_{DD}$  voltage level, the LVR circuit will place the device in the reset state. Once the primary regulator output reaches the  $V_{LVR}$  threshold, the MCU, after a delay equal to 4064 CPU bus clock cycles, will release the reset signal internally. If, at this point, the output of the POR circuit connected to the  $\overline{RST}$  pin has not reached a valid  $V_{IH}$  level, the device will remain in the reset state. Once the voltage level at the  $\overline{RST}$  pin does reach a valid  $V_{IH}$  level, the MCU reset signal will be released and the device will exit the reset state and begin normal operation.

During the MCU's initialization sequence, which normally occurs immediately following an exit from the reset state, the user should set the PDC bit in the MISC register to a logic one, since this bit is not automatically set when the primary regulator exits the standby mode. This will prevent subsequent read/modify/write instructions involving the MISC register from inadvertently returning the primary regulator to standby mode.

Setting the PDC bit is the only software initialization necessary for proper operation of the on-chip voltage regulator. Once this is done, the MCU can proceed with its normal initialization and application routines. Refer to Figure 6 for an illustration of this voltage regulator initialization sequence.

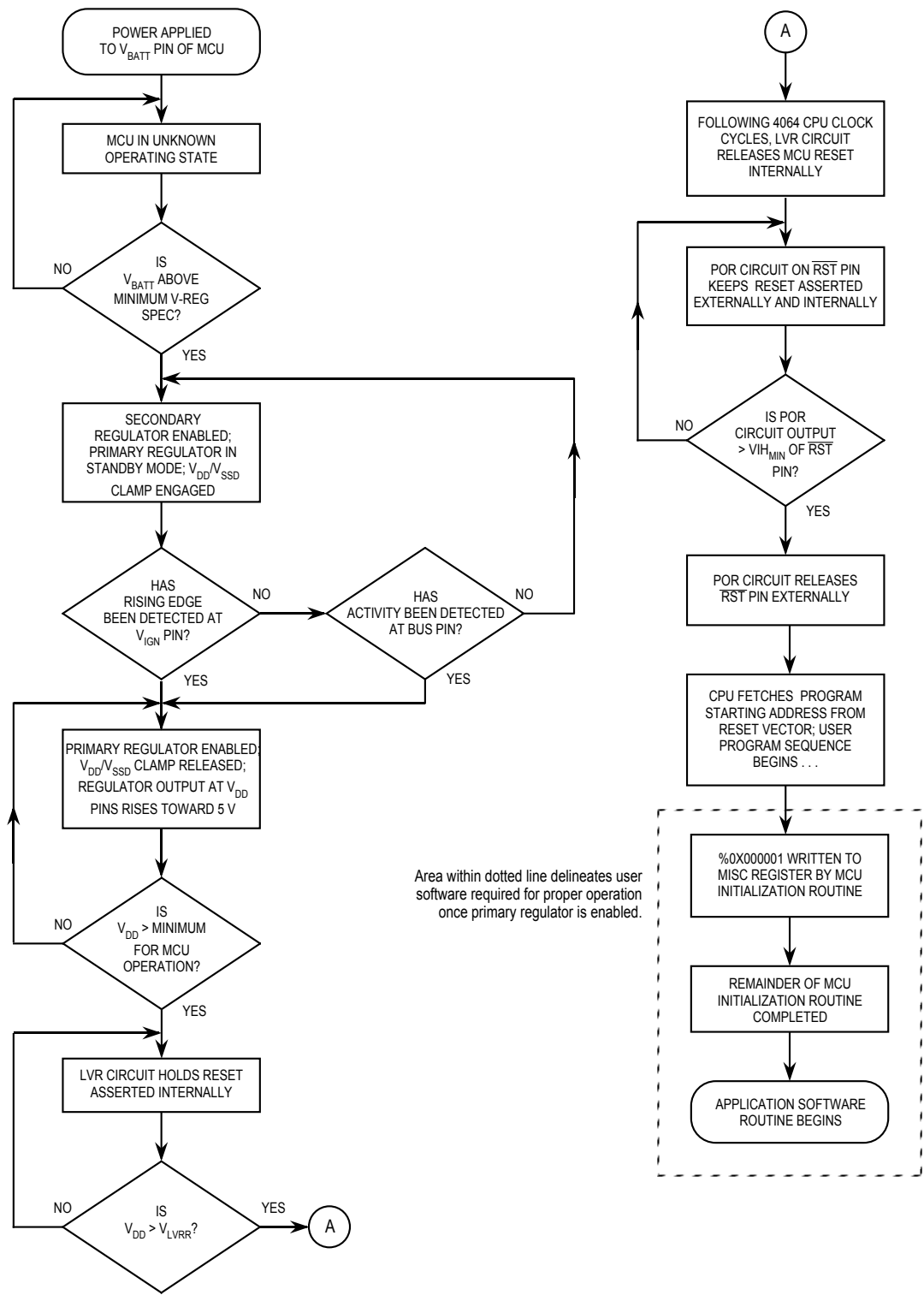
## Putting the Primary Regulator into Standby Mode

Once normal application processing is under way, the CPU can return the primary regulator to standby mode at any time by writing a logic zero to the PDC bit in the MISC register. In the Figure 2 example, this might be done whenever the IGNS bit in the MISC register is read as a logic zero, indicating that the vehicle ignition has been switched off.

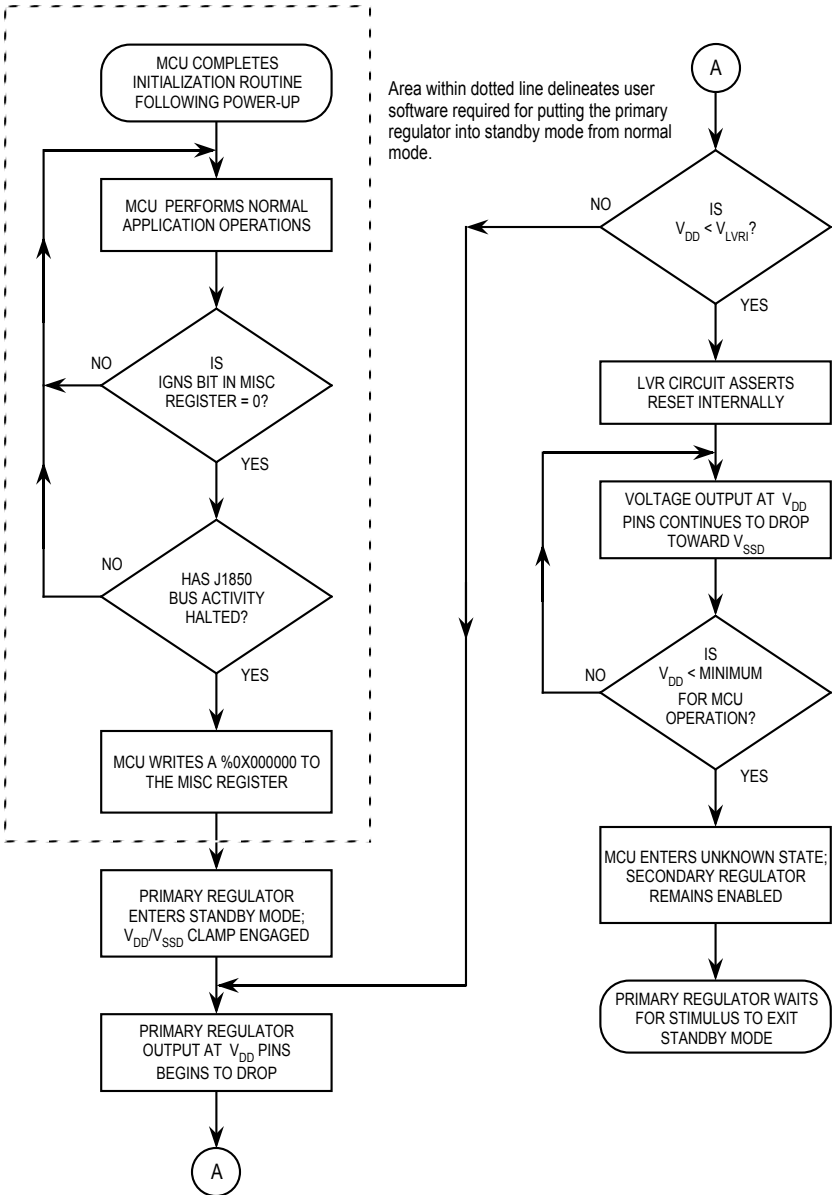
When a logic zero is written to the PDC bit, the primary regulator will go immediately into standby mode, the  $V_{DD}$  to  $V_{SSD}$  clamp will be enabled, and the power consumption of the MCU will be reduced significantly. Figure 7 illustrates the sequence which occurs when the primary regulator is put into standby mode by the CPU through software.

## Exiting Standby Mode

Once the primary voltage regulator has been put into the standby mode through software, it can only exit the standby mode and return to the normal operating mode after the detection of a rising edge at the  $V_{IGN}$  pin or, as in the automotive circuit example, following the detection of activity at the BUS pin. Once either of these two events occurs, the primary regulator's exit from standby mode is identical to the exit from standby mode after a power-up of the MCU, so the same software routine can be used. Refer to Figure 8 for an illustration of this sequence.



**Figure 6. Voltage Regulator Initialization Flowchart**



**Figure 7. Standby Mode Entry Flowchart**

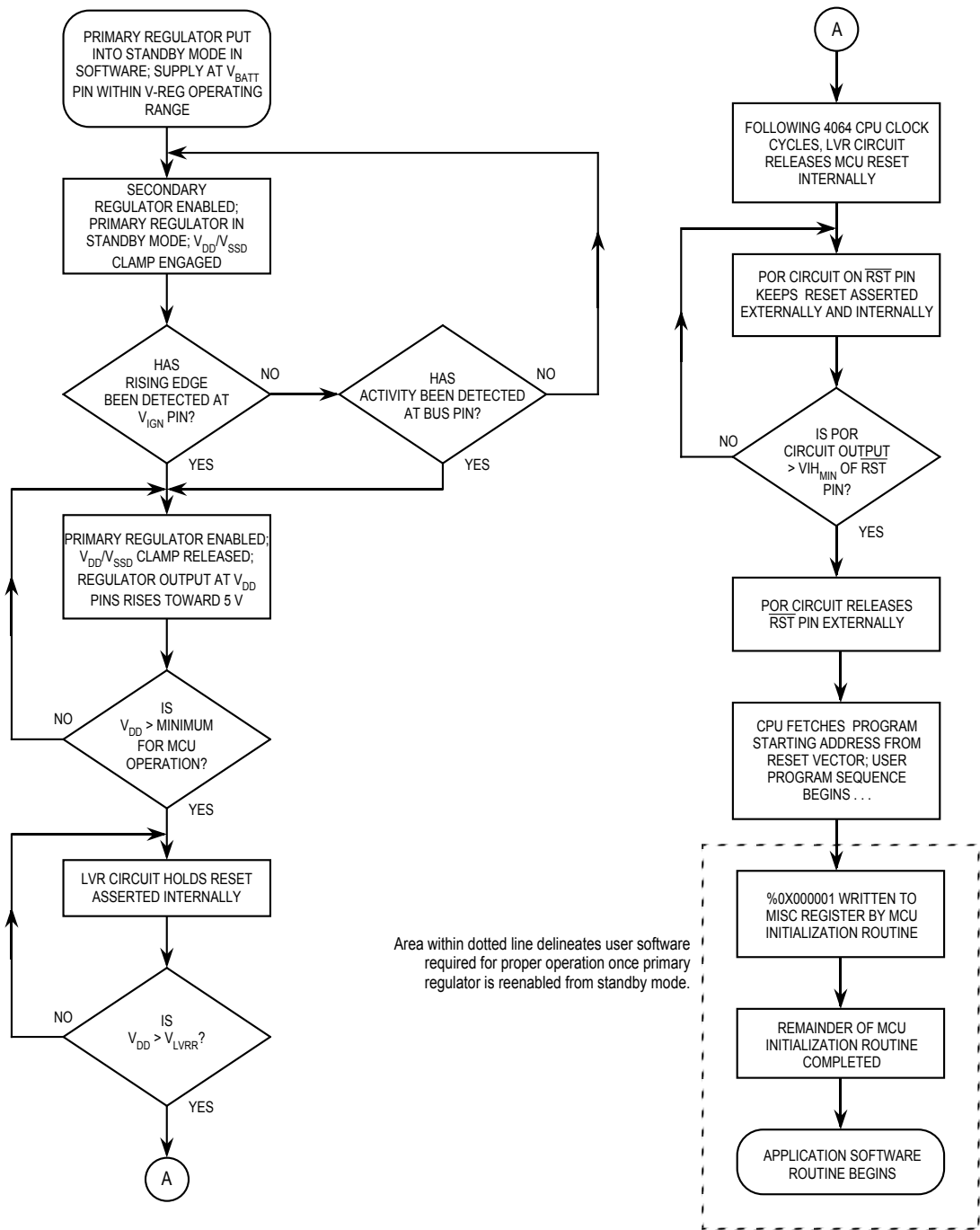


Figure 8. Exiting Standby Mode Flowchart

## CONCLUSION

The M68HC05 Family on-chip voltage regulation system is a significant step in technology integration, allowing the user to maintain application functionality while reducing chip count and printed circuit board area. As of the publication date of this application note, this voltage regulator is available only on the MC68HC705V8 and the MC68HC05V7. However, it will undoubtedly see wide-spread use in future M68HC05 and M68HC08 CSIC designs.

The power supply control and configuration information which is described herein outlines the operation of the voltage regulator as it has been implemented on the MC68HC05V7 and the MC68HC705V8. Future implementations may function differently or be specified over a different operating range. For information on the use of this voltage regulator as implemented on any subsequent members of the M68HC05 MCU Family, refer to the applicable technical documents.



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