AN11730

PTN5100 PCB layout guidelines

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Document information

Info	Content
Keywords	PTN5100, USB PD, Type C, Power Delivery, PD Controller, PD PHY
Abstract	This document provides a practical guideline for incorporating the USB Type C Power Delivery (PD) PHY layout into PCB designs.

Revision history

Rev	Date	Description
1	20150924	Initial version

Contact information

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1. Introduction

This document provides a practical guideline for incorporating the USB Type C Power Delivery (PD) PHY layout into a Printed Circuit Board (PCB) design.

These are general guidelines related to the layout of the PTN5100 only and not the power supply unit that can deliver up to 100 W across the type C cable. The PTN5100 is used to control the power switching devices (FETs, load switches…), and the power supply is responsible to generate the power rails that switch into VBUS.

2. PTN5100 interconnection PCB layout

PTN5100 is a 20 pin device and the layout guidelines below group them into separate groups depending on the function of the pins.

2.1 SPI Host Interface

2.1.1 Clock Signal Routing

PTN5100 supports SPI clock as high as 30 MHz. The rising and falling edges of the clock signal tend to be very short, therefore, the standard signal integrity PCB layout rules should be incorporated for reliable data transfer on the SPI bus. The following recommendations should be taken into account when routing the clock signal.

- The spacing between the clock trace should be three to four times away from other signal to minimize cross talk to keep the clock clean from noises.
- Minimize the use of vias to reduce PCB trace impedance changes that would create signal reflection.
- Route clock trace with controlled impedance, normally a 50 ohm PCB trace.
- The clock signal should be routed straight and avoid any sharp bend that creates signal reflection.

2.1.2 Data Signal Routing

- The SPI data in and data out signals should be routed with identical length as the clock signal. This will keep the propagation delay the same between the clock and the data lines to ensure reliable data transfer on the SPI bus.
- The data signal should be routed with the same controlled impedance as the clock signal - 50 ohm.
- Avoid any sharp bend and route the signal at 45 degree angle instead.

2.2 FET controls

The power switching device such as power FETs or load switches are controlled directly by PTN5100. Even though these power switching devices must handle current of 5 A or more, the control signals carry a few mA or less and they are just static signals (just on and off).

When the power switching devices are in the off state, these signals might have high voltage transition on them when the cable is plugged in. Keep these signals three to four times the width of the PCB trace away from other traces.

2.3 CC1 and CC2

These signals are used as the communication channels between two USB PD devices. They are also being used to deliver power (VCONN) to a type C cable's imbedded electronic if they are not used as the communication channel.

- The spacing between CC1 and CC2 traces should be three to four times away from other signal to minimize cross talk to keep these signals clean from noises.
- Follow SPI clock and data routing to avoid signal reflection
- VCONN current can be as high as 1.2 A (6 W), therefore, these PCB traces must be designed to handle this much current. PCB trace width of more 20 mil is recommended if the standard 1Oz copper pour is used.

2.4 VCONN_IN

- VCONN_IN is the power supply that is used to provide power to power cable. To avoid high frequency noise signal from coupling into the electronic circuit in the cable, a 100 pF and a 0.1 uF capacitors are recommended to bypass this pin.
- Follow the placement recommendation in 2.5 to place these decoupling capacitors.
- VCONN current can be as high as 1.2 A (6 W), therefore, this PCB trace must be designed to handle this much current. PCB trace width of more 20 mil is recommended if the standard 1 Oz copper pour is used.
- Keep VCONN_IN trace away from any high speed signal. The rule of three to four times the trace spacing from another signal should be applied.

2.5 POWER SUPPLY PINS – VIO and VDD

- PTN5100 has two power supply input pins – VIO is the supply for the I/O ring and VDD is the supply for the device's internal circuitries. Use one 0.1 uF and one 0.01 uF ceramic capacitors (0603 or 0402 size) to decoupling each supply pin. The coupling capacitors should be places as close as possible to each supply pin, this will minimize the inductive resistance creates by the length of the PCB trace.
- The routing of the power supply traces from the package pin to the decoupling capacitors should be short, and wide. Each capacitor should have its own via to the ground plane. Avoid sharing the same ground via between the two capacitors.

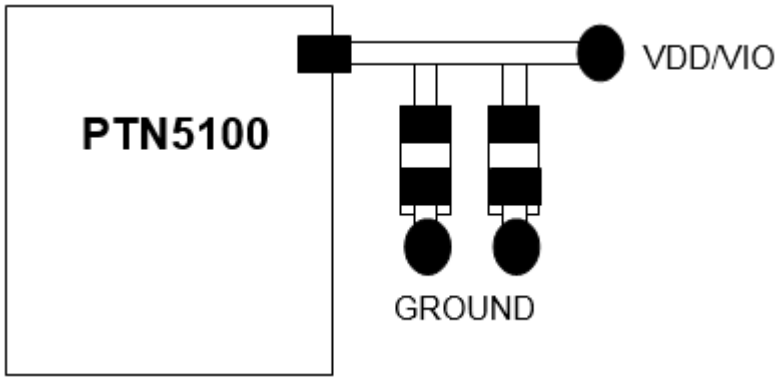

Fig 1. Power supply pins

2.6 V_MCUPWR

V_MCUPWR comes from the PTN5100 internal LDO to provide power to the external microcontroller which acting as a host to the PTN5100.

- To avoid high frequency noise signal from coupling into external microcontroller, a 2.2 uF and a 0.1 uF capacitors are recommended to bypass this pin.
- Follow the placement recommendation in 2.5 to place these decoupling capacitors.
- The PCB trace to the external microcontroller should be as wide as and direct as possible.

2.7 BYPASS

- This is the PTN5100 internal power rail bypass pin. A low ESR 2.2uF ceramic capacitor is required. A ceramic capacitor such as Murata GRM188R61C225KE15D or equivalent should be used.
- Place the bypass capacitor as close as possible to the pin.
- Follow the recommendation in 2.5.

2.8 HWQFN/HVQFN exposed center pad solder lands

The center pad under the device is used as the device's ground pin, as well as thermal relieve. This center pad must be connected to the system ground.

During reflow soldering, solder paste melts and gas or trapped air is released, causing splattering or solder balling. Solder balling and splatter can be minimized if the solder paste is printed as a number of individual dots, instead of one large deposit, and if the solder paste is kept at a sufficient distance from the edge of the solder land.

The solder paste pattern area about should cover 30 % of the solder land area. When printing solder paste on the exposed die pad solder land, the solder paste dot area should cover no more than 20 % of this solder land area. Furthermore, the paste should be printed away from the solder land edges. This is illustrated in figure below; the solder paste pattern area lies within the boundary indicated by the red line and it is divided by the entire solder land area.

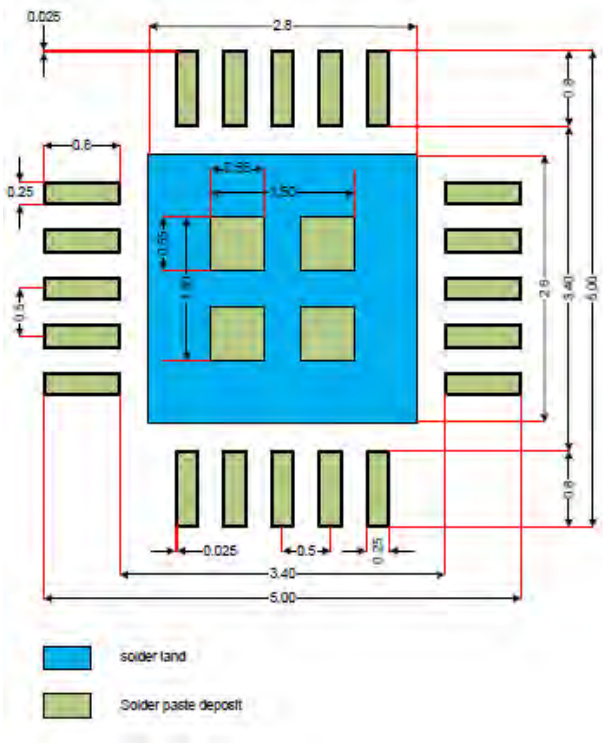

Fig 2. Solder paste dot area

3. Summary

- Standard signal integrity PCB layout should be applied to minimize cross talk, signal reflection.
- VCONN and CC1/CC2 PCB traces must be designed to carry at least 1.2 A of current.
- The PTN5100 center pad is utilized as the ground pin, therefore, it must be connected to the system ground.
- The center pad should be divided into smaller pads to minimize soldering issue.
- A low ESR ceramic capacitor is required on the BYPASS pin.

4. Reference

1. USB PD Specification Revision 2

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6. List of figures

7. Contents

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