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A Ku band quad LNB reference design based on TFF1044HN

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Document information

Info	Content
Keywords	TFF1044, BFU910F, Quad LNB, DVB-S, Ku band to L-band Down Converter, FIMOD IC, Ku Band
Abstract	This application note describes a reference design based on TFF1044HN and BFU910, including the design details and the test results.

Revision history

Rev	Date	Description
1	20150717	First publication

1. Introduction

NXP Semiconductors developed two new products for the Satellite LNB market, a fully integrated Quad Down-Converter IC (TFF1044HN) and an Ultra-Low Noise Bipolar transistor in SiGe technology (BFU910F). With these products the currently discrete Quad LNB market can be addressed with following benefits:
- design time reduction
- PCB size reduction
- decreased costs of ownership, alignment free concept

To support the Quad LNB market a reference design was implemented in NXP, which is called the NXP Quad in this document. The performance targets and followed approach can be found in this Application Note. Also actual performance, bill of materials, mechanical drawings and artwork files are given in this document to enable a head start for new integrated Quad designs!

2. The NXP Quad

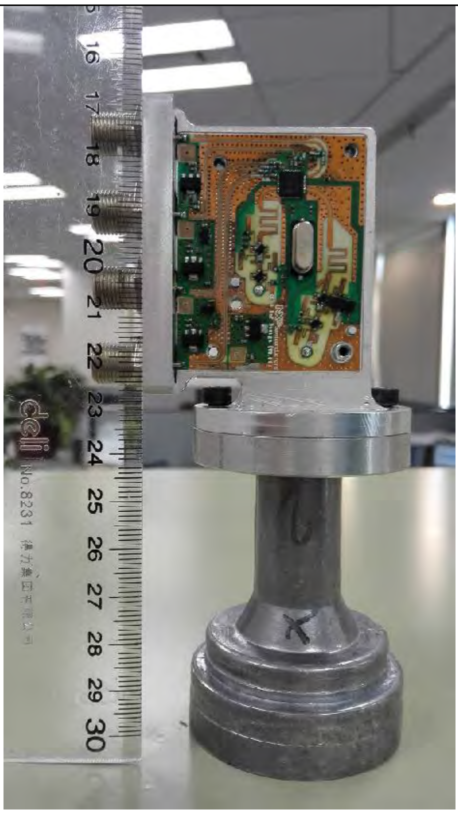


Figure 1 The NXP QUad

2.1 Product definition

Before starting the integrated reference LNB design a feasibility study was done. The market to address was investigated and electrical as well as mechanical targets were set, as listed in the sections below.

2.2 Approach

As some electrical performance parameters can be defined differently, and uncertainty on the reference planes may arise, a “benchmark” discrete Quad LNB (called benchmark LNB in this document) was bought from the market. This was done in order to make a performance comparison with NXP Quad Ref. LNB on the main performance parameters. Also the benchmark LNB as well as the NXP Quad were put on a dish antenna and the received live signal quality were measured to compare the final performance.

2.3 Functional requirements

The Quad LNB has two orthogonal mode inputs, implemented in Ku band circular waveguide. The two RF input signals are amplified by two cascaded LNA stages and are mixed down from Ku to L-band by 9.75 GHz and 10.6 GHz LO’s.

On the four available IF outputs, implemented in F-type connectors, each RF polarization as well as band can be accessed. The Quad Ref. LNB has internal regulators and can be fed from either one or multiple IF’s over the coaxial cable, by applying bias Tees inside the Quad Ref. LNB.

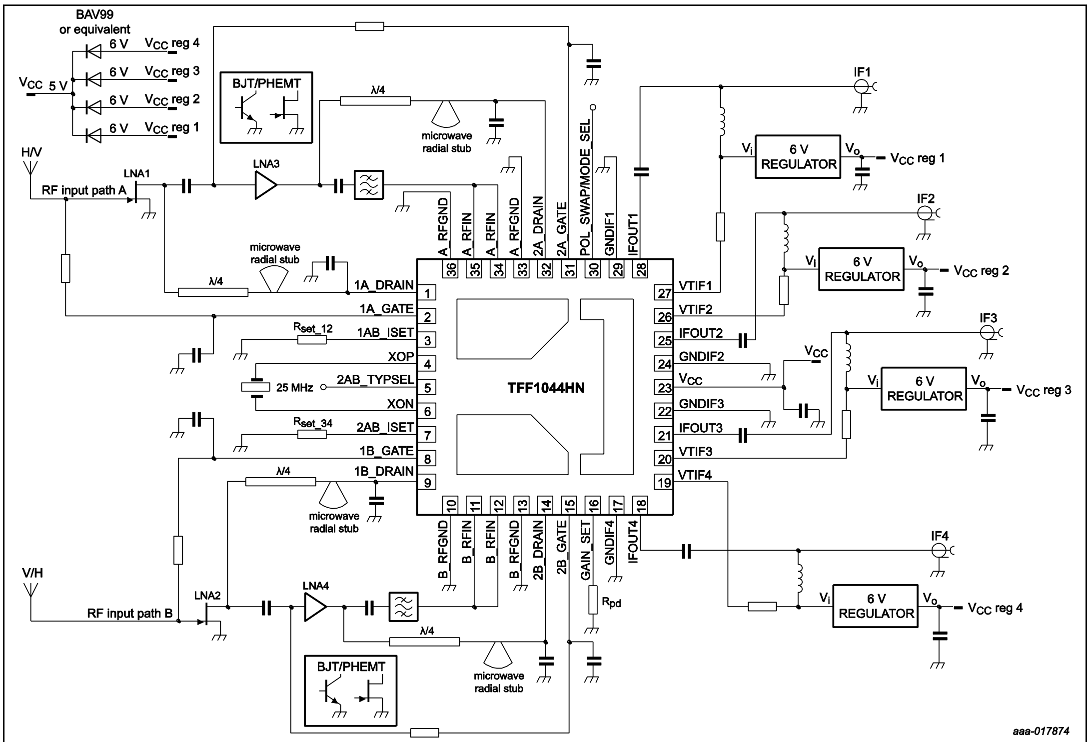


Figure 2 Block diagram for integrated Quad LNB

Apart from the TFF1044 four LNA stages, four linear regulators, four diodes, one 25 MHz crystal and some passives are required.

2.4 Electrical requirements

The electrical requirements are mostly operator dictated, for NXP Quad Ref. LNB the Astra specifications were taken as reference. These are listed in the table below.

Table 1 Target specification

Parameter		Value	Unit	Comments
Input Frequency	Low Band	10.70 to 11.70	GHz	
	High Band	11.70 to 12.75	GHz	
Output Frequency	Low Band	950 to 1950	MHz	
	High Band	1100 to 2150	MHz	
Local Oscillator Frequency	Low Band	9750	MHz	Offset less than ±1MHz
	High Band	10600	MHz	
RMS Phase Jitter		2.5 (max.)	°	Integrated from 10kHz to 13MHz
Conversion Gain		60 (typ.)	dB	
Gain Ripple		5 (max.)	dB	over complete low or high band
Noise Figure	Low Band	1.1 (typ.)	dB	Comparable with benchmark LNB
	High Band	1.3 (typ.)	dB	
3rd Order Intermodulation		10 (min.)	dBm	
Output Return Loss (75 Ω)		8 (min.)	dB	
Cross Polar Rejection		20 (min.)	dB	
In-band Spurious		-60 (max.)	dBm	Comparable with benchmark LNB
Current Consumption	One IF-port on	180	mA	
	All IF-ports on	250	mA	

2.5 Mechanical requirements

Discrete quad LNB usually employs two PCBs and the PCB size is much bigger. For example, the benchmark LNB has two PCB with the total size of 4500mm^2 (65*45mm and 35*45mm respectively).

The Quad Ref. LNB should be built with a single (Rogers) PCB. The size should be as small as possible, however mechanical dimensions are linked to the minimum space between the IF (F-type) connectors. Minimum spacing of those, in order to enable access to the four IF cables, is 16 mm. The final PCB size is decided as 2000mm^2 (50mm long and 40mm wide) and is nearly 45% of the total PCB size of the benchmark LNB.

The Quad Ref LNB will be equipped with a flange (circular waveguide diameter 17.6 mm), a feed-horn with flange will be supplied but customers can use their own feed-horn design by un-screwing this.

2.6 The NXP Quad, design considerations

Given the required overall conversion gain the choice for two cascaded LNA stages (per polarization) is dictated. First LNA stage chosen is a common used Pseudomrphic High Electron Mobility Transistor (pHEMT) for excellent NF. Second stage is NXP Bipolar Junction Transistor (BJT) BFU910F, this transistor has approximately 1.5 dB more gain compared to typical pHEMT devices, which compensates nicely for the NFmin. (See also section 5.1.1)

TFF1044 provides bias for both the first stage and the second stage. The first stage is for pHEMT with adjustable bias current. The second stage is selectable between pHEMT and BJT also with adjustable bias current. NXP BJT's like BFU910F have a supply current advantage over pHEMT devices of approximately 3mA per LNA.

Band-pass filters were applied to increase the overall image rejection (3 section hairpin filters). With this filters an average image rejection at PCB level of 46 dB is realized.

The supply topology chosen is to use four linear regulators (6 Volt), one per IF path, and combining their outputs by simple diodes.

The PCB design target to minimize the PCB size with the premise of good RF performance and safe IF connector clearance. (See also section 5.4).

3. The NXP Quad, measurement results

3.1 Parametric results, main parameters

This is an overview of the typical values measured for the main parameters by comparison with that of the benchmark LNB. For more detailed results please see section 7.

Table 2 Measured performance of the NXP Quad vs the benchmark LNB

Parameters		NXP Quad	Benchmark LNB	Requirements	Unit
LO accuracy	Low Band	0.1	0.3	±1.0 (max.)	MHz
	High Band	0.1	0.3		MHz
RMS Phase Jitter		1.4	0.2	2.5 (max.)	°
Conversion Gain		60	60	60 (typ.)	dB
Gain Ripple		3	3	5 (max.)	dB
Noise Figure	Low Band	1.0[1]	1.0	1.1 (typ.)	dB
	High Band	1.0[1]	1.1	1.3 (typ.)	dB
OIP3		12	10	10 (min.)	dBm
Cross Polar Rejection		25	28	20 (min.)	dB
In-band Spurious		-65	-60	-60 (max.)	dBm
Current Consumption	One IF-port on	159	153	180 (max.)	mA
	All IF-ports on	214	213	250 (max.)	mA

[1] : Noise Figure measured in one polarization, shows the potential of the concept.

3.2 Measurement results live signal Quality

Measured parameters on modulated signals were the signal strength, Carrier to Noise Ratio (C/N), Modulation Error Rate (MER) and for the 8-PSK signals the Link Margin (LKM).
In the results one cannot differentiate the NXP Quad from the benchmark LNB's. For detailed results see section 6.8.

3.3 Conclusions

The Quad LNB reference design has shown to be competitive compared to benchmark LNB's. The benefits for OEM's / ODM's are clearly in the PCB size reduction, design time reduction and costs of ownership. This reference design can also serve as a starting point for derivatives for alternative Quad / Quattro / IP LNB markets.

4. Key-components, product description

4.1 TFF1044HN

TFF1044HN is an integrated down-converter for use in universal quad and quattro

Low Noise Block (LNB) convertors in 10.70 GHz to 12.75 GHz K_u band satellite receiver systems.

The device incorporates required mixers, Local Oscillators (LO), Intermediate Frequency (IF) amplifier stages, IF switch matrix, Voltage and Tone detection for polarity and band switching and pHEMT bias control for a pair of two-stage-LNA (as shown in Figure 3). It can be used to create an alignment free product with two RF inputs and four IF outputs and enables PCB size reduction.

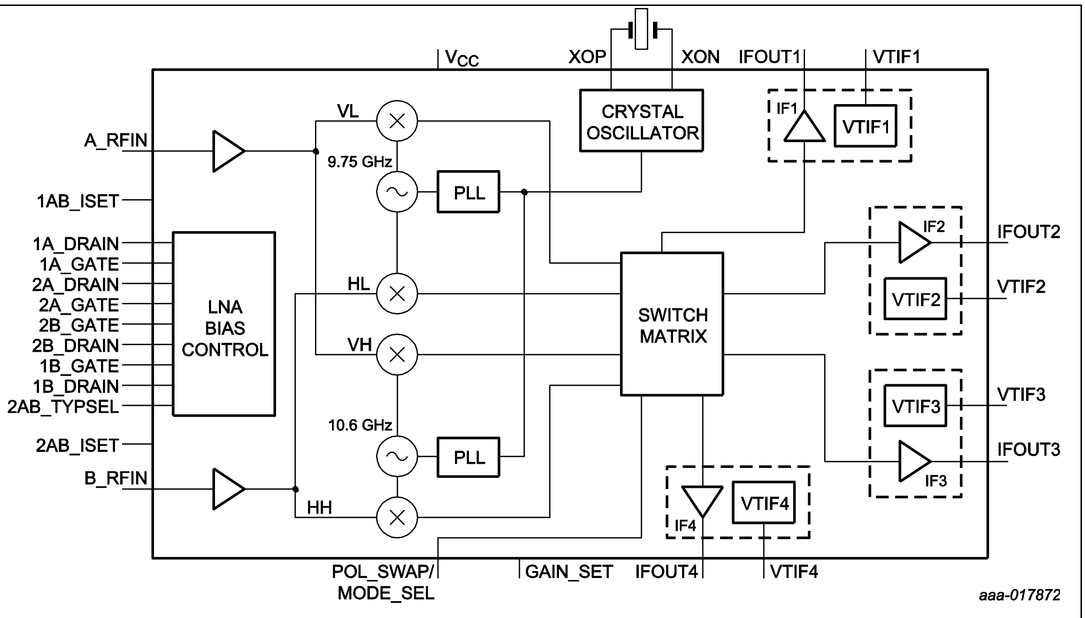


Figure 3 TFF1044 block diagram

Apart from the TFF1044, only a few external components, including the LNA stages, a 25 MHz crystal, voltage regulator(s), two diode-pairs and some passive circuitry is required to complete a quad LNB. The number of components is significantly reduced compared to discretely build quad/quattro LNB's.
The TFF1044HN offers some degree of flexibility for ease of application, through the use of its control pins. The settings of these pins are introduced in this section so that readers can be easier to understand the design consideration which is described in Section 5.1.

- **POL_SWAP / MODE_SEL:** This pin serves as polarization swap selection pin to enable PCB routing with optimum (none crossing) Ku band RF tracks.
The vertical and horizontal polarizations are assigned to the RF path A and RF path B inputs according to Table 1. The setting for quattro mode operation is also given in the same table.

Table 1 Polarity swap / mode selection settings

Connection of POL_SWAP/MODE_SEL (Pin 30)	Mode	Polarity	
		RF A (pin 35)	RF B (pin 11)
GND	quad	horizontal	vertical
Float	quad	vertical	horizontal
GND via 100 kΩ pull-down resistor	quattro	N/A	N/A

- **GAIN_SET:** This pin provides a three levels adjustable gain.
TFF1044 has selectable gain states in order to have freedom to vary the overall LNB gain. The conversion gain can be set to 30dB, 33dB or 36dB by the external connection of GAIN_SET pin, which is shown in Table 2.

Table 2 Conversion gain settings

Connection of GAIN_SET (Pin 16)	Gain Mode	Typical Conversion Gain
GND	low	30 dB
Float	medium	33 dB
GND via 100 kΩ pull-down resistor	high	36 dB

The gain of the TFF1044HN quad LNB with two-stage LNA is typically 55 to 61dB by different gain setting. For even higher conversion gain, the 3rd stage of LNA has to be employed.

- **2AB_TYPSEL:** This pin enables different biasing schemes for the second stage LNA depending on the preferred technology, BJT or pHEMT.

TFF1044 leaves the flexibility of different transistor type of the 2nd stage LNA to the user, and **Table 3** presents how to set it by 2AB_TYPSEL pin.

Table 3 Second stage LNA type selection settings

Connection of 2AB_TYPSEL (Pin 5)	Type of the 2nd stage of LNA	
	RF path A	RF path B
GND	pHEMT	pHEMT
Float	BJT	BJT

- **1AB_ISET / 2AB_ISET:** These pins set the current of the 1st and the 2nd stage of LNA respectively.

The parameters spread of the LNA transistors, whether pHEMT or BJT, depends on the current of the Drain (of pHEMT) or Collector (of BJT). So it is more stable to use a current source instead of voltage source to supply the transistor. TFF1044HN is capable of providing such current sources for the transistors as the 1st and 2nd stages of the LNAs for both polarities.

TFF1044HN allows the user to set the current of the 1st and 2nd stage separately. The typical drain current of pHEMT is 10mA, and correspondingly, a 22kΩ pull-down resistor should be connected to 1AB_ISET /2AB_ISET. While the typical current of BFU910F is 6-7mA, and the corresponding resistor at 2AB_ISET is 33kΩ.

4.2 BFU910F

BFU910F is an NPN silicon germanium Radio Frequency (RF) BJT for high speed, low noise applications in a plastic, four-pin dual-emitter SOT343F package.

BFU910F has the characterization of low NF and high gain. At 12GHz, The minimum noise figure (NFmin) is 0.65 dB and the maximum stable gain (MSG) is 14.2 dB.

In Ku band application, BFU910F is usually biased at 2V/7 mA. Compared with pHEMT, BFU910 has the merits of lower current, no negative voltage needed, higher gain, easier for wide-band matching.

In the quad LNB reference design, BFU910F is used as the second stage LNA. Although its individual NFmin is slightly higher than some pHMET, the higher gain of BFU910F makes the overall NF even better.

5. Design

5.1 General Consideration

5.1.1 Gain and NF simulation

The ADS schematic of the Front End (FE) of the NXP Quad is given in Figure 4. The FE includes two stages of LNA, a Circular Waveguide (CWG) with input matching, intermediate stage matching and output circuits (output matching, Band Pass Filter (BPF) and 50Ω transmission-line).

NE3503M04 and BFU910F are employed as the 1st and 2nd stage LNA respectively.

The Circular Waveguide (CWG) is used as the input interface, and the parameters of the CWG with input matching circuits is extracted and stored in the S4P model in the schematic in Figure 4.

The models of the intermediate matching and the output circuits of the FE are simulated by Momentum.

Based on the simulation of the FE, which is shown in Figure 5, the overall gain and NF of the LNB (FE+TFF1044HN) is calculated and shown in Figure 6.

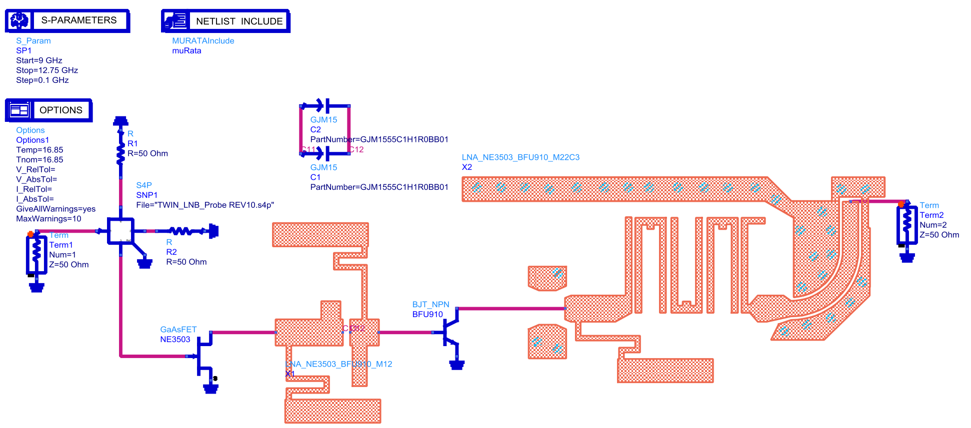


Figure 4 FE circuits for ADS schematic simulation

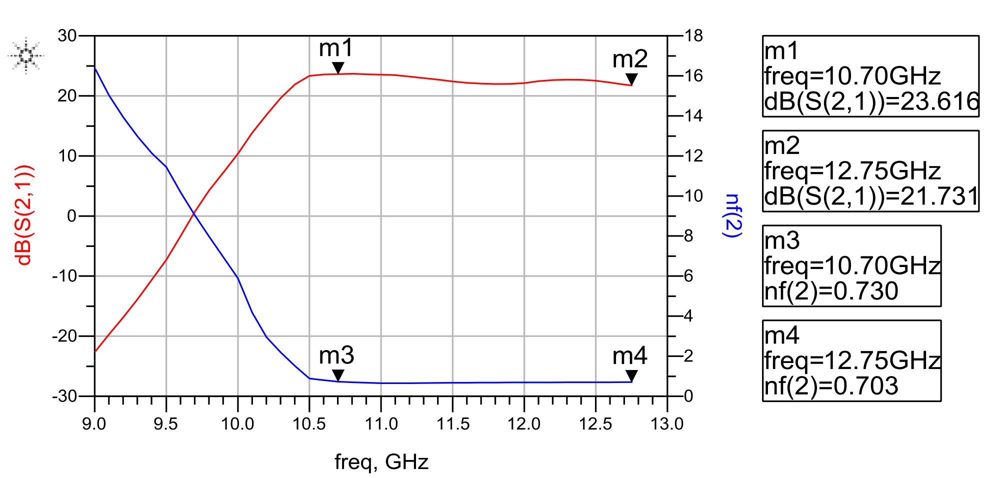
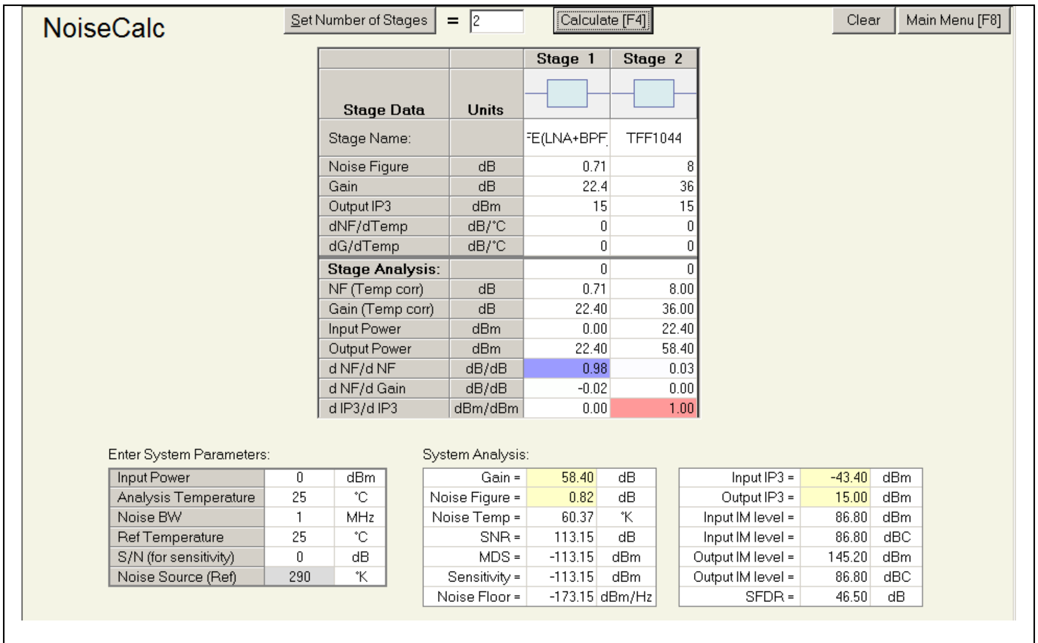


Figure 5 FE Gain and NF simulation:
NF is 0.730dB at 10.7GHz and 0.703dB at 12.75GHz
Gain is 23.616dB at 10.7GHz and 21.731dB at 12.75GHz



Stage Data	Units	Stage 1	Stage 2
Stage Name:		FE(LNA+BPF	TFF1044
Noise Figure	dB	0.71	8
Gain	dB	22.4	36
Output IP3	dBm	15	15
dNF/dTemp	dB/°C	0	0
dG/dTemp	dB/°C	0	0
Stage Analysis:		0	0
NF (Temp corr)	dB	0.71	8.00
Gain (Temp corr)	dB	22.40	36.00
Input Power	dBm	0.00	22.40
Output Power	dBm	22.40	58.40
d NF/d NF	dB/dB	0.98	0.03
d NF/d Gain	dB/dB	-0.02	0.00
d IP3/d IP3	dBm/dBm	0.00	1.00

Enter System Parameters:

Input Power	0	dBm
Analysis Temperature	25	°C
Noise BW	1	MHz
Ref Temperature	25	°C
S/N (for sensitivity)	0	dB
Noise Source (Ref)	290	°K

System Analysis:

Gain =	58.40	dB
Noise Figure =	0.82	dB
Noise Temp =	60.37	°K
SNR =	113.15	dB
MDS =	-113.15	dBm
Sensitivity =	-113.15	dBm
Noise Floor =	-173.15	dBm/Hz

Input IP3 =	-43.40	dBm
Output IP3 =	15.00	dBm
Input IM level =	86.80	dBm
Input IM level =	86.80	dBC
Output IM level =	145.20	dBm
Output IM level =	86.80	dBC
SFDR =	46.50	dB

Figure 6 Simulated Gain & NF of the whole LNB:
The NF is 0.82dB and the Gain is 58.4dB

5.1.2 TFF1044 configuration

Regarding to the configuration of the NXP Quad:

1) High gain mode: Gain_SET (pin 16) is pull-down by a 100kΩ resistor
2) BJT (BFU910) as the 2nd stage of LNA: 2AB_TYPSEL (pin 5) is left floating
3) RFA as vertical polarity and RFB as horizontal polarity: POL_SWAP/MODE_SEL (Pin 30) is left floating
4) The bias of the 1st stage is 2V/10mA: 1AB_ISET (pin 3) is pulled-down by a 22kΩ resistor
5) The bias of the 2nd stage is 2V/7mA: 2AB_ISET (pin 7) is pulled-down by a 33kΩ resistor f

The detailed schematic and BOM are given in Section 5.2 and Section 5.3 respectively.

5.1.3 PCB and mechanical parts

In traditional discrete quad LNB, two PCBs are usually employed because the RF crossing traces are inevitable with single PCB layout. But it is not a problem anymore in TFF1044HN based quad LNB. In the NXP Quad, single PCB solution is employed and the PCB size has been designed as small as possible:

- The length of the PCB is determined by the safe distance between the F-type connectors. Any neighboring F-type connectors must be placed at least 16mm far from each other to avoid conflicts. The minimum PCB length is 50mm: three times of the minimum safe distance plus the pads dimensions.
- The width of the PCB is determined by the geometric dimension of the distribution circuits (FEs and IF transmission lines) and safe distance between the IF transmission lines. The minimum PCB width is 40mm.

The PCB layout is presented in Section 5.4, and related assembly drawing is in Section 5.5.

The LNB has a Circular Waveguide (CWG) input interface so that the LNB can be tested both in lab and on dish. The precision of the waveguide significantly impacts the RF performance of the LNB, and its dimension is described in Section 5.6.

5.2 Schematic

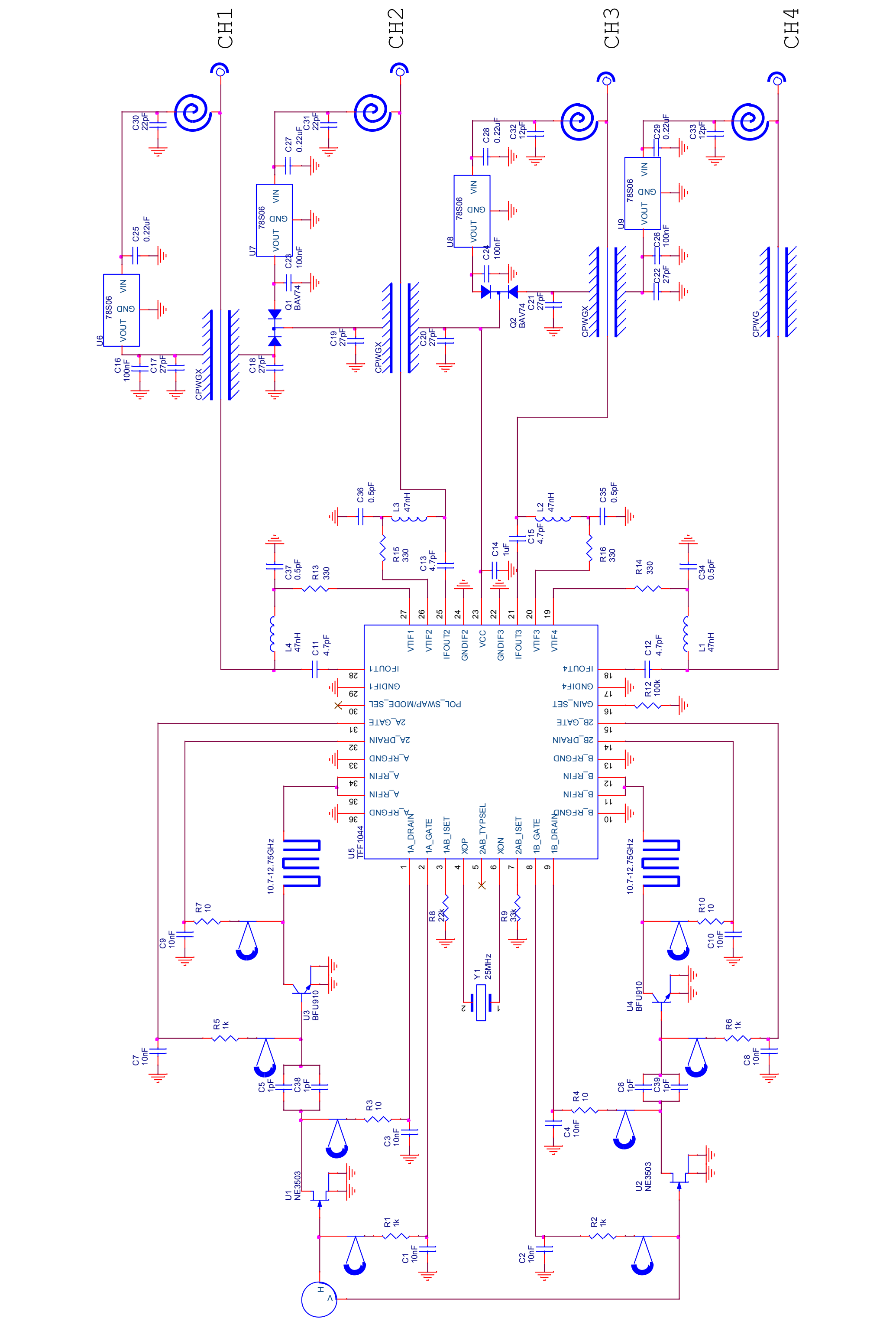


Figure 7 Schematic of NXP Quad

5.3 BOM

Table 4 Bill of material

Designator	Description	Footprint	Qty	Value	Supplier Name/type
U1,U2	HJFET	SOT343	2		Renesas-NE3503M04
U3,U4	SiGe BJT	SOT343	2		NXP-BFU910F
U5	FIMOD	SOT1359-1	1		NXP -TFF1044HN
U6,U7,U8,U9	Regulator	SOT-89	4		Silicore-78S06M
Q1,Q2	CC-Diodes	SOT-23	2		NXP-BAV74
C1, C2, C3, C4, C7, C8, C9, C10	Capacitor	0402	8	10nF	Murata-GRM155R71H103K
C5, C6, C38, C39	Capacitor	0402	4	1pF	Murata-GJM1555C1H1R0C
C11, C12, C13, C15	Capacitor	0402	4	4.7pF	Murata-GRM1555C1H4R7C
C14	Capacitor	0402	1	1uF	Murata-GRM155R61A105K
C34, C35, C36, C37	Capacitor	0402	4	0.5pF	Murata-GRM1555C1HR50B
C16, C23, C24, C26	Capacitor	0402	4	0.1uF	Murata-GRM155R71C104K
C17, C18, C19, C20, C21, C22	Capacitor	0402	6	27pF	Murata-GRM1555C1H270J
C25, C27, C28, C29	Capacitor	0603	4	0.22uF	Murata-GRM188R71E224K
C30, C31, C32, C33	Capacitor	0402	4	22pF	Murata-GRM1555C1H220J
R1,R2,R5,R6	Resistor	0402	4	1kΩ	PSA-WR04X1001FTL
R3, R4, R7, R10	Resistor	0402	4	10Ω	PSA-WR04X10R0FTL
R8	Resistor	0402	1	22kΩ	PSA-WR04X2202FTL
R9	Resistor	0402	1	33kΩ	PSA-WR04X3302FTL
R12	Resistor	0402	1	100kΩ	PSA-WR04X1003FTL
R13, R14, R15, R16	Resistor	0402	4	330	PSA-WR04X3300FTL
L1,L2,L3,L4	Inductor	0402	4	47nH	LQW15AN47NG
Y1	Crystal	HC-49XA	1	25MHz	JFVNY-HC-49XA-C16TTA-25.000MHz DYNAMIC-DMS2500016

5.4 PCB layout

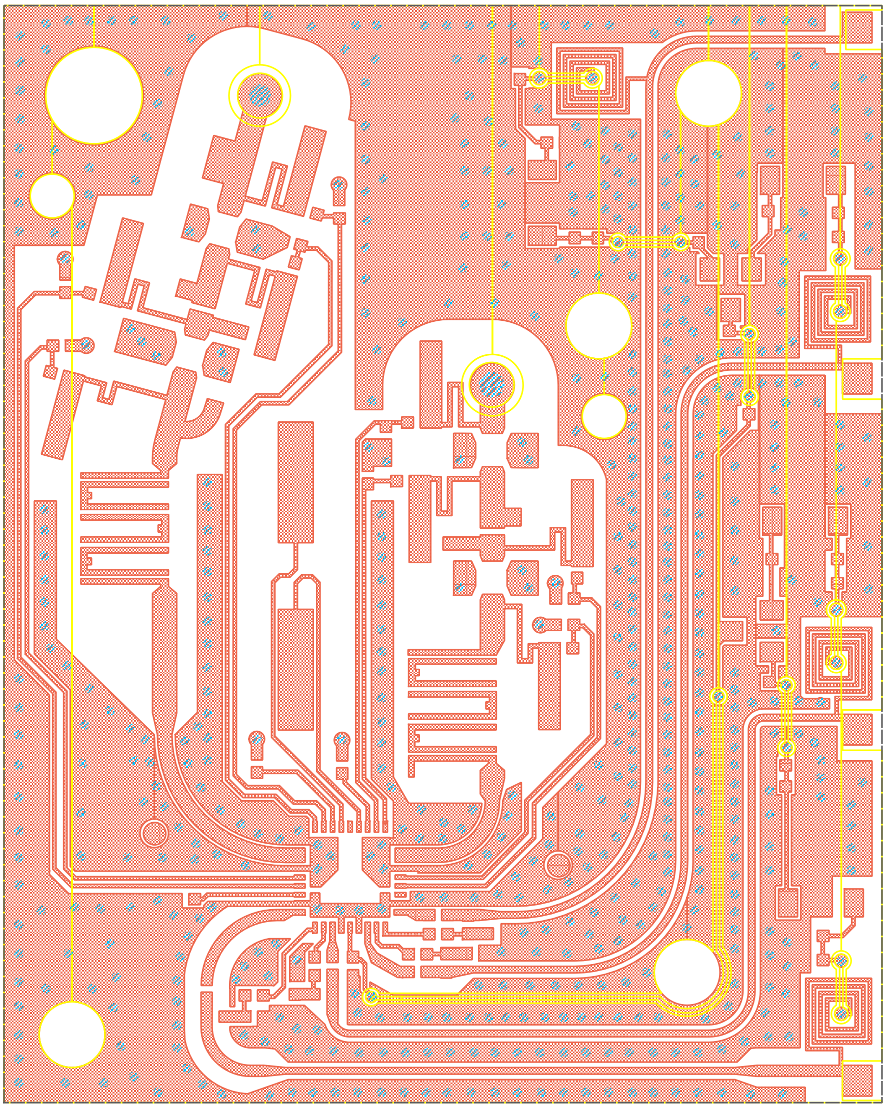


Figure 8 PCB layout

5.5 Assembly

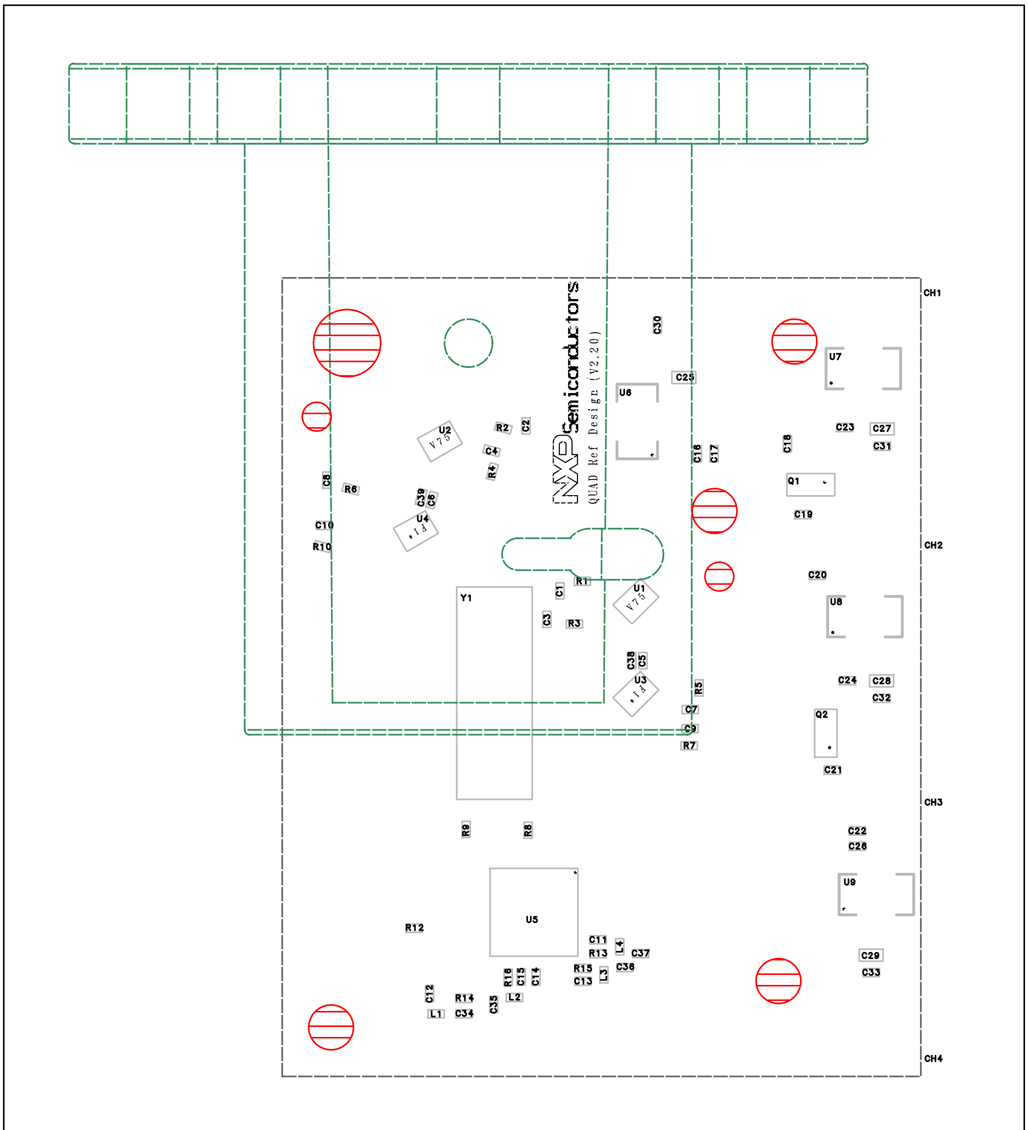


Figure 9 Assembly drawing

5.6 Mechanical drawing

The mechanical drawings of the base, cove short stick and probes are presented in Figure 10 to Figure 12. The alignment of the probes is very important to the NF of the LNB. A fixture is made to assemble the probes precisely, which is shown in Figure 13. The assembly view of NXP Quad is given in Figure 14.

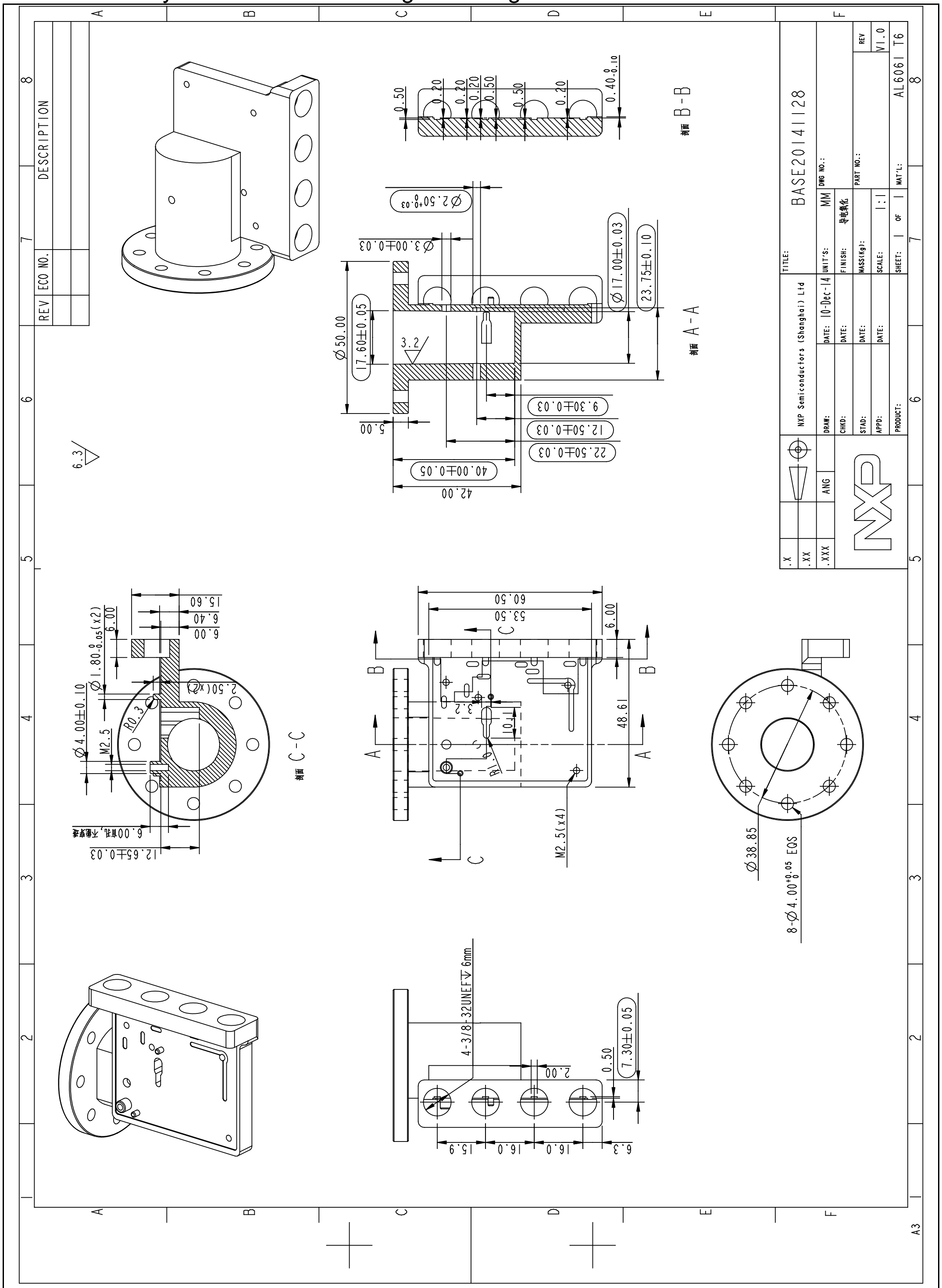


Figure 10 Mechanical drawing: Base

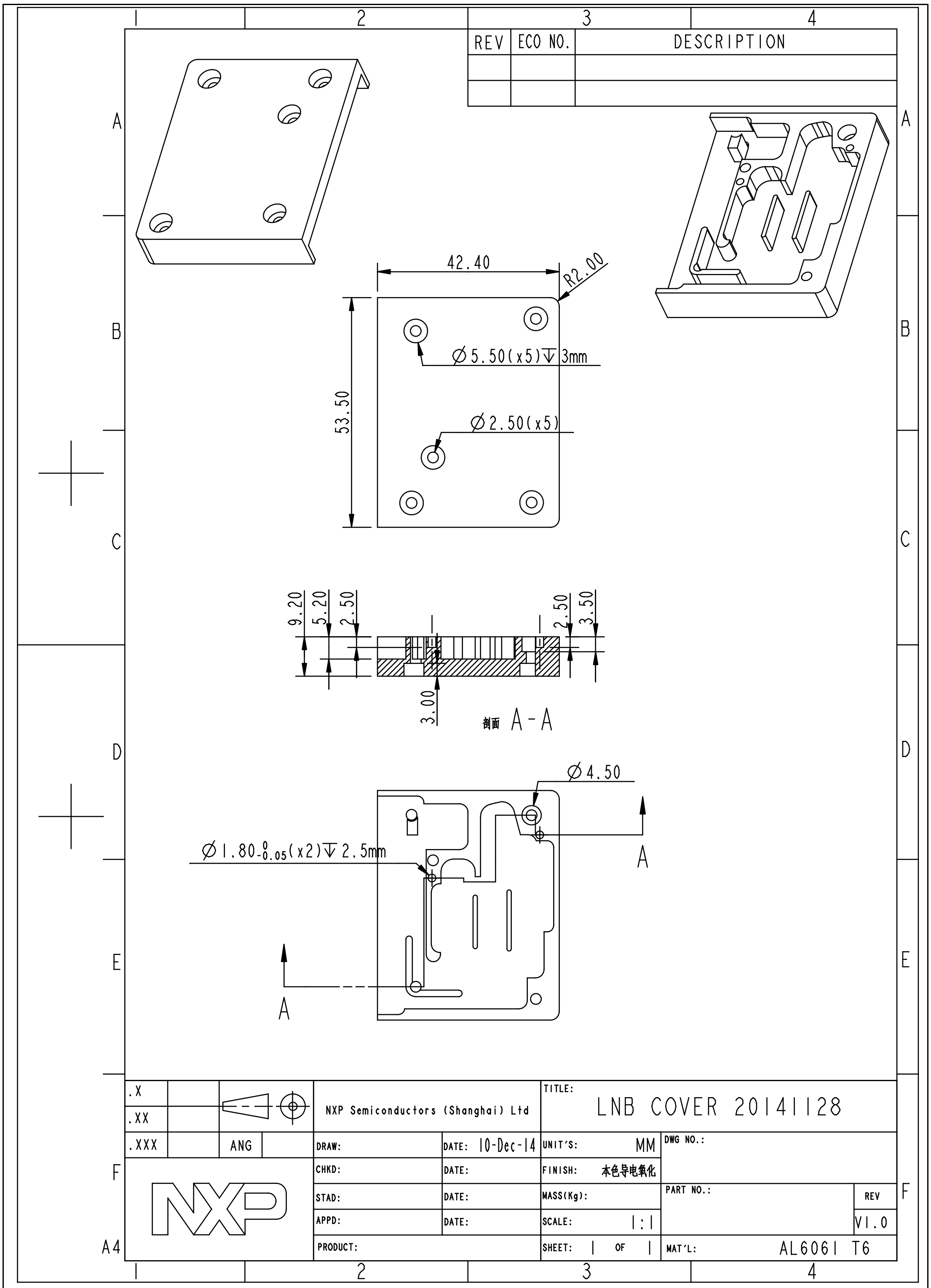


Figure 11 Mechanical drawing: cover

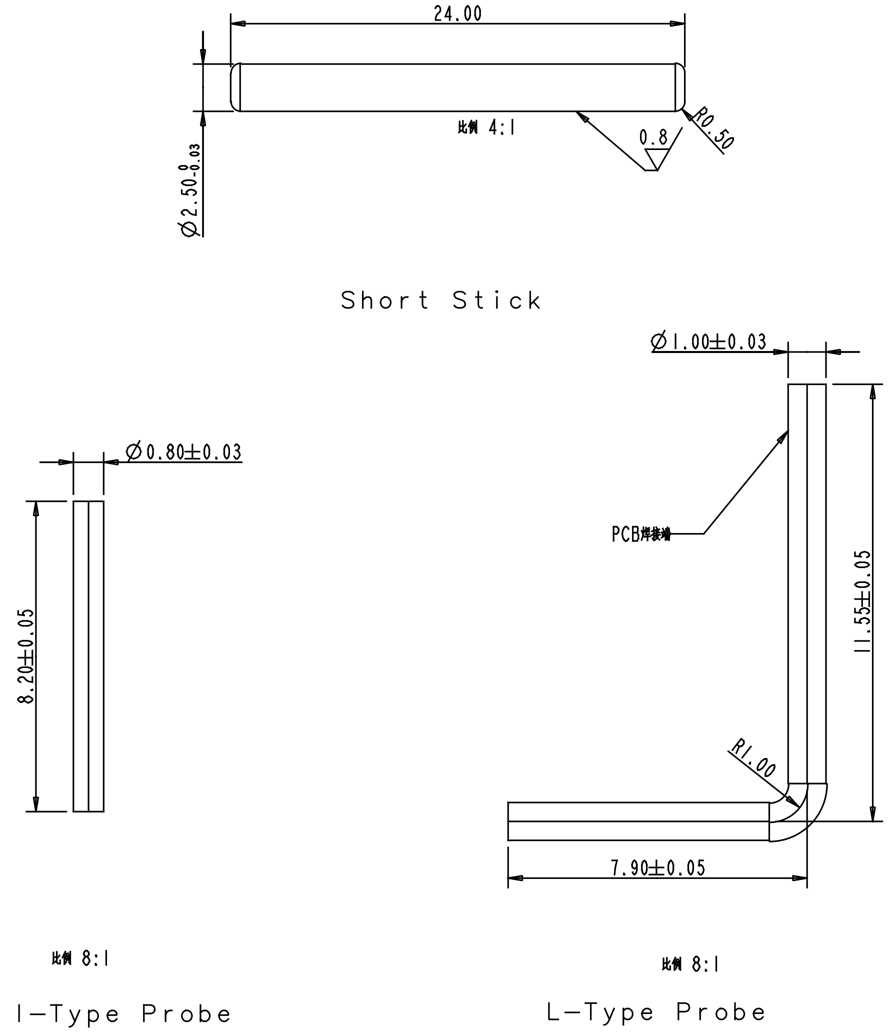


Figure 12 Mechanical drawing: short stick & probes

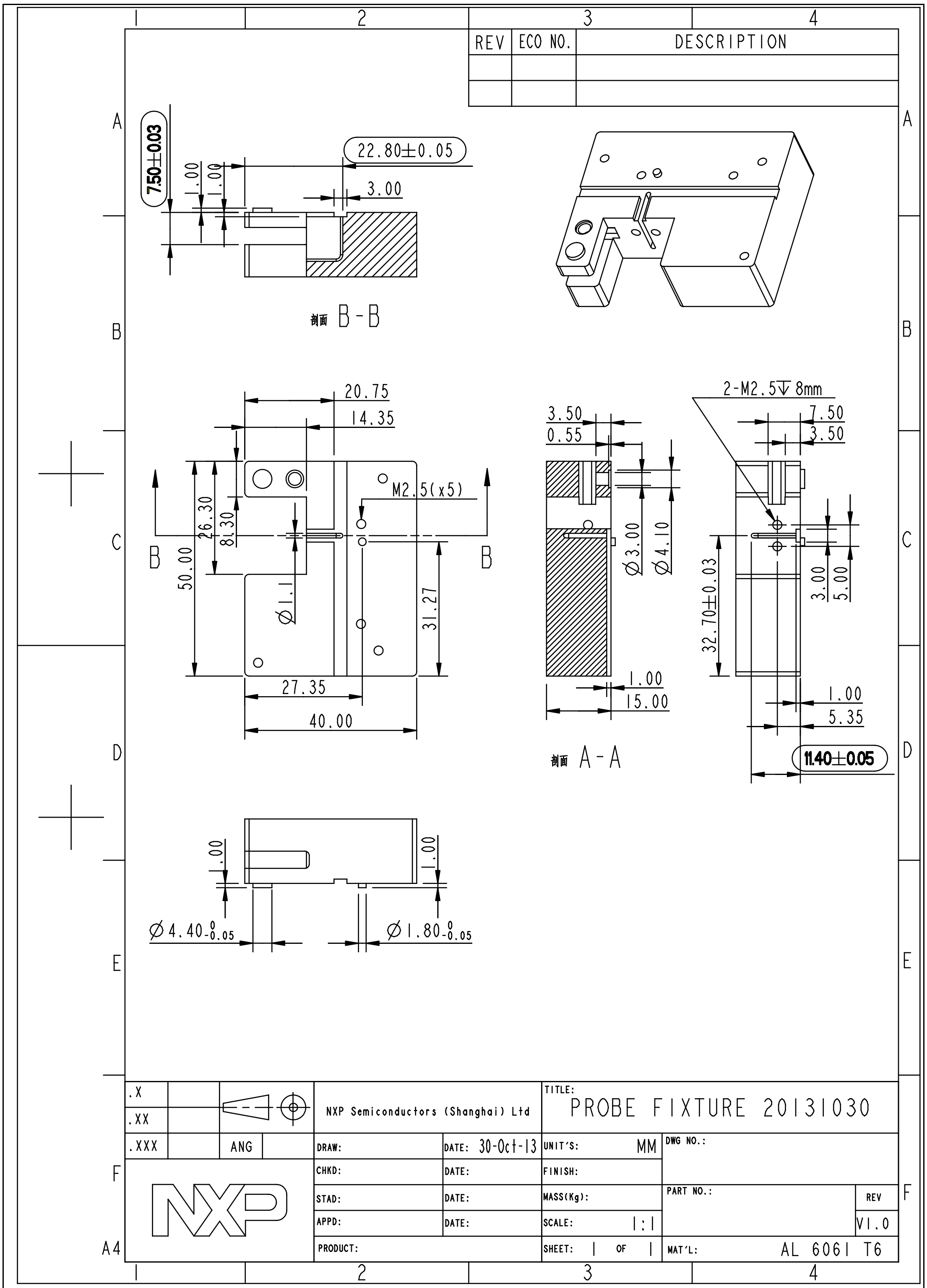


Figure 13 Mechanical drawing: Fixture

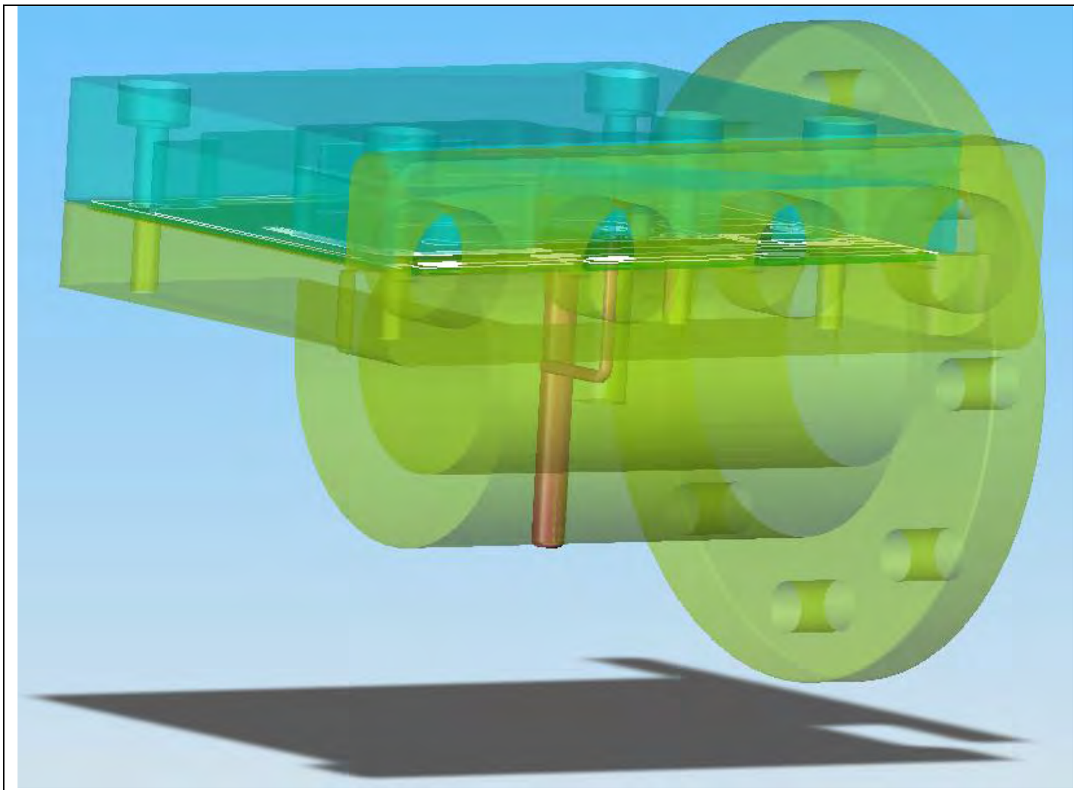


Figure 14 Mechanical drawing: assembly

6. Test Results

The NXP Quad is tested in lab for RF performance and on dish for signal quality. The electric test results are given in Section 6.1 to Section 6.7, while the signal quality test results are given in Section 6.8.

6.1 Noise Figure

The NF test setup is shown in Figure 15. The NF is tested by Rhode & Schwarz FSU spectrum analyzer with an Agilent 346A noise source.

An Orthogonal Mode Transducer (OMT) is used as the adaptor between the coaxial connector and the waveguide. The loss of the OMT, which is used in the NF test calibration is given in Figure 16.

Since the conversion gain of the DUT is about 60dB, the noise contribution of the spectrum analyzer receiver is negligible. So the Second Stage Corrected function is switched off in this test. When one IF port is under test, all the other ports are switched off to avoid the impacts due to cross talk and cross polar.

For LNB based on any Fully Integrated Mixer Oscillator Down-converter (FIMOD) IC, the harmonic of the crystal can be looked as extra noise. Different from the thermal noise, this interference is not white noise but a single spectrum. So how it impacts the system Signal Noise Ratio (SNR) is different. To evaluate the physical SNR degradation in DVB-S signal receiving system with the NXP Quad, the Resolution Band Width (RBW) is set 10MHz, which is as close to typical symbol rate of a real system as possible.

The NF of NXP Quad is typically 1.1dB, and independent on which IF port is under test as shown in Figure 17.

Figure 18 compares the NF of the NXP Quad and the benchmark LNB. Both LNBs are measured under the same test condition, and their NF are comparable.

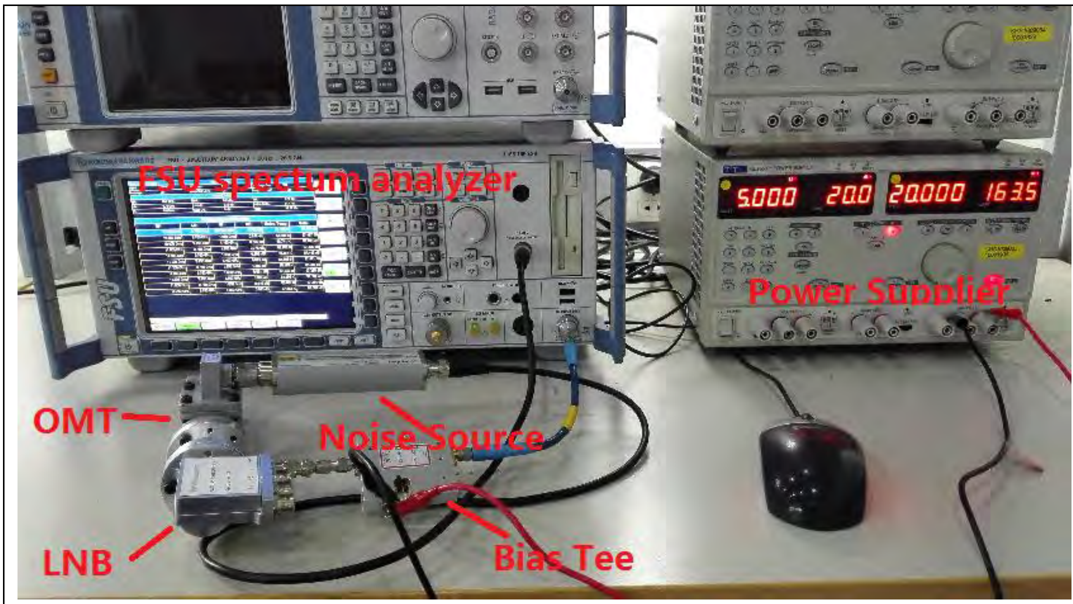


Figure 15 NF test setup

Loss Input Settings

Selection	Table
Loss Input Constant	0 dB

Loss Input Table

RF	Loss Input
10.7 GHz	0.15 dB
10.8 GHz	0.14 dB
10.9 GHz	0.14 dB
11 GHz	0.12 dB
11.1 GHz	0.11 dB
11.2 GHz	0.1 dB
11.3 GHz	0.09 dB
11.4 GHz	0.08 dB
11.5 GHz	0.09 dB
11.6 GHz	0.09 dB
11.7 GHz	0.1 dB
11.8 GHz	0.11 dB
11.9 GHz	0.11 dB
12 GHz	0.1 dB
12.1 GHz	0.09 dB
12.2 GHz	0.08 dB
12.3 GHz	0.09 dB
12.4 GHz	0.11 dB
12.5 GHz	0.13 dB
12.6 GHz	0.15 dB
12.7 GHz	0.18 dB
12.75 GHz	0.19 dB

Figure 16 The loss of the OMT

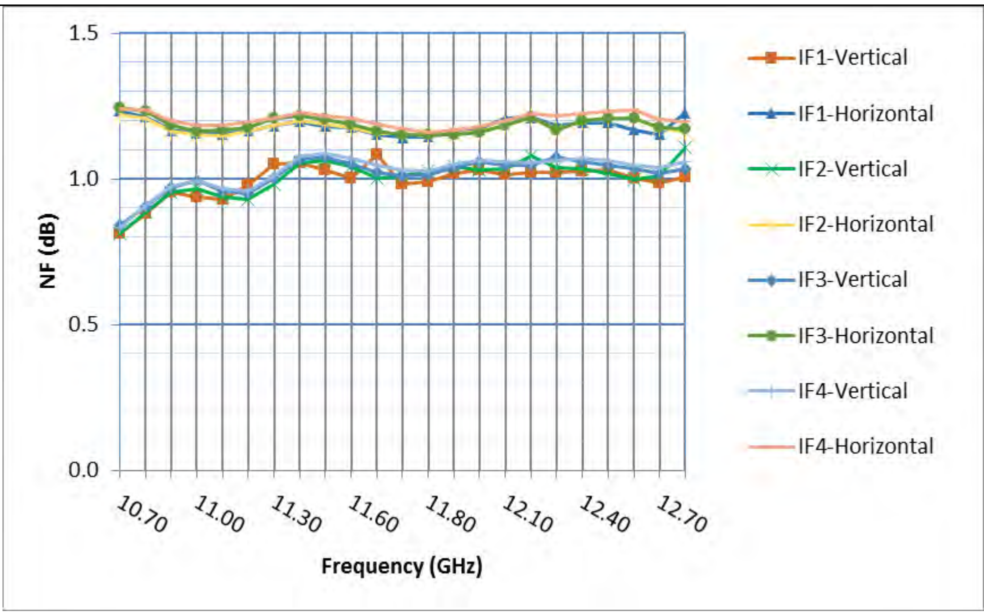


Figure 17 NF test results
The NF is typically 1.0-1.2dB

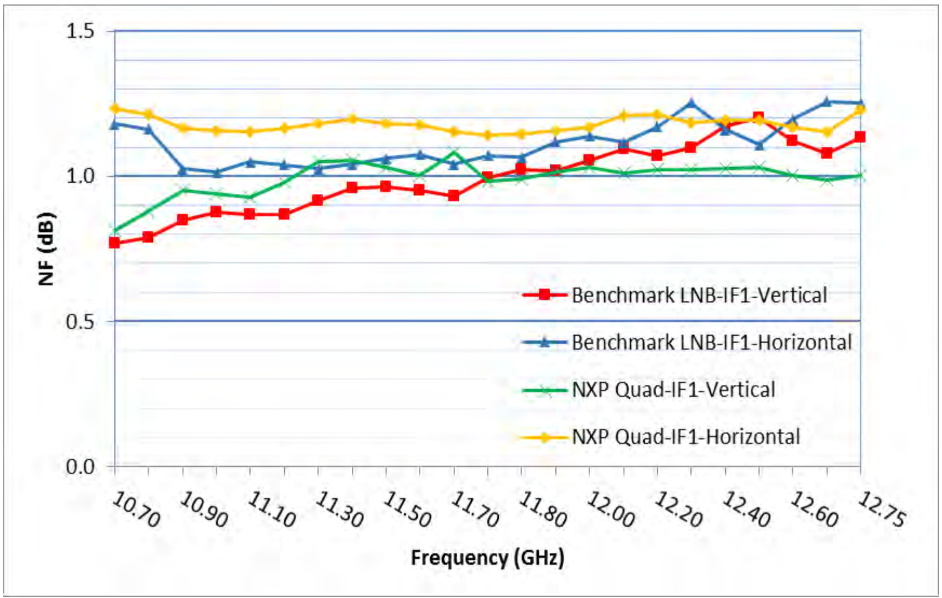


Figure 18 Noise Figure comparison NXP Quad vs. Benchmark LNB
The NF of the NXP Quad and the benchmark LNB are comparable

6.2 Conversion gain

The conversion gain test setup is shown in Figure 19. A Rhode & Schwarz Vector Network Analyzer (VNA) ZVA 24 with frequency conversion option is used in the test. The Power sensor is used for source and receiver power calibration. In conversion gain test, all the ports which are not under test are switched off.

Figure 20 to Figure 23 depict the conversion gain plots of the NXP Quad at both polarities and both bands. In all plots, M1 marks the maximum gain while M2 marks the minimum gain. The conversion gain is in the range of 60±3dB. In all conditions, the gain flatness is typically 2-3dB.

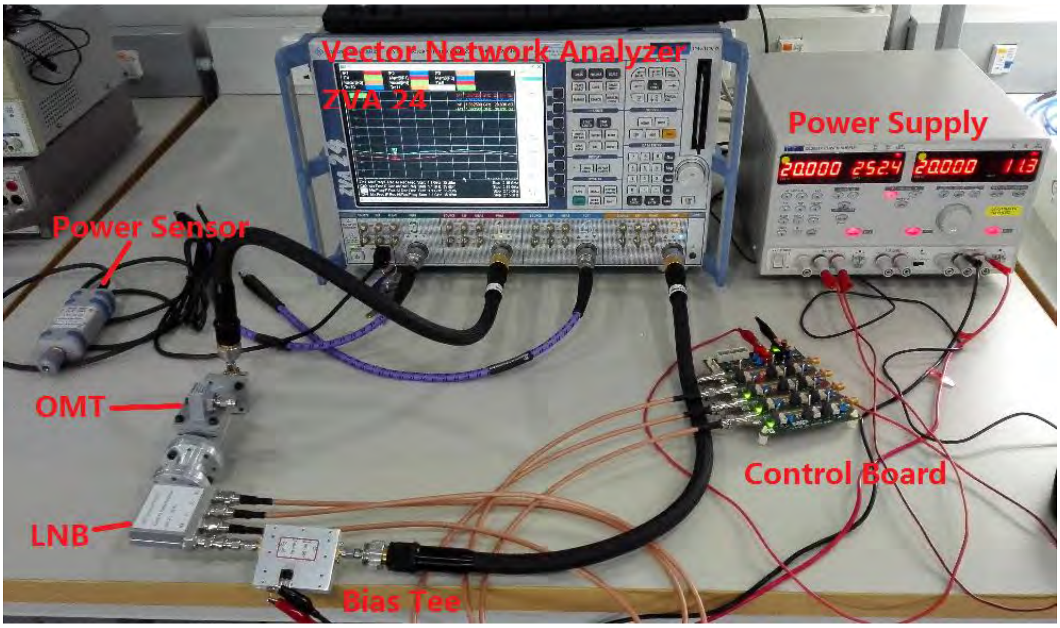


Figure 19 Conversion gain test setup

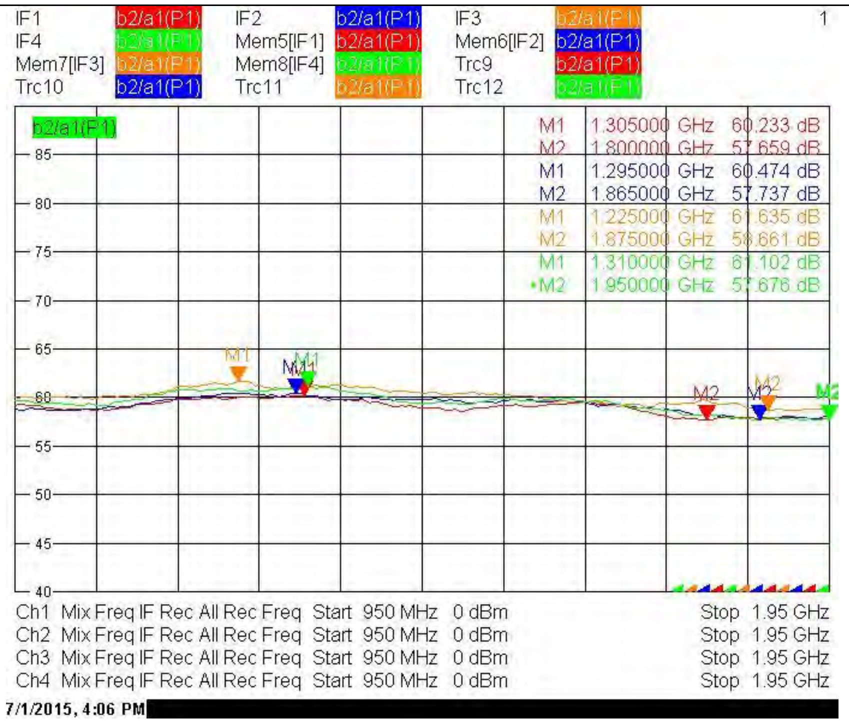


Figure 20 The conversion gain of vertical polarity & low band is 58-62dB
The gain ripple in each IF channel is 3dB max.

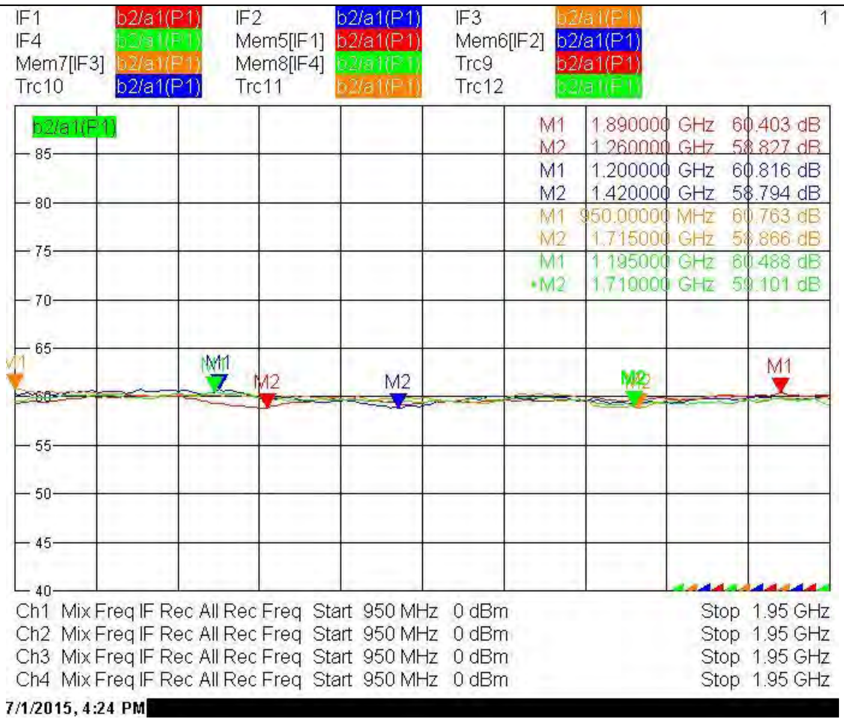


Figure 21 The conversion gain of horizontal polarity & low band is 59-61dB
The gain ripple in each IF channel is 2dB max.

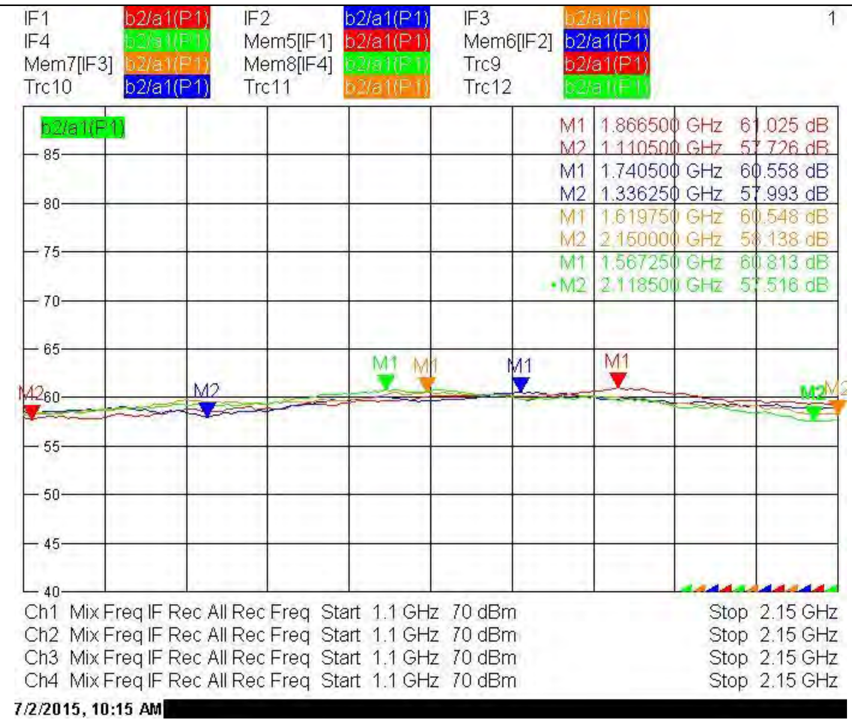


Figure 22 The conversion gain of vertical polarity & high band is 58-61dB
The gain ripple in each IF channel is 3dB max.

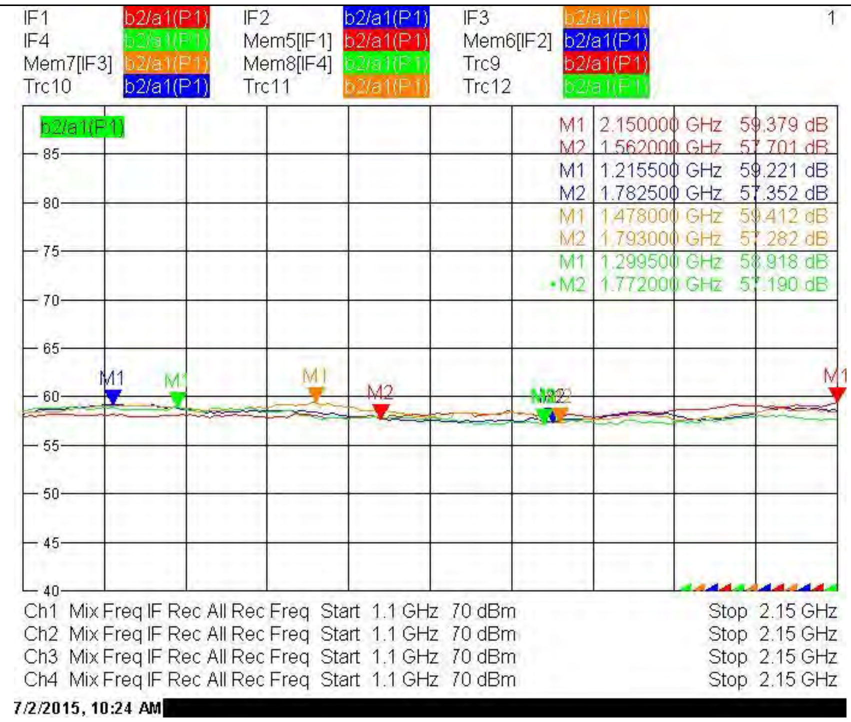


Figure 23 The conversion gain of horizontal polarity & high band is 57-59dB
The gain ripple in each IF channel is 2dB max.

6.3 The third order Output Intercept Point (OIP3)

The OIP3 test setup is shown in Figure 24. Rhode & Schwarz Vector Network Analyzer (VNA) ZVA 24 with frequency conversion and intermodulation test option is used in the test. In addition, a power combiner are used to combine the two tones generated by Port 1 and Port 3 of the VNA, and two isolators are inserted between the power combiner arms and the ports of the VNA to avoid the unwanted IM3 components generated by the instrument itself.

The interval between of two tones is 10MHz, Measurement bandwidth is 200 kHz, and the calibrated input power of each tone is -70dBm. When any port is under test, all the other ports are switched off.

The OIP3 plots for low band and high band are given in Figure 25 and Figure 26 respectively.

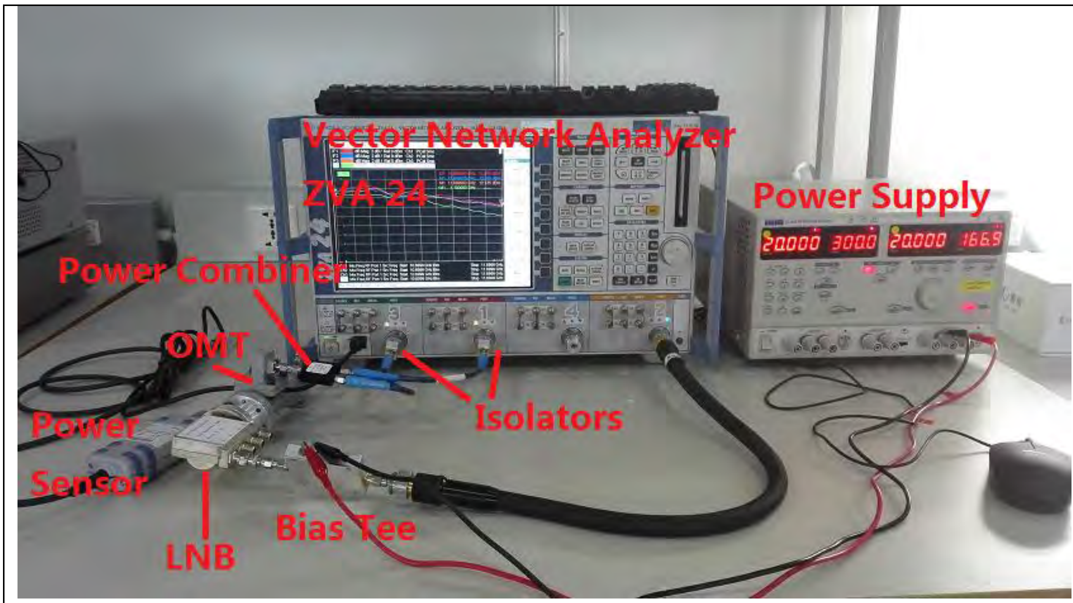


Figure 24 OIP3 test setup

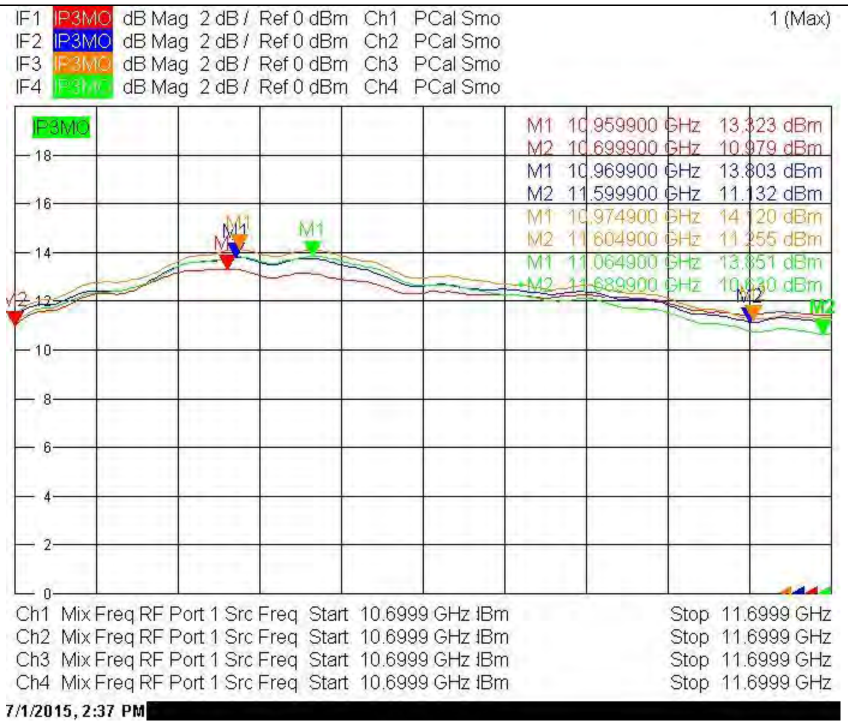


Figure 25 The OIP3 of low band is 11dBm (min.) and 12dBm (typ.)

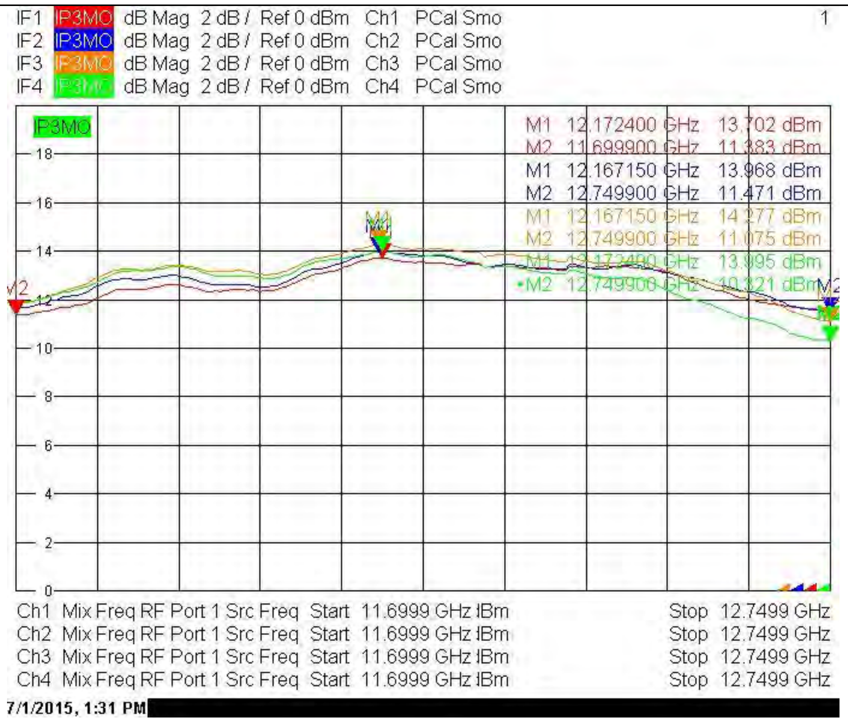


Figure 26 The OIP3 of high band is at least 10dBm (min.) and 12dBm (typ.)

6.4 RMS phase jitter

The RMS phase jitter test setup is shown in Figure 27. A CW signal with very good phase noise is generated by Rhode & Schwarz SMF100A signal generator and injected into the LNB input. The phase jitter is measured at the IF ports by Rhode & Schwarz spectrum analyzer FSU.

The input CW signal is 11.6875GHz for low band and 12.7375GHz for high band. And the output level is -35dBm. The detailed phase jitter test setup for FIMOD IC is described in NXP's application note AN11139.

Since all IF ports of the NXP Quad LNB use the same LO for low band or high band, only one IF port is selected for the LO RMS phase jitter test. All the other IF ports which are not under test are switched off.

The test results are given in Figure 28 and Figure 29 for 9.75GHz and 10.6GHz LO. The RMS phase jitter of these two LO are 1.3° and 1.4° respectively.

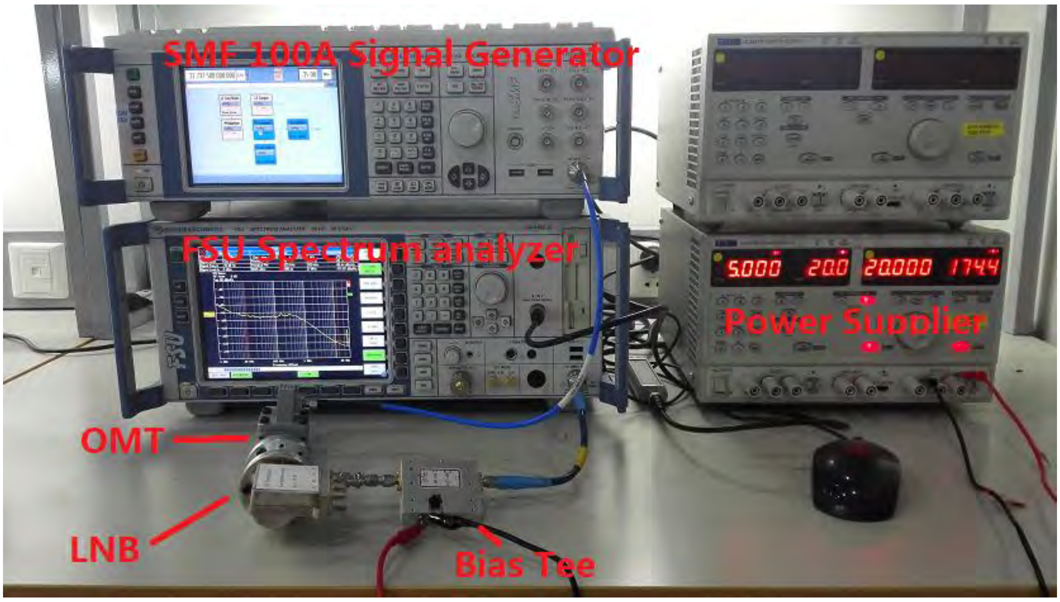


Figure 27 RMS phase jitter test setup

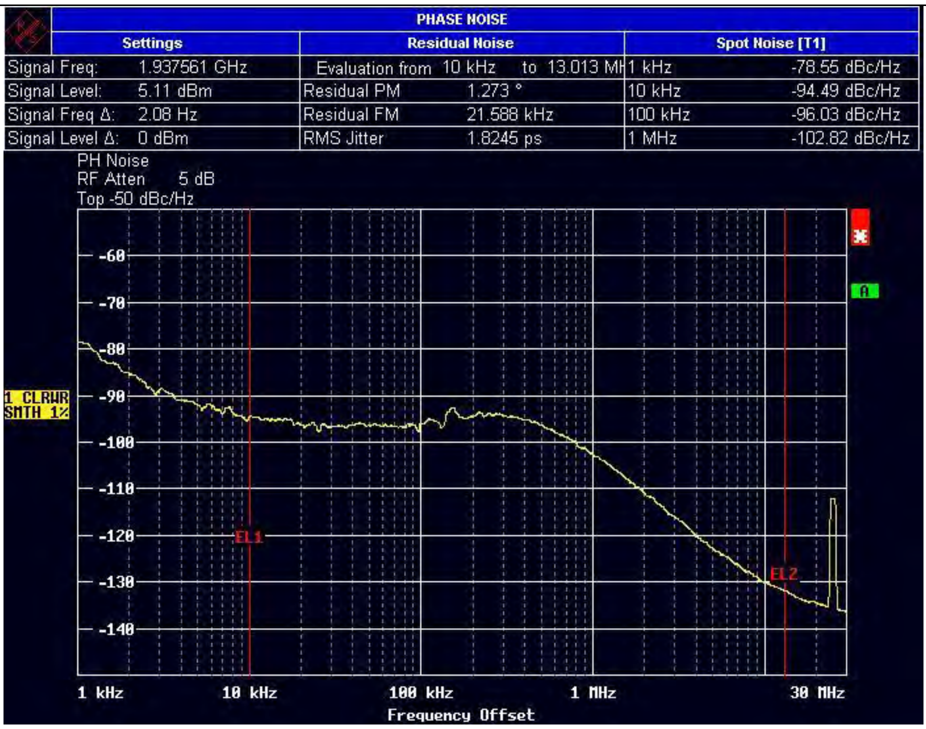


Figure 28 The RMS phase jitter of 9.75GHz LO is 1.3°

Figure 29 The RMS phase jitter of 10.6GHz LO is 1.4°

6.5 Cross polar

The test setup for conversion gain, which is shown in Figure 19, can be used for cross polar test as well.

The signal from different polarity comes in by two ways:

1) The RF coupling in the waveguide, RF chains and RF internal coupling;

2) The IF coupling in the switch matrix, IF transmission lines, and IF internal coupling.

As a smart function of TFF1044HN, when all the IF ports are set as the same polarity, the bias of the LNA of the other polarity is switched off to save power consumption. So in order to obtain the cross polar in the worst case, when one IF port is under test, all the other ports are switched on and set to the other polarity but kept the identical band setting, as shown in Table 5.

Table 5 --- Cross Polar test setting

Test Port	Polarity	Band	The other IF ports		
			Power	Polarity	Band
1,2,3,4	Vertical	Low	ON	Horizontal	Low
		High			High
	Horizontal	Low		Vertical	Low
		High			High

The process of cross polar test is:

Step 1: Run conversion gain test, including power calibration.

Step 2: Store the conversion gain to memory, generate Curve A.

Step 3: Connect the input cable to the other polarity of the OMT.

Step 4: Measure the conversion gain from the other polarity, generate Curve B.

Step 5: Generate the cross polar curve by <Curve A/Curve B>.

The test results of the NXP Quad at both polarities and both bands are given in Figure 30 to Figure 33. Even in the worst case, the cross polar is better than 20dB.

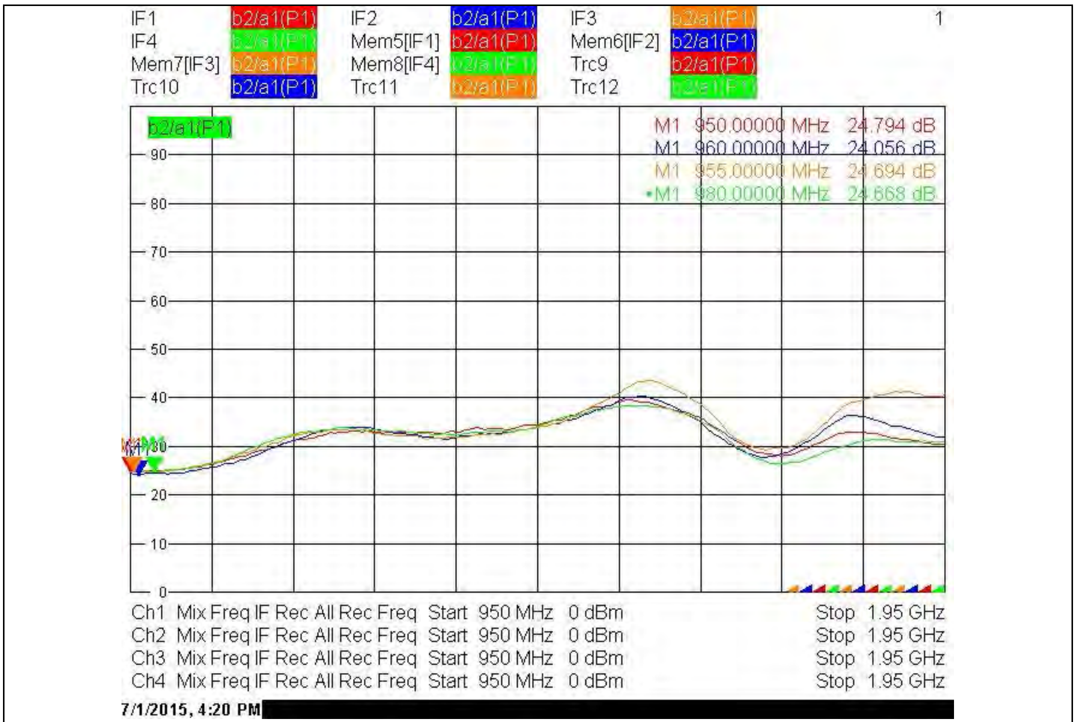


Figure 30 The Cross Polar of vertical polarity & low band is 24dB (min.)

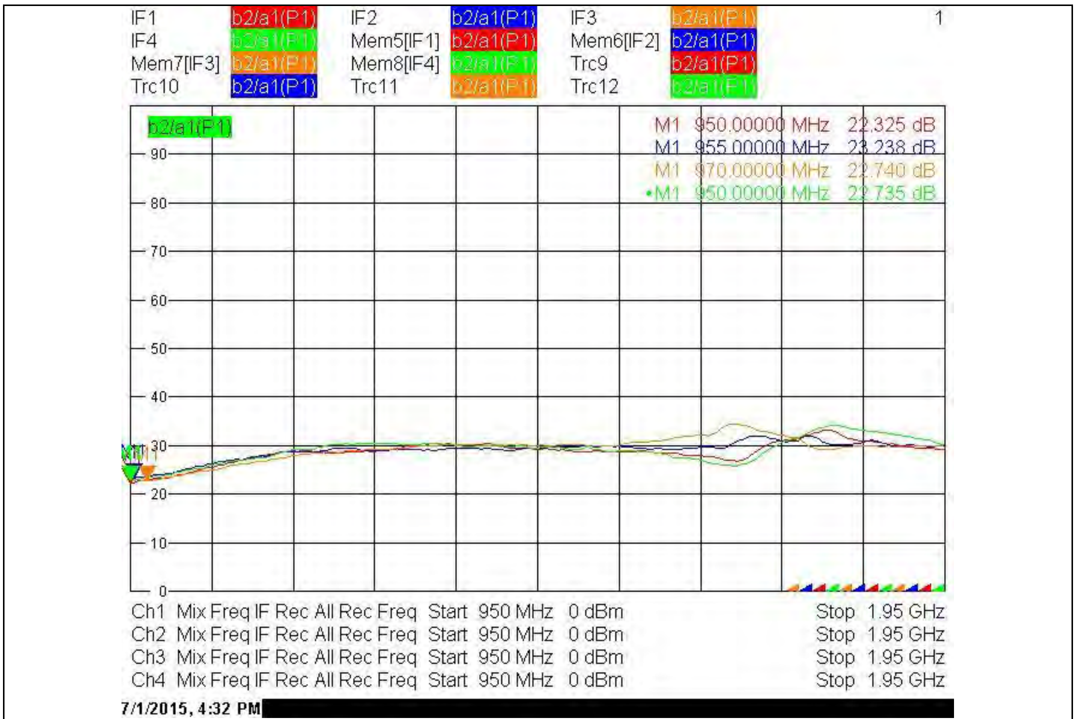


Figure 31 The Cross Polar of horizontal polarity & low band is 22dB (min.)

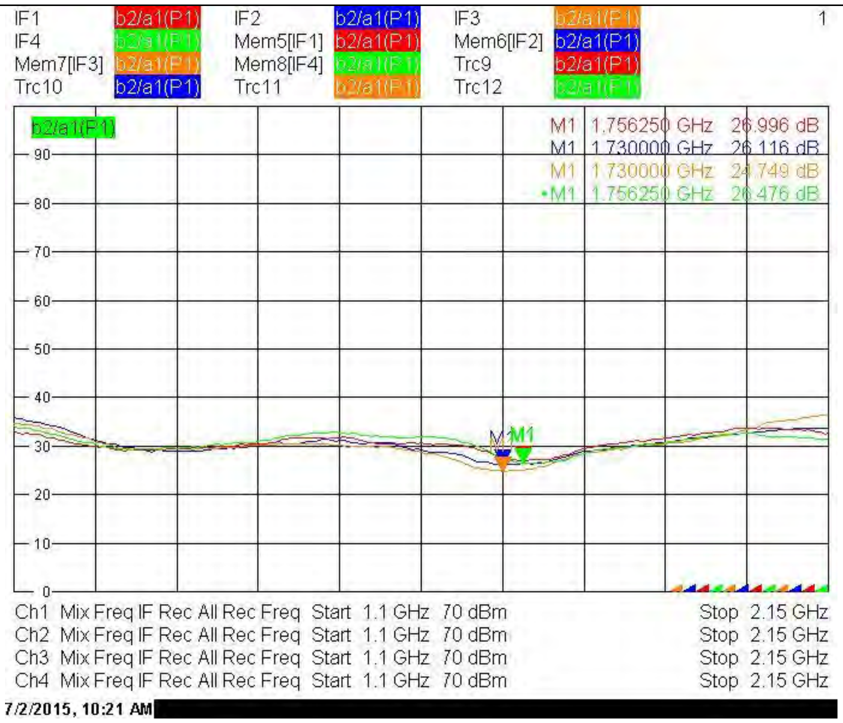


Figure 32 The Cross Polar of vertical polarity & high band is 25dB (min.)

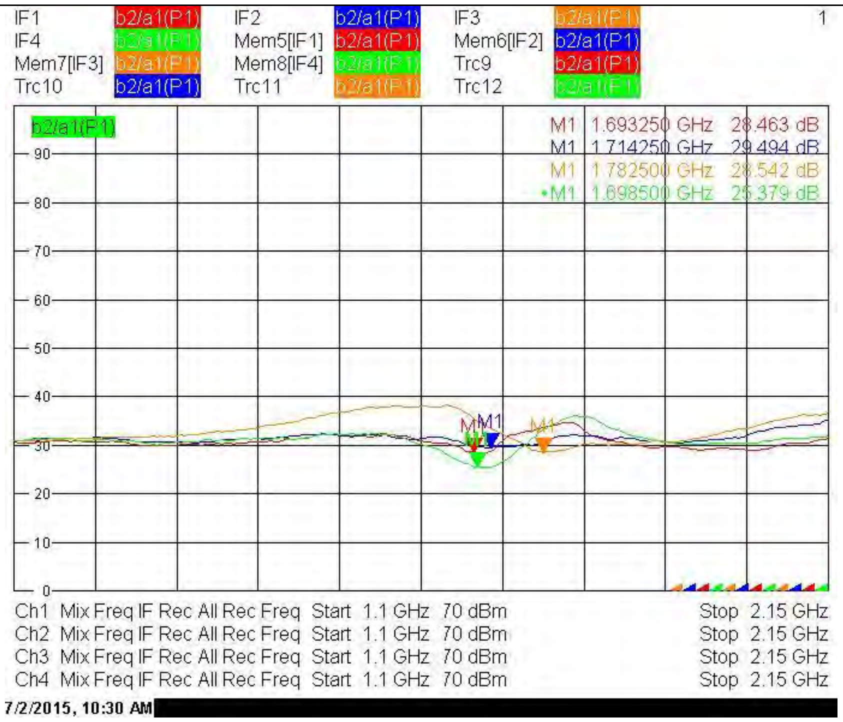


Figure 33 The Cross Polar of horizontal polarity & high band is 25dB (min.)

6.6 Spurious

The major spurious of any quad LNB is at 850MHz (out of IF band) and 1700MHz (in band), which are the 2nd and 4rd intermodulation products of 9.75GHz and 10.6GHz LO.

The spurious test setup is shown in Figure 34. The input of the LNB under test is terminated by the OMT and 50Ω loads to block the interference from the free space. A Rhode & Schwarz spectrum analyzer FSU is used to measure the level of 850MHz and 1700MHz spurious. The loss of the bias Tee and IF cable has been measured and subtracted in the final results.

The status of the other IF ports effect on the spurious level under test. The test settings are listed in Table 6.

The spurious at 850MHz and 1700MHz of the NXP Quad is given in Figure 35 and Figure 36 respectively. The abbreviation PV, PH, LB, HB in the legend stand for vertical polarity, horizontal polarity, low band and high band setting of the IF port under test respectively. While the abbreviation OF, VL, VH, HL, HH in the table under horizontal axis stand for switched off, vertical polarity and low band, vertical polarity and high band, horizontal polarity and low band, horizontal polarity and high band respectively.

According to the test results, when the port is horizontal polarized and low band, the 850MHz spurious is about -14dBm. For the other settings, the spurious is better than -22dBm. For most setting, the 1700MHz is lower than -60dBm. The worst case is -54dBm. The 1700MHz spurious level obviously depends on the status of the other IF ports.

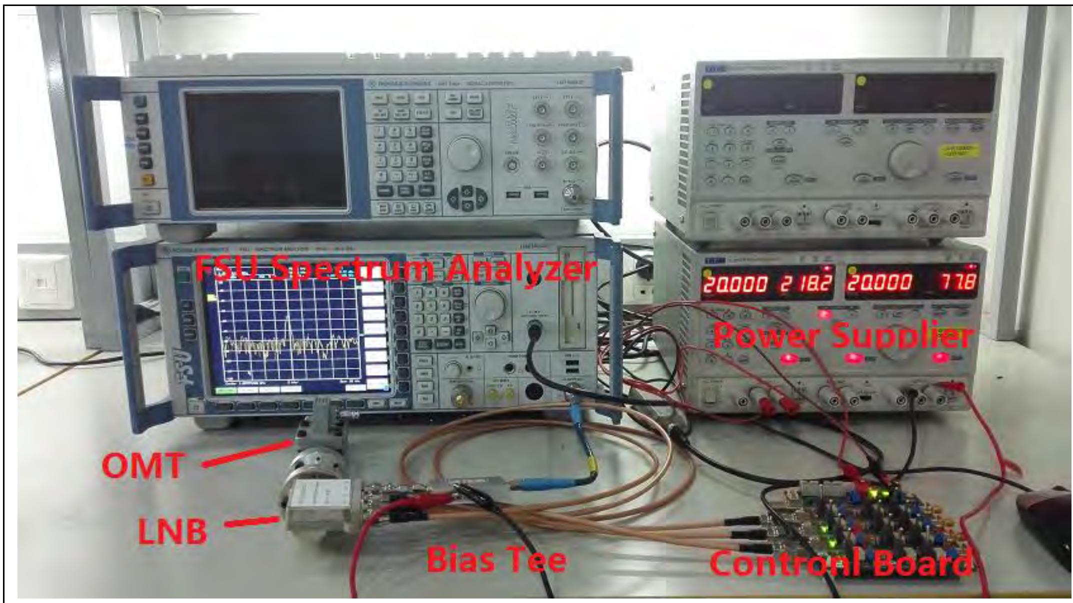
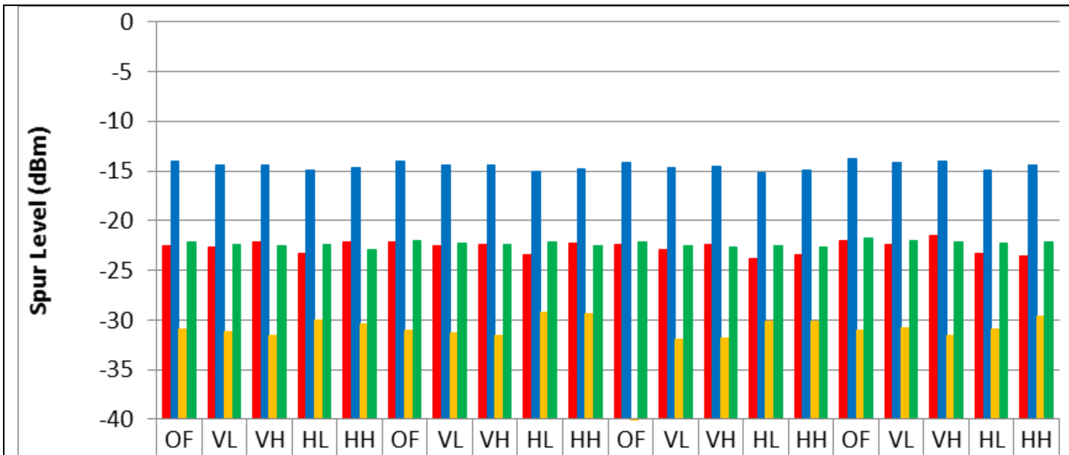


Figure 34 Spurious test setup

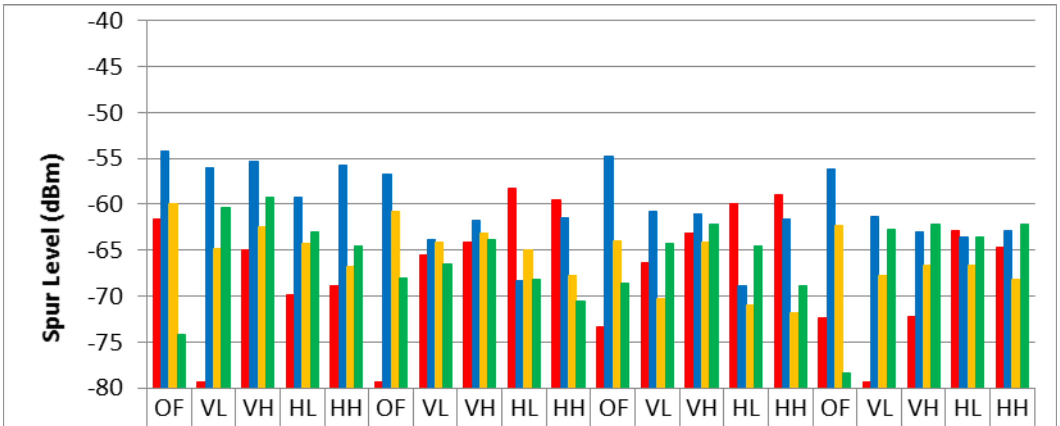
Table 6 850MHz and 1700MHz measurement setting

Test Port	Polarity	Band	The other IF ports: Power	The other IF ports: Polarity	The other IF ports: Band
1,2,3,4	Vertical	Low	OFF	N/A	N/A
			ON	Vertical	Low
					High
				Horizontal	Low
					High
		High	OFF	N/A	N/A
			ON	Vertical	Low
					High
				Horizontal	Low
					High
	Horizontal	Low	OFF	N/A	N/A
			ON	Vertical	Low
					High
				Horizontal	Low
					High
		High	OFF	N/A	N/A
			ON	Vertical	Low
					High
				Horizontal	Low
					High



Test Port	OF	VL	VH	HL	HH	OF	VL	VH	HL	HH	OF	VL	VH	HL	HH	OF	VL	VH	HL	HH
	IF Port 1					IF Port 2					IF Port 3					IF Port 4				
PV_LB	-23	-23	-22	-23	-22	-22	-23	-22	-23	-22	-22	-23	-22	-24	-23	-22	-22	-22	-23	-24
PH_LB	-14	-14	-14	-15	-15	-14	-14	-14	-15	-15	-14	-15	-15	-15	-15	-14	-14	-14	-15	-14
PV_HB	-31	-31	-32	-30	-30	-31	-31	-32	-29	-29	-62	-32	-32	-30	-30	-31	-31	-32	-31	-30
PH_HB	-22	-22	-23	-22	-23	-22	-22	-22	-22	-23	-22	-23	-23	-23	-23	-22	-22	-22	-22	-22

Figure 35 Spurious at 850MHz is -23dBm (typ.) and -14dBm (max.)



Test Port	OF	VL	VH	HL	HH	OF	VL	VH	HL	HH	OF	VL	VH	HL	HH	OF	VL	VH	HL	HH
	IF Port 1					IF Port 2					IF Port 3					IF Port 4				
PV_LB	-62	-79	-65	-70	-69	-79	-66	-64	-58	-60	-73	-66	-63	-60	-59	-72	-79	-72	-63	-65
PH_LB	-54	-56	-55	-59	-56	-57	-64	-62	-68	-62	-55	-61	-61	-69	-62	-56	-61	-63	-64	-63
PV_HB	-60	-65	-63	-64	-67	-61	-64	-63	-65	-68	-64	-70	-64	-71	-72	-62	-68	-67	-67	-68
PH_HB	-74	-60	-59	-63	-65	-68	-67	-64	-68	-71	-69	-64	-62	-65	-69	-78	-63	-62	-64	-62

Figure 36 Spurious at 1700MHz is -65dBm (typ.) and -54dBm (max.)

6.7 Summary on electrical specification

Table 7 Electrical test summary

Parameter		NXP Quad			Benchmark LNB			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Current	1 IF ON[1]		159			153		mA
	2 IF ON[2]		199			174		
	3 IF ON[2]		216			193		
	4 IF ON[2]		234			213		
LO Frequency	Low Band		9749.9			9750.3		MHz
	High Band		10599.9			10599.7		
Conversion Gain	Low Band	58	60	62	59	61	66	dB
	High Band	57	59	61	59	61	63	
Gain Ripple			2.3	3.4		3.1	5.1	dB
Noise Figure	Low Band		1.1	1.2		1.0	1.2	dB
	High Band		1.1	1.2		1.1	1.3	
RMS Phase Jitter[3]	Low Band		1.3			0.2		°
	High Band		1.4			0.2		
OIP3	Low Band	11	12		8	10		dBm
	High Band	10	12		9	12		
Cross Polar Rejection		22	25		22	28		dB
Spurious	850MHz		-23	-14		-41	-23	dBm
	1700MHz		-65	-54		-60	-46	

[1] Only one polarity is selected;

[2] Both polarities are selected.

[3] Integrated from 10kHz to 13MHz.

6.8 Signal quality in live signal receiving

The NXP Quad is mounted on an Andrew 120cm dish antenna to receive the signal from satellite of Astra 19.2^{E}, and the Signal strength, Modulation Error Ratio (MER), Carrier Noise Ratio, Link Margin (LKM, only available in case of DVB-S2)) are measured by Rhode & Schwarz DVB-S / DVB-S2 tester. A 20 meters length coaxial cable (approximately 15dB attenuation) is used to connect the LNB and the tester. The test setup is pictured in Figure 37 (A short cable is employed only for demonstration).

The signal quality of the benchmark LNB is measured as well as the NXP Quad, and the results are compared in Figure 38 to Figure 43. The abbreviation of LB/HB, 1 - 4, V/H, S2 in the legend of these plots stand for low/high band, IF port number, vertical/horizontal polarity, DVB-S2 respectively.

Figure 38 and Figure 39 depict the C/N of the received signal from vertical and horizontal polarity respectively. The C/N of the received signal by the benchmark LNB and the NXP Quad are on the same level.

Figure 40 and Figure 41 depict the MER of the demodulated signal from vertical and horizontal polarity respectively. The MER of the received signal by the benchmark LNB and NXP Quad are close to each other.

Figure 42 and Figure 43 depict the LKM of the DVB-S2 signal (8-PSK modulation) from the vertical and horizontal polarity respectively. The LKM results by the benchmark LNB and the NXP Quad are comparable as well.

In general, the NXP Quad LNB has the comparable signal quality with the benchmark LNB.

Figure 37 Live signal test setup

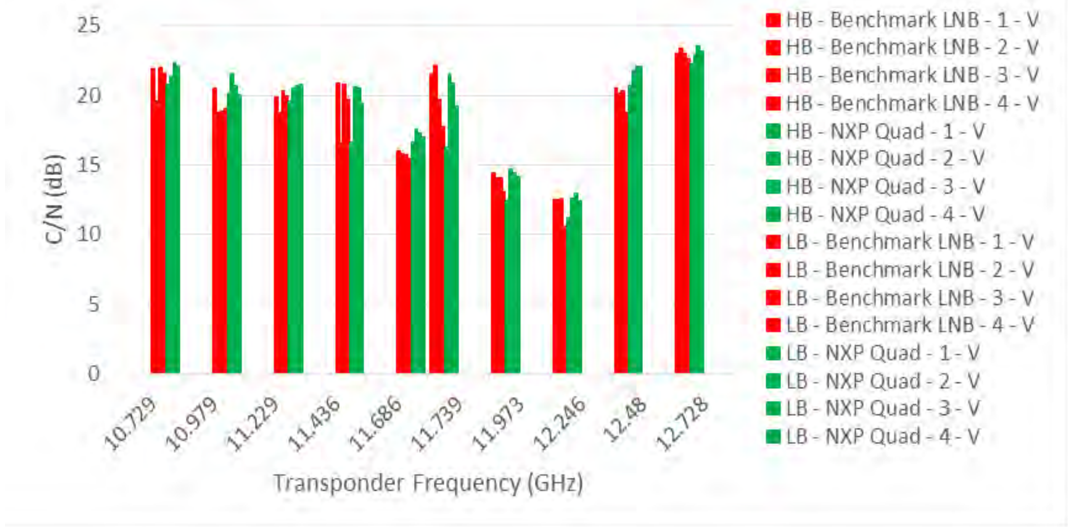


Figure 38 C/N in live signal receiving at vertical polarity
The CN of NXP Quad and the Benchmark LNB are comparable

Figure 39 C/N in live signal receiving at horizontal polarity
The CN of NXP Quad and the Benchmark LNB are comparable

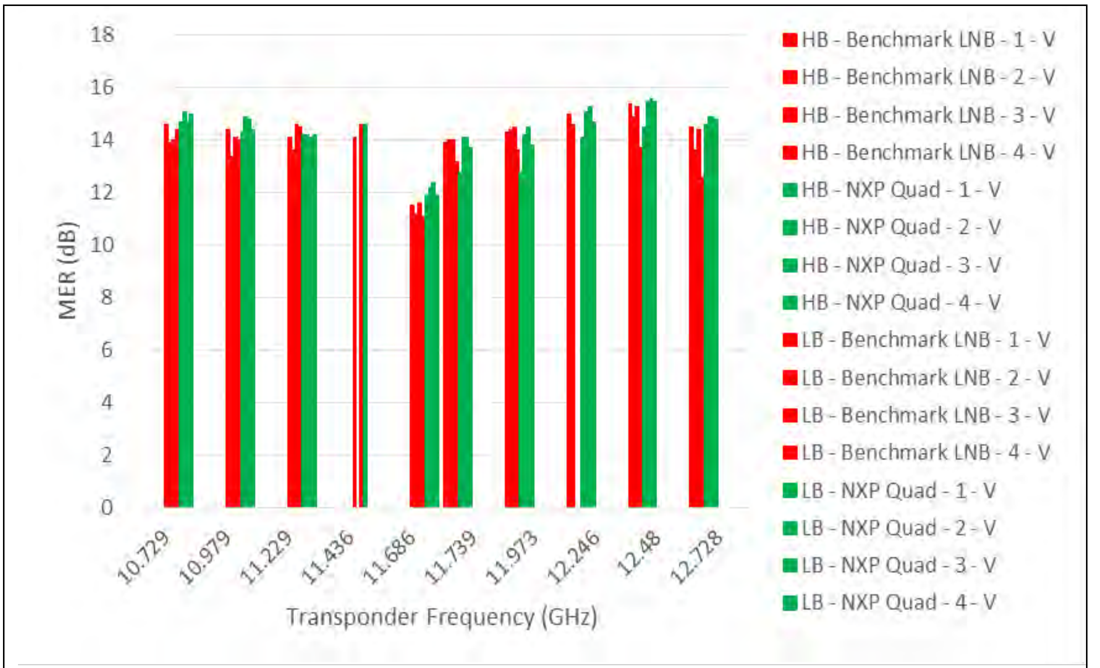


Figure 40 MER in live signal receiving at vertical polarity
The MER of NXP Quad and the Benchmark LNB are comparable

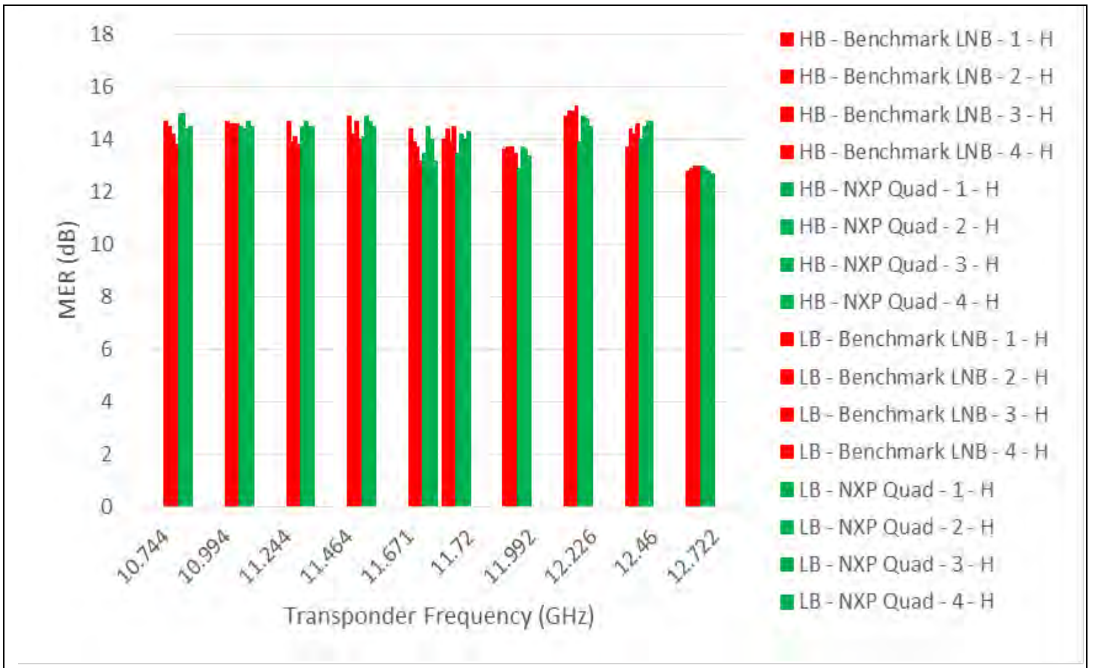


Figure 41 MER in live signal receiving at horizontal polarity
The MER of NXP Quad and the Benchmark LNB are comparable

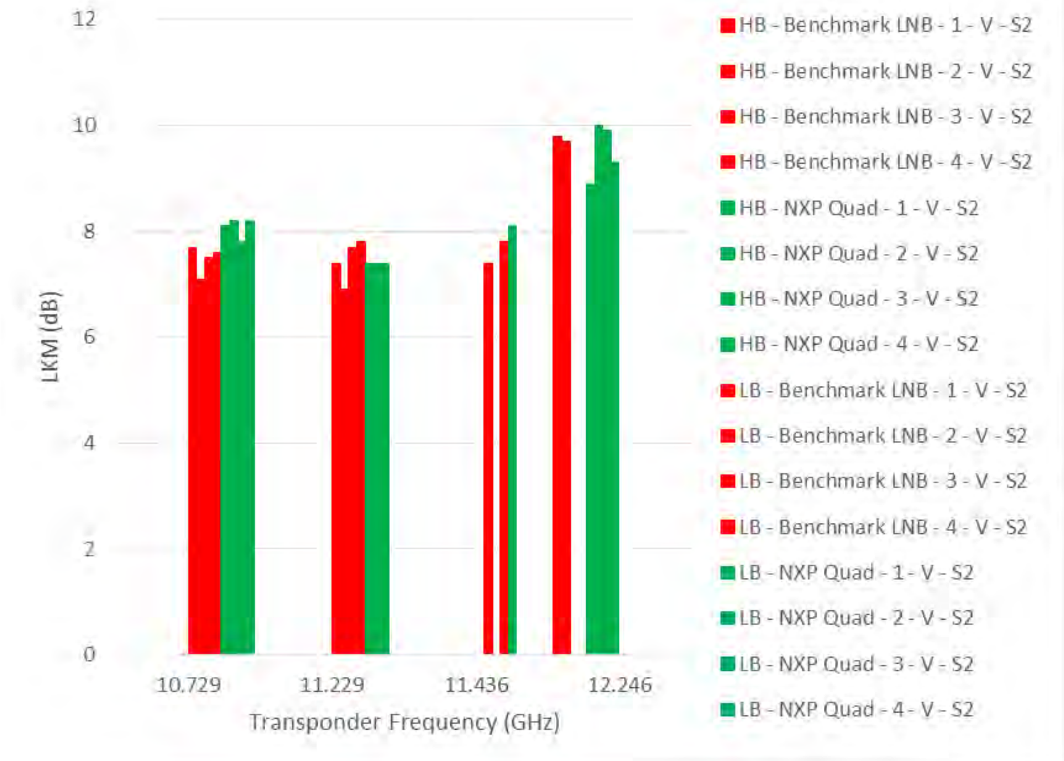


Figure 42 LKM in live signal receiving at vertical polarity
The LKM of NXP Quad and the Benchmark LNB are comparable

Figure 43 LKM in live signal receiving at horizontal polarity
The LKM of NXP Quad and the Benchmark LNB are comparable

7. Conclusions

A Quad LNB reference design based on BFU910F and TFF1044HN has been described in this document. The detailed design including the schematic, BOM, PCB layout, assembly drawing and mechanical drawing are presented.

According to the electric test results summarized in Section 6, the performance of the reference is comparable with the benchmark LNB in commercial market.

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