AN11640

TFF1044 Application Recommendations

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Document information

Info	Content
Keywords	TFF1044, Quad LNB, Quattro LNB, DVB-S, Ku band to L-band Down Converter, FIMOD IC, Ku Band, NF, PCB
Abstract	This application note describes how to use the TFF1044 in a typical environment, (typically in DVB-S outdoor equipment). It also lists some do's and don'ts and frequently asked questions.

Revision history

Rev	Date	Description
1	20150604	First publication

Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Introduction

This document describes the functionality and use of TFF1044 DCV IC. It also gives some application hints and a schematic for a Quad LNB design with pHEMT first stage LNA's and SiGe second stage LNA stages.

2. Product Description

The TFF1044HN is a 10.70 GHz to 12.75 GHz Ku band down converter for use in universal quad and Quattro Low Noise Block (LNB) in satellite receiver systems.
The device features two RF inputs (two polarizations) and four IF outputs (up to 4 active IF paths). It integrates bias generation and control for the external LNA stages, image rejection filtering, LO generation, down conversion mixers, IF amplifier stages, voltage and tone detection on each IF output (for polarization and band selection) and the 4 (IF channels) x 4 (2 polarizations, 2 bands) IF matrix switch.
For flexibility, the gain can be controlled in three discrete stages, the polarization of the RF inputs can be swapped and the second stage LNA biasing control can be switched from pHEMT to BJT configuration.

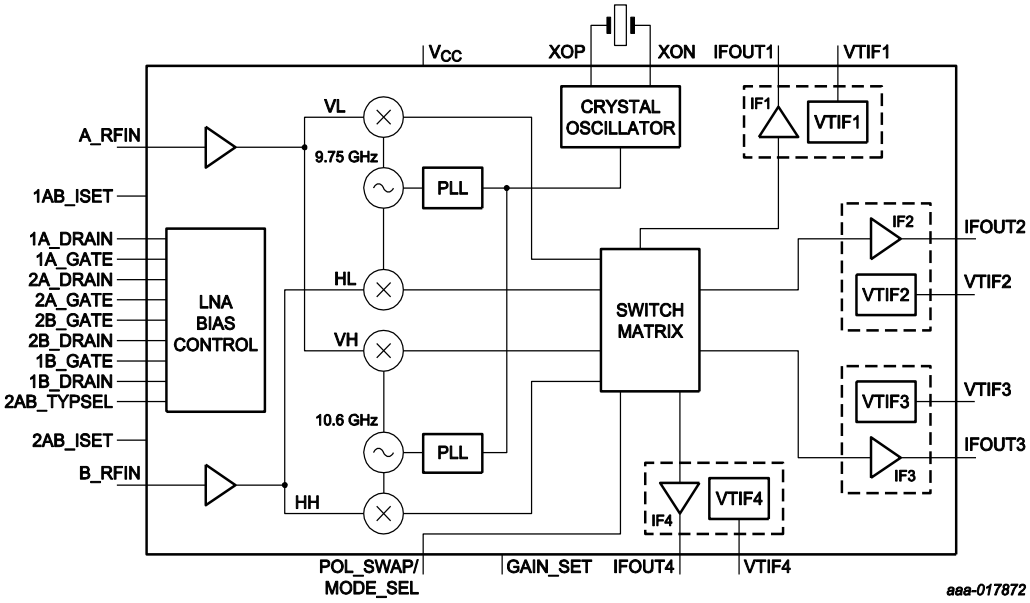


Fig 1. **TFF1044 block diagram**

2.1 Design considerations

The TFF1044 is designed for “outdoor end-user products” such as Quad- and Quattro LNB’s used for Direct-To-Home Television (DTHTV).
It can be used to create an alignment free product with two RF inputs and four IF outputs and enables Printed Circuit Board size reduction.

Apart from the TFF1044, the LNA stages, a 25 MHz crystal, voltage regulator(s) and some passive circuitry is required to complete a quad LNB.

As each device is fully functional tested TFF1044 enables significant cost reduction in the MP final test / repair process compared to discretely build quad/quattro LNB’s.

Image rejection filters are integrated, depending on the required overall image rejection additional filtering may be applied.

Two RF inputs are present to convert the orthogonal polarized signals simultaneously, required LNA’s are usually implemented by two cascaded stages per polarization.
There is a polarization swap selection pin to enable PCB routing with optimum (none crossing) Ku band RF tracks.

The TFF1044 has selectable gain states in order to have freedom to vary the overall LNB gain. Targeted overall Conversion Gain (using two cascaded LNA stages) is 51 dB – 61 dB depending on the gain setting and applied LNA stages (pHEMT and/or SiGe RF transistor). The TFF1044 is capable of driving the bias for the LNA stages for GaAs as well as for SiGe based RF transistors. Depending on required overall NF and Gain also three cascaded stages (biasing for third stage not integrated in TFF1044) may be used.

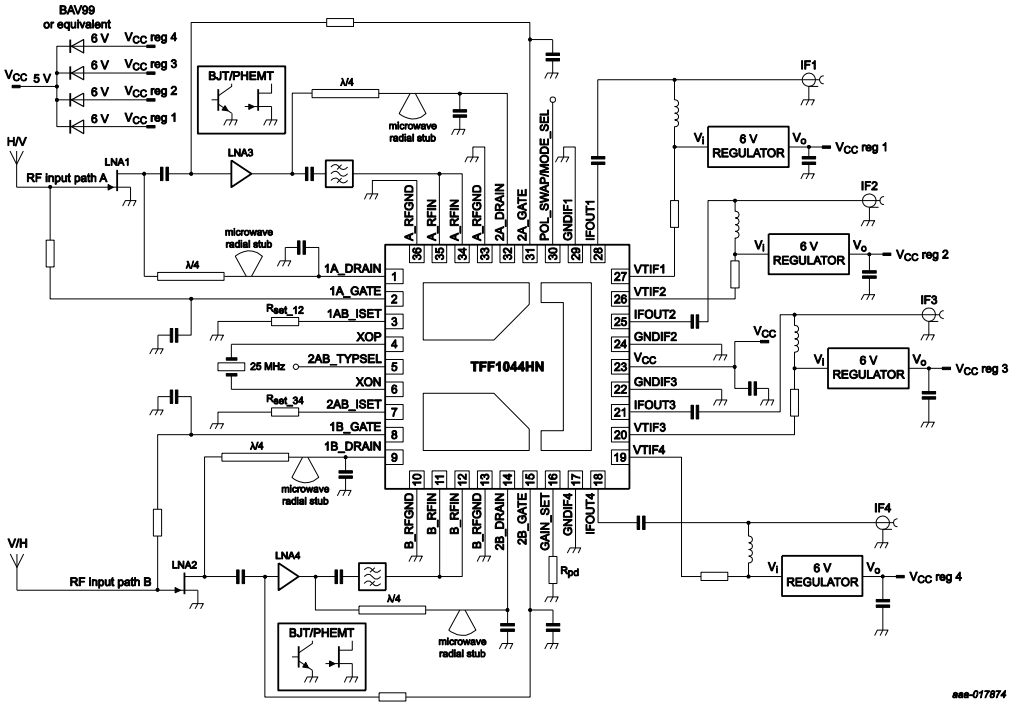


Fig 2. **Typical Quad LNB block diagram**

2.2 Noise Figure and Gain, system level example 1

Example for 2 cascaded pHEMT LNA's, typical gain (EU) LNB:

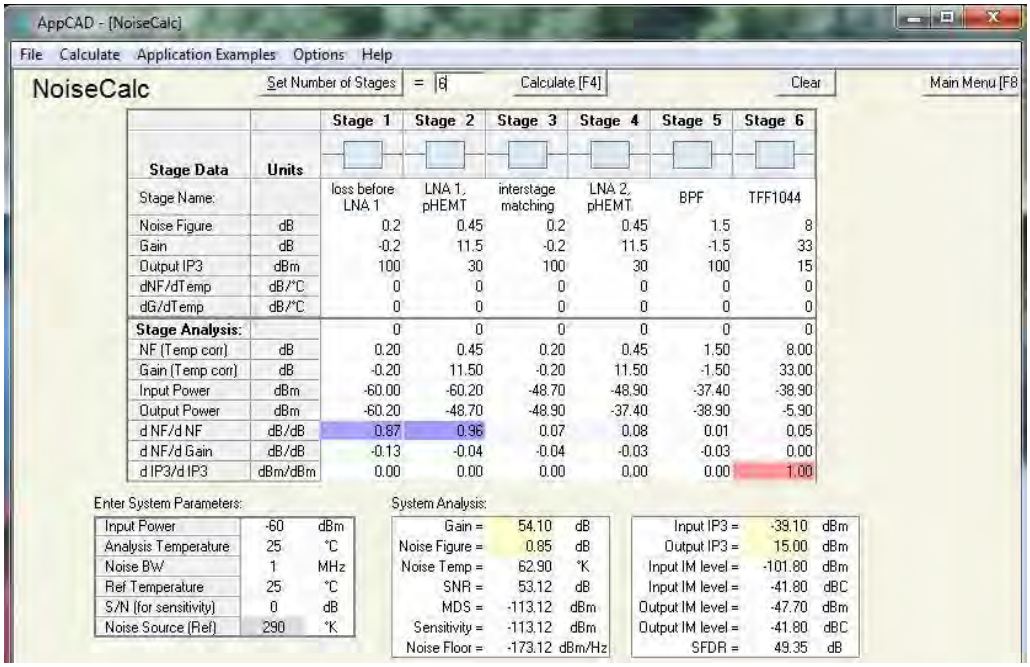
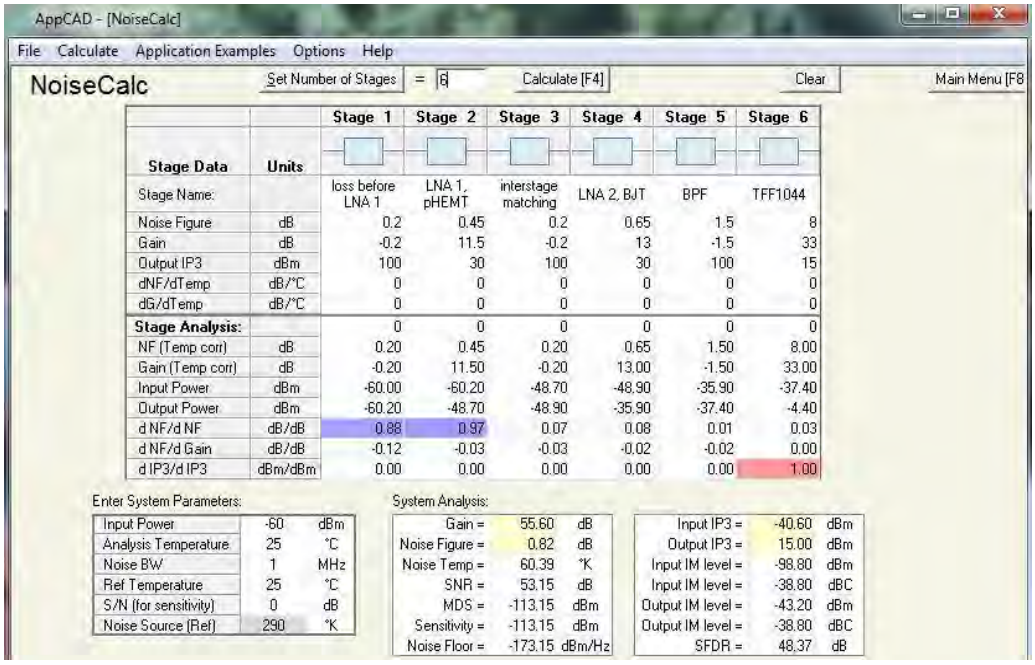


Fig 3. Typical EU gain AppCAD example

In this Noise/Gain budget example for a 55dB Gain LNB, based on Rogers material. We assume two frequently used pHEMT devices are applied as LNA1/LNA2 stages. Gain mode for TFF1044 is medium, values applied are typical (overall typical Gain is 54 dB, NF is 0.85 dB).

2.3 Noise Figure and Gain, system level example 2

Example for 1st stage pHEMT, 2nd stage BJT LNA's, typical gain (EU) LNB:



Stage Data	Units	Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6
Stage Name:		loss before LNA 1	LNA 1, pHEMT	interstage matching	LNA 2, BJT	BPF	TFF1044
Noise Figure	dB	0.2	0.45	0.2	0.65	1.5	8
Gain	dB	-0.2	11.5	-0.2	13	-1.5	33
Output IP3	dBm	100	30	100	30	100	15
dNF/dTemp	dB/°C	0	0	0	0	0	0
dG/dTemp	dB/°C	0	0	0	0	0	0
Stage Analysis:		0	0	0	0	0	0
NF (Temp corr)	dB	0.20	0.45	0.20	0.65	1.50	8.00
Gain (Temp corr)	dB	-0.20	11.50	-0.20	13.00	-1.50	33.00
Input Power	dBm	-60.00	-60.20	-48.70	-48.90	-35.90	-37.40
Output Power	dBm	-60.20	-48.70	-48.90	-35.90	-37.40	-4.40
d NF/d NF	dB/dB	0.88	0.97	0.07	0.08	0.01	0.03
d NF/d Gain	dB/dB	-0.12	-0.03	-0.03	-0.02	-0.02	0.00
d IP3/d IP3	dBm/dBm	0.00	0.00	0.00	0.00	0.00	1.00

Input Power	-60	dBm
Analysis Temperature	25	°C
Noise BW	1	MHz
Ref Temperature	25	°C
S/N (for sensitivity)	0	dB
Noise Source (Ref)	290	°K

Gain =	55.60	dB
Noise Figure =	0.82	dB
Noise Temp =	60.39	°K
SNR =	53.15	dB
MDS =	-113.15	dBm
Sensitivity =	-113.15	dBm
Noise Floor =	-173.15	dBm/Hz

Input IP3 =	-40.60	dBm
Output IP3 =	15.00	dBm
Input IM level =	-98.80	dBm
Input IM level =	-38.80	dBC
Output IM level =	-43.20	dBm
Output IM level =	-38.80	dBC
SFDR =	48.37	dB

Fig 4. Typical EU Gain AppCAD example using 2 BFU910

In this Noise/Gain budget example for a 55dB Gain LNB, based on Rogers material. In this Noise/Gain budget example we assume one frequently used pHEMT device as first stage cascaded by a BFU910 as 2nd LNA stage. Gain mode for TFF1044 is medium, values applied are typical (overall typical Gain is 56 dB, NF is 0.82 dB).
So compared to example 1 replacing the 2nd stage LNA by SiGe BFU910 RF transistor the overall gain increased by 1.5dB while the overall Noise Figure decreases by 0.03dB!

2.4 Noise Figure and Gain, system level example 3

Example for 1st stage BFU910, 2nd stage BFU910 LNA's, typical high gain LNB:

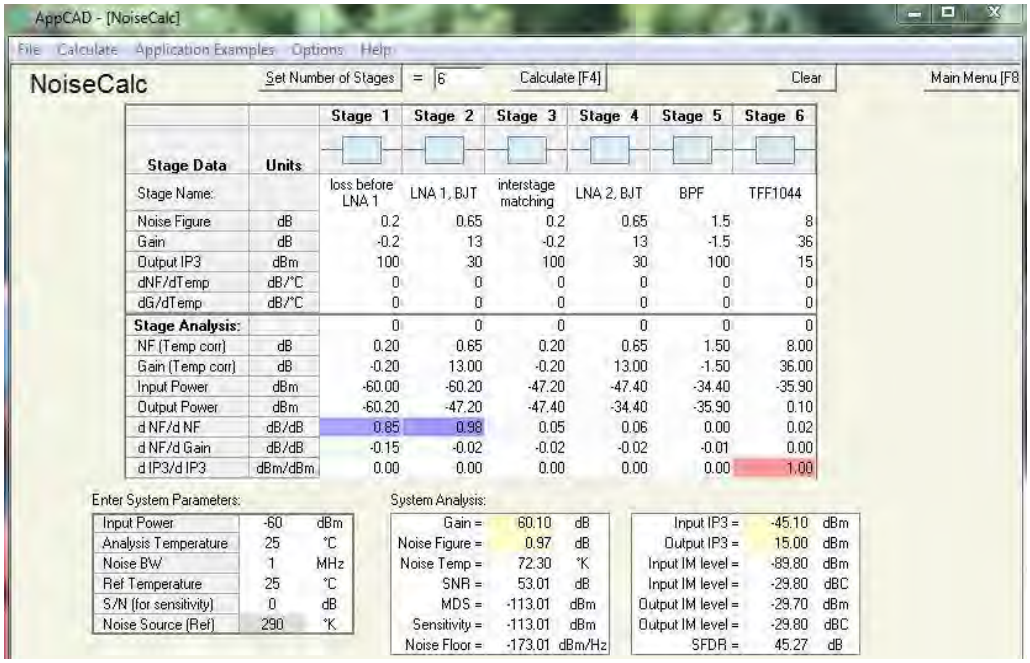


Fig 5. Typical high gain AppCAD example using 4 BFU910

In this Noise/Gain budget example for a 60dB Gain LNB, based on Rogers material. In this Noise/Gain budget example we assume both LNA stages are implemented by SiGe BFU910.
Please note that the biasing for two LNA stages is sourced from the TFF1044, two stages need to be biased by resistive networks (compared to pHEMT a simple network could be applied as no negative bias voltage is required).
Gain mode for TFF1044 is high, values applied are typical (overall typical Gain is 60 dB, NF is 0.97 dB).

Overview of system-level examples:

1st stage LNA	2nd stage LNA	TFF1044 gain setting	Expected Overall Gain	Expected Overall NF
Common used pHEMT	Common used pHEMT	medium	54 dB	0.85 dB
Common used pHEMT	NXP BFU910	medium	56 dB	0.82 dB
NXP BFU910	NXP BFU910	high	60 dB	0.97 dB

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3. I/O's description

3.1 RF inputs, A_RFIN and B_RFIN

The two RF-inputs are designed to have a characteristic impedance of 50 Ω in the Ku band, and are AC coupled. However there is a DC short to GND on both inputs (inductors used as part of the RF filtering). Therefore LNA outputs that carry DC cannot be directly connected to the A_RFIN and/or B_RFIN pins.

A S1P file with complex impedance over frequency, required for S11 optimization in a simulator, can be down-loaded from www.nxp.com.

RF input impedance in Smith chart, (1) = 10.7 GHz, (2) = 12.75 GHz

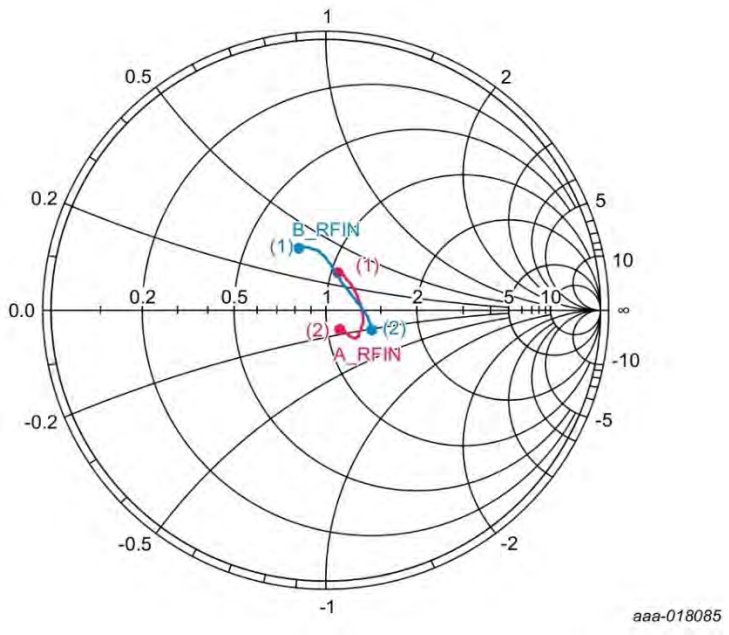

Fig 6. Typical RFA/RFB input impedance

There is a slight difference between both inputs, due to the physical design.

3.2 IF outputs

The four IF outputs have a characteristic impedance of 75 Ω in the L-band and are DC coupled. A DC blocking capacitor is required. Those outputs are usually combined with the Vif_X (with 1<X<4) pins to enable V/T detect on each IF output (not required for Quattro mode).

3.3 PHEMT bias control

Maximum four LNA stages, normally two cascaded stages per RF path, can be biased. The first stages are pHEMT types only. The second LNA stages can be pHEMT or RF transistor: set by the pin 2AB_TYPSEL. Connect this pin to GND for pHEMT bias selection, and leave it floating to bias BFU910 or equivalent.

3.4 LNA bias current setting

Used to program the LNA quiescent current, i.e. 10mA for typical pHEMT's. Pin 1AB_ISET programs the quiescent current for the first stage LNA's (RFA as well as RFB), the pin 2AB_ISET has a similar function for the 2nd LNA stages. A typical resistor of 22 kΩ to GND is applied to set 10 mA typical DC bias current. The allowed range for the Rset resistors is 15 kΩ to 220 kΩ. Typical values of the quiescent current as function of the Rset resistor value is shown in the table below.

Rset value	220 kΩ	33 kΩ	22 kΩ	15 kΩ
Average Id measured at nominal conditions	1 mA	7 mA	11 mA	15 mA

3.5 Crystal pins (reference oscillator)

These are used to connect the crystal, required for the PLL in the LO generation. Avoid long in-balanced tracks, they could lead to interference.
A typical load capacitance of 16 pF is seen for the TFF1044 including the parasitic capacitance of the PCB pads.

3.6 IF mode control pins (VT-IF X, 1 < X < 4)

These are inputs correlated to the four IF outputs and control the 4 x 4 switch matrix. Switching between RFA and RFB depends on the DC value, LB/HB selection depends on the presence of a 22 kHz pulse superposed on the DC.

3.7 Polarization Swap / Mode Select

With this pin one could set the TFF1044 in different modes, for example toggle the RFA ⇔ RFB selection mode (depending on Voltage on pin VT_IF X). This enables the shortest none-crossing possible routing of the RF tracks in the front-end part of the LNB.

To program the TFF1044 into Quattro mode this pin should be pulled down to GND via a 100 kΩ resistor. For normal operation (RFA is horizontal) this pin should be grounded, to swap (RFB is horizontal) the pin must be kept floating.

3.8 Gain Select

The TFF1044 conversion gain has three modes, low, medium and high gain (typ. 30, 33 and 36dB). Pin GAIN_SET must be grounded for low gain, floating for medium gain and connected to GND via 100 kΩ for high gain mode.

4. Typical application Diagrams / Schematics

Example of NXP Quad Reference LNB, more detailed info in AN11674

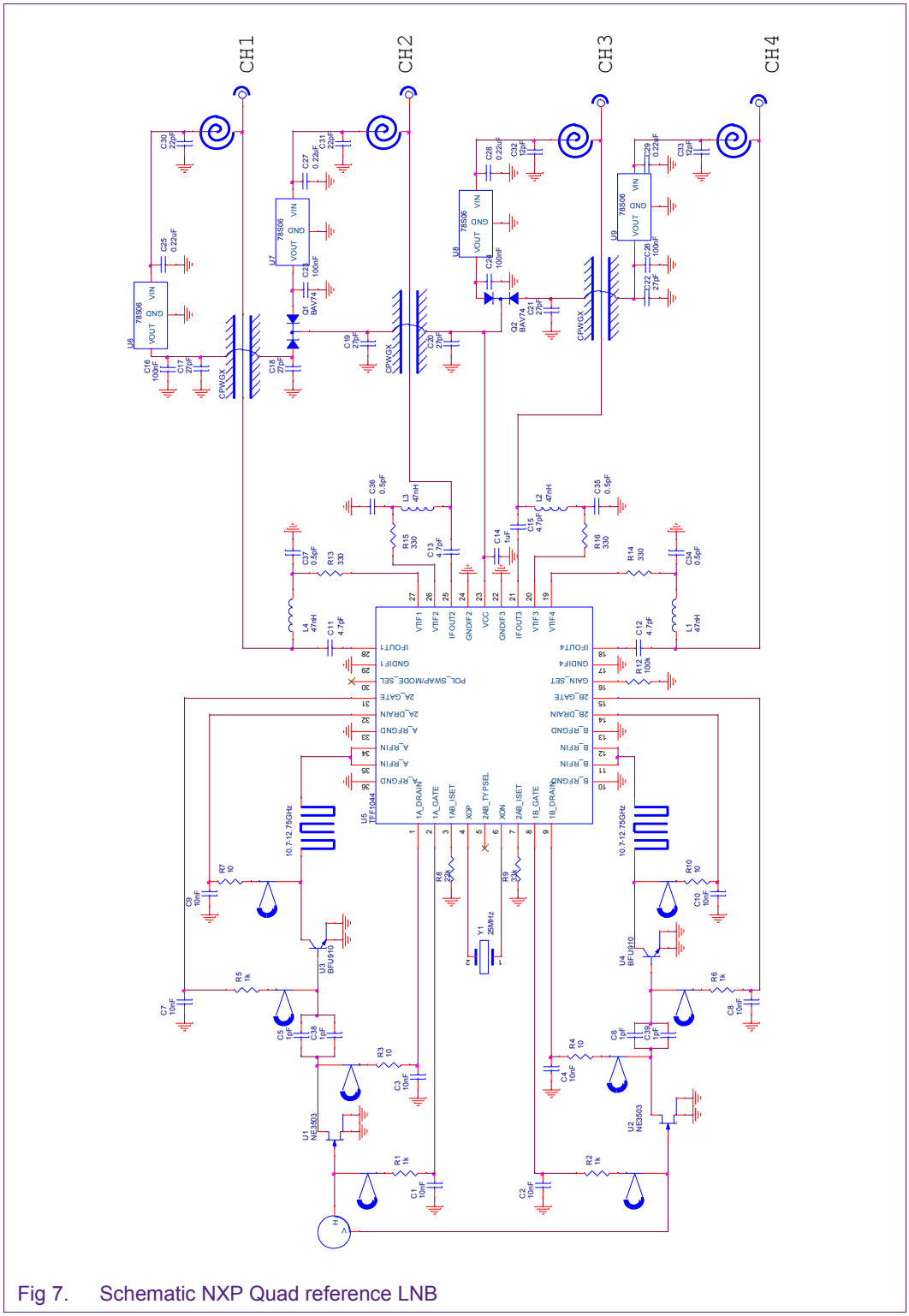

Fig 7. Schematic NXP Quad reference LNB

Picture of NXP Quad Reference LNB, see also AN11674

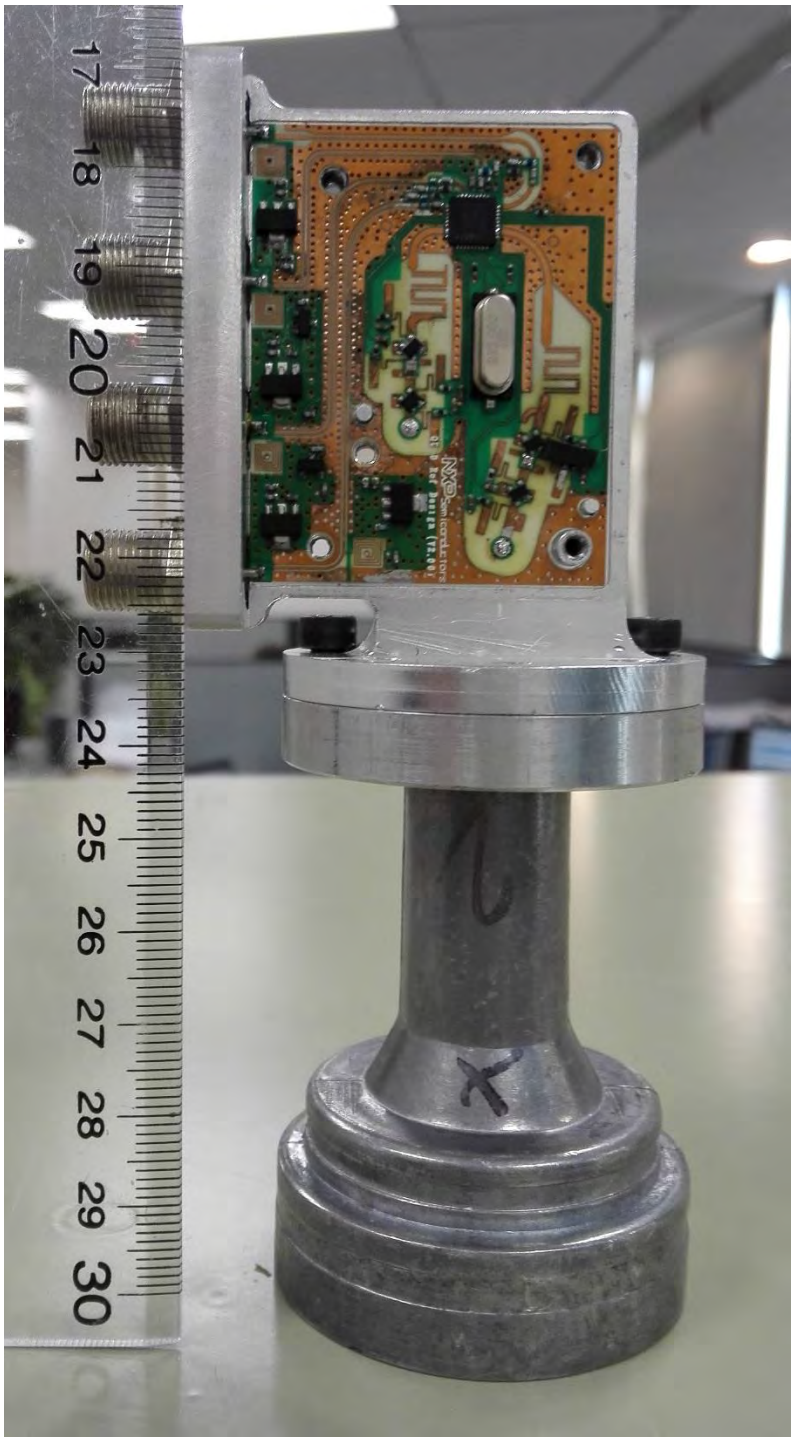

Fig 8. NXP Quad Reference LNB

4.1 Supply topology

LNB's (DVB-S outdoor equipment) are usually supplied by the indoor equipment over the coaxial cable(s). RF is superposed on the DC content, hence in the LNB Bias Tees are required to separate the DC from the AC content.

The DC voltage at the IF is also used to select the required polarization for corresponding IF. Common used values are 18 V (Vertical Polarization) or 13 V (Horizontal Polarization).

In addition a low frequency pulse is used to control the band selecting for corresponding IF. A common frequency for this pulse is 22 kHz, no tone selects LB, with tone present, within specified voltage range, HB is selected.

Requirements for the supply:

1) The entire supply current can be sourced from 1 indoor unit (STB) or multiple (maximum 4), DC separation between the IF outputs is required;
2) The 22kHz pulse may not be present on each IF hence isolation at 22 kHz is required in order to guarantee proper band selection;
3) In case linear regulators are used the worse-case scenario for power dissipation and thermal behavior should be monitored/safeguarded (usually in case the LNB has only one active user at 18 Volts).

In NXP Quad reference LNB design each IF has a linear regulator (each one having Imax >200 mA) connected to generate 6 Volts. By doing this the IF's are separated for DC.
The outputs of the regulators are combined, using 4 diodes (If >200 mA), to prevent current flowing from one regulator to the others in case multiple IF's are activated. Due to these diodes the supply voltage for the TFF1044 will be the regulator voltage minus one forward diode voltage.

4.1.1 Regulator decoupling capacitors

The regulators require a decoupling capacitor to GND at each input to suppress noise on the supply lines and to enable stable operation. Using a large capacitor value will cause a low AC impedance and might impact the 22 kHz pulse amplitude. A too small value might lead to regulator instability. Align with the vendor of applied regulator for the lowest, but still safe, possible capacitor value. The capacitor at the regulator outputs can have each required value.

4.1.2 TFF1044 decoupling capacitor

The TFF1044 has integrated regulators and supply decoupling for high frequencies. For low frequency noise/ripple rejection a decoupling capacitor of 1uF, close to the Vcc pin, is recommended.

4.1.3 The IF output Transmission Lines/ Bias Tees

Example for application, configuration for one IF path:

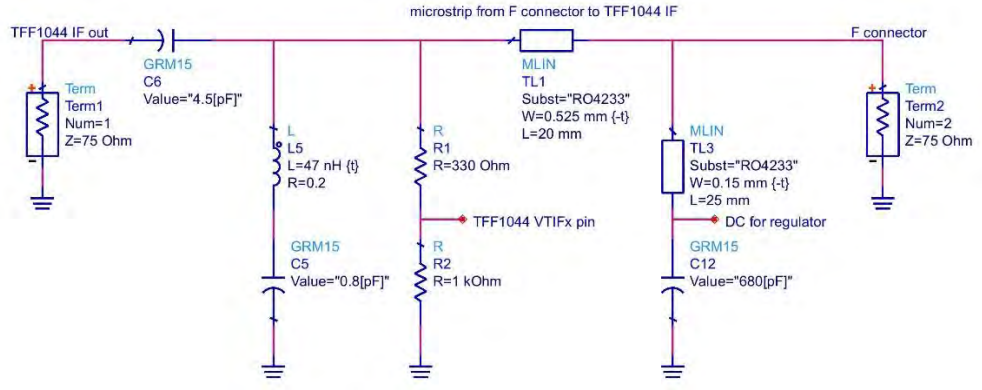

Fig 9. IF path incl. bias Tee / 850 MHz trap-filter

The signal path from TFF1044 IF outputs to the LNB F-connector should contain:
- a 75 Ohms transmission line (TL) to transport RF energy from TFF1044 to F-connector, represented in the schematic above as TL1;
- a way to transport the 22 kHz pulse from the F-connector to the TFF1044 VT-detect pin, by the 330 ohms resistor R1;
- a Bias Tee to separate the DC on the F-connector and feed it into the regulator without effecting the RF signal path, represented in the schematic above as TL3;
- a DC blocking functionality to protect the TFF1044 IF output as C6;
- optionally a trap-filter to suppress the spurious tone generated by the difference of the LO frequencies, created in the schematic above by L5/C5.

Simulated transfer for given configuration:

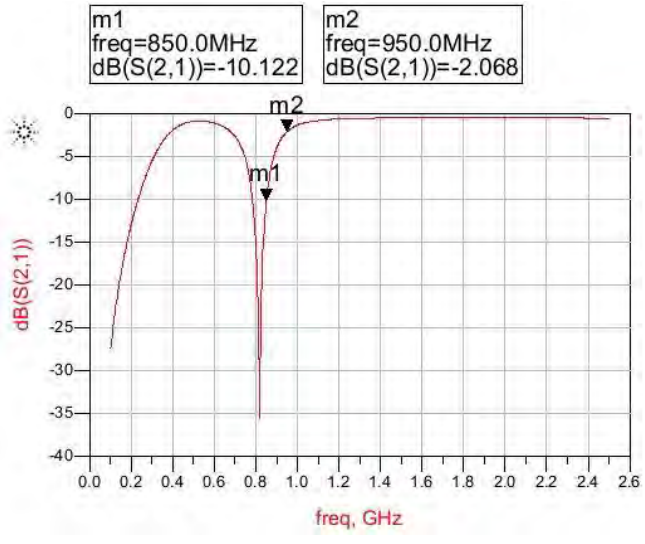

Fig 10. Simulated S21 for shown IF path

Experiments on the TFF1044 evaluation board show that in case a low cost variable wire wound inductor is used (0.4mm wire/2.5mm diameter/4.5 turns), as often applied in tin-canned tuners, and alignment is allowed a rejection of the 850 MHz spurious up to 25 dB is possible. The impact on the 950 MHz gain can be less than 1 db.

5. Creating a PCB layout with TFF1044

5.1 Recommended footprint

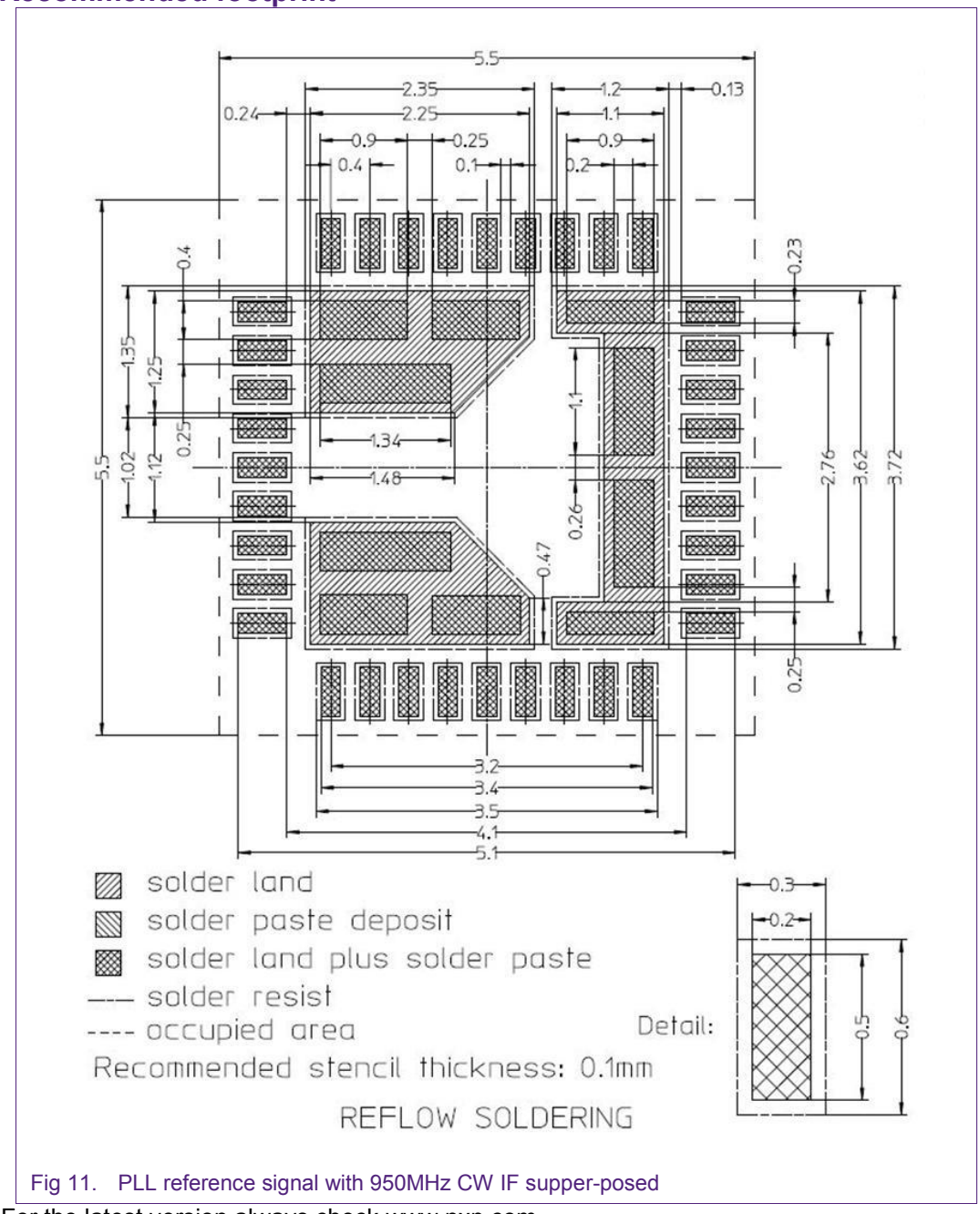

Fig 11. PLL reference signal with 950MHz CW IF supper-posed

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We recommend to connect the ground-planes under the device, keeping the free areas under the center. It is also recommended to connect the GND pins 10, 13, 17, 22, 24, 29, 33, 36 towards the inner ground

6. Do's and Don'ts

6.1 Measuring the TFF1044

The TFF1044 can be evaluated in an isolated environment on NXP's evaluation board OM7980. If required a control board to generate the 13V/18V and 22 kHz pulse via a bias Tee is available, type number ON7981.

6.1.1 Noise Figure

Most LNB parameters can be measured in conventional way, however because a PLL is applied in the LO generation compared to DRO based LNB's differences might be observed. These are mostly related to the PLL reference frequency (XO). When measuring close to the noise floor in the IF spectrum at a XO harmonic frequency spurious might be observed that are not present in DRO based concepts, however with modulated signals under normal operating conditions the spurious ratios do not degrade the BER or MER.

6.1.1.1 Measuring Noise Figure off XO grid

In case noise figure is measured, applying Y-factor method, with a small resolution bandwidth it is recommended to avoid measuring exactly on the XO grid. In that case the C/(N+I) ratio and not the C/N ratio is measured. Avoid measuring on a grid like 950, 1000, 1050 MHz. Alternatively use a frequency grid like 937.5, 987.5, 1037.5 MHz.

6.1.1.2 Measuring Noise Figure at LO spurious

In case noise figure is measured, applying Y-factor method, with a small resolution bandwidth it is recommended to avoid measuring exactly on the LO beat, which is two times the difference in applied LO (2 x (10.6 – 9.75)) = 1.7 GHz. In case noise figure is measured at 1700 MHz the C/(N+I) ratio and not the C/N ratio is measured, as explained in the section above.

6.2 Avoid choosing too high resistor value in the VT detect line

As the VT detect pins draw some current the voltage detected at the pin will be lowered by the resistive losses in the cable and mentioned series resistor. Consequently the threshold for the polarization detection will change. A high resistor value (we recommend 330 Ω) will have less impact on the connected impedance (Zo and Q-factor for the 850 MHz trap filter in case applied) but induce the risk for the LNB not to be switching to the right polarization. See also section 4.1.2 on this.

6.3 Keep symmetry in XO lines

In the PCB layout of the XO lines it is important to keep as much symmetry in the XO lines as possible, especially in case the reference crystal is placed away from the TFF1044. By doing this eventual disturbing signals that enter the XO lines in common mode will be cancelled.

7. Soldering TFF1044 in workshop environment

- TFF1044 has a HVLGA36 (or SOT1359-1) package;
- In the application there is usually a large ground-plane, soldering requires to apply heat from the bottom as well as from the top side;
- In this guide-lines we show how the device can be soldered onto a PCB (for low volumes), or for repair purpose;
- In NXP case a Weller rework station is applied with top and bottom heating.

Preparation step 1, Clean the surface for the TFF1044 soldering pads

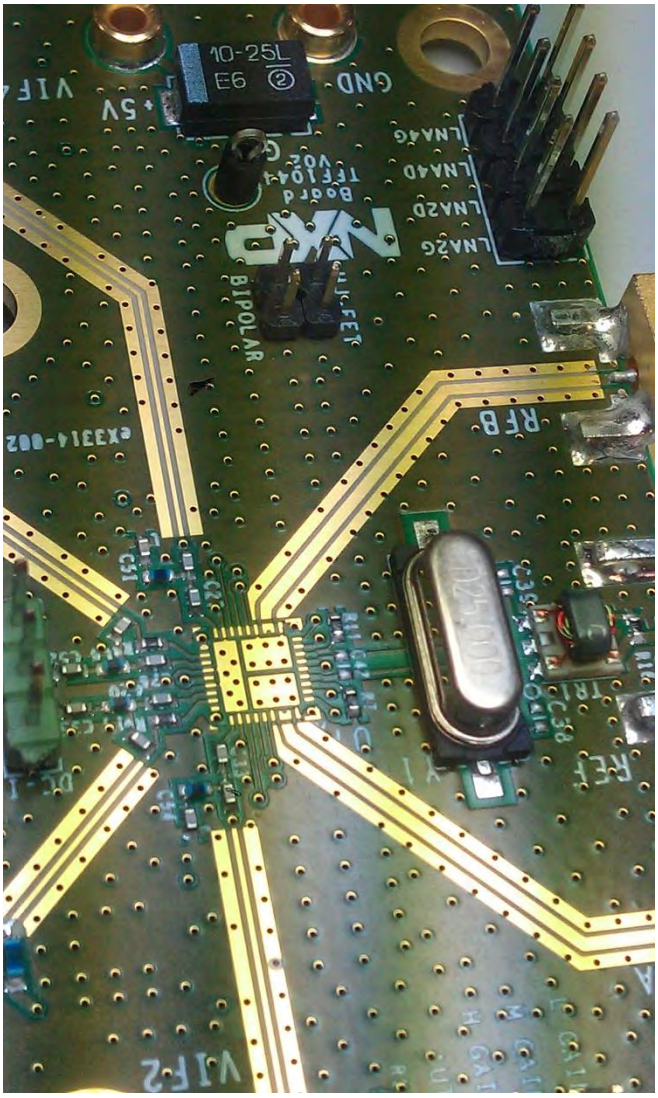

Fig 12. PCB cleaned before assembly

Preparation step 2, Apply the solder paste using a dispenser

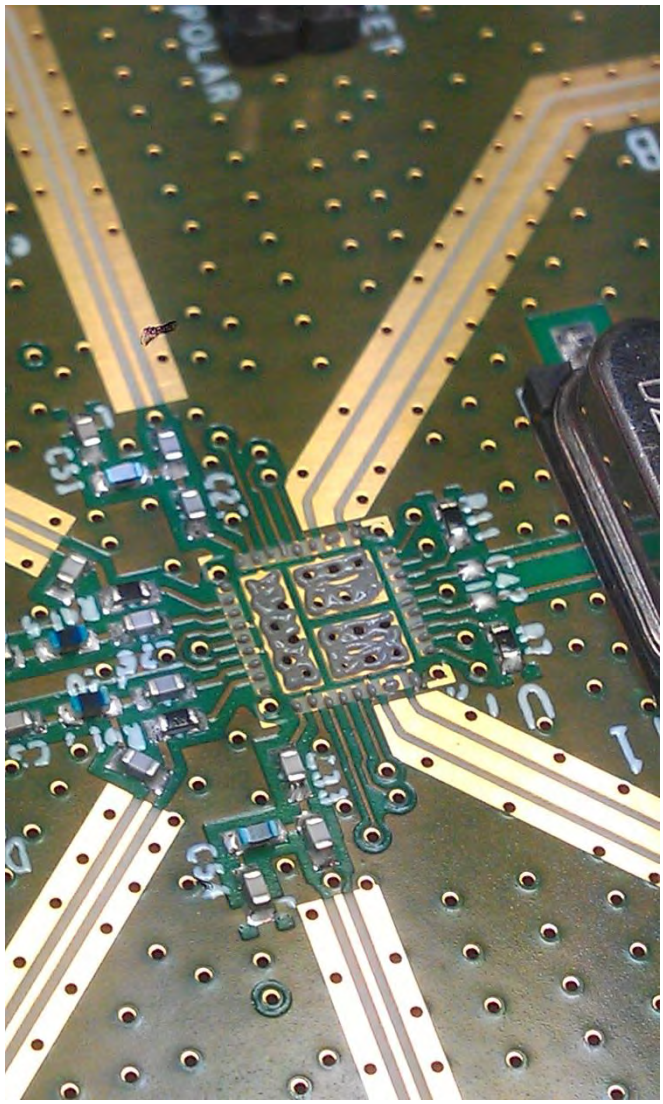

Fig 13. Solder paste applied

The soldering / repair station (Weller)

It is required to apply heat from bottom and top side.

Fig 14. repair station

The soldering process

Just before the soldering process (nozzle up)

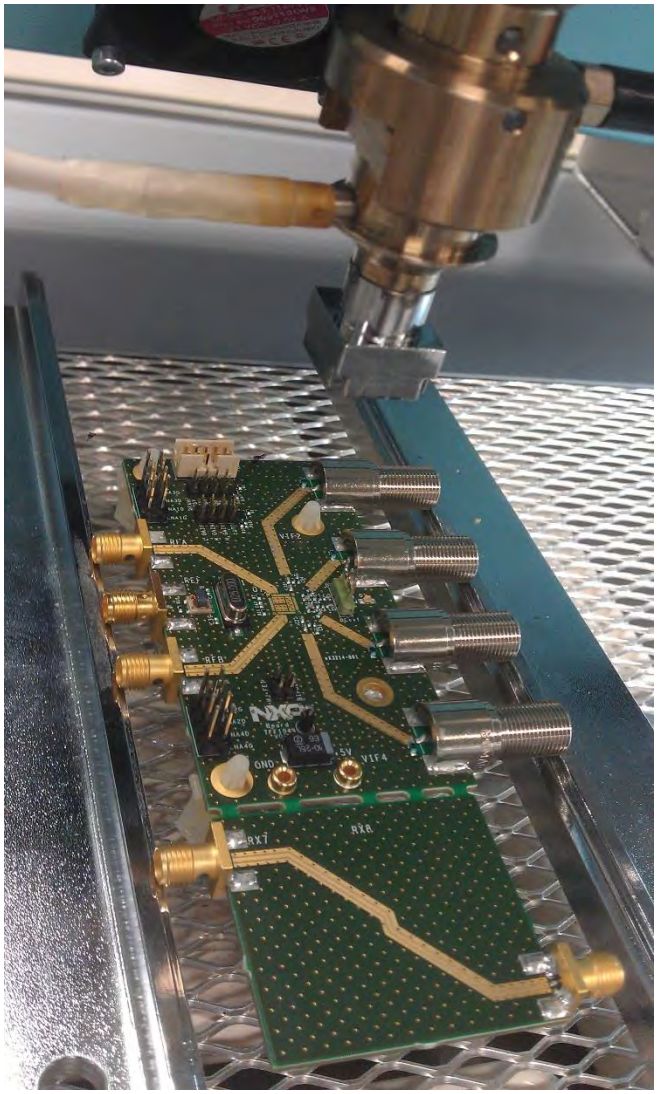

Fig 15. soldering process 1

The soldering process

During the soldering process (nozzle down). The Weller is pre-heated before the soldering process starts.

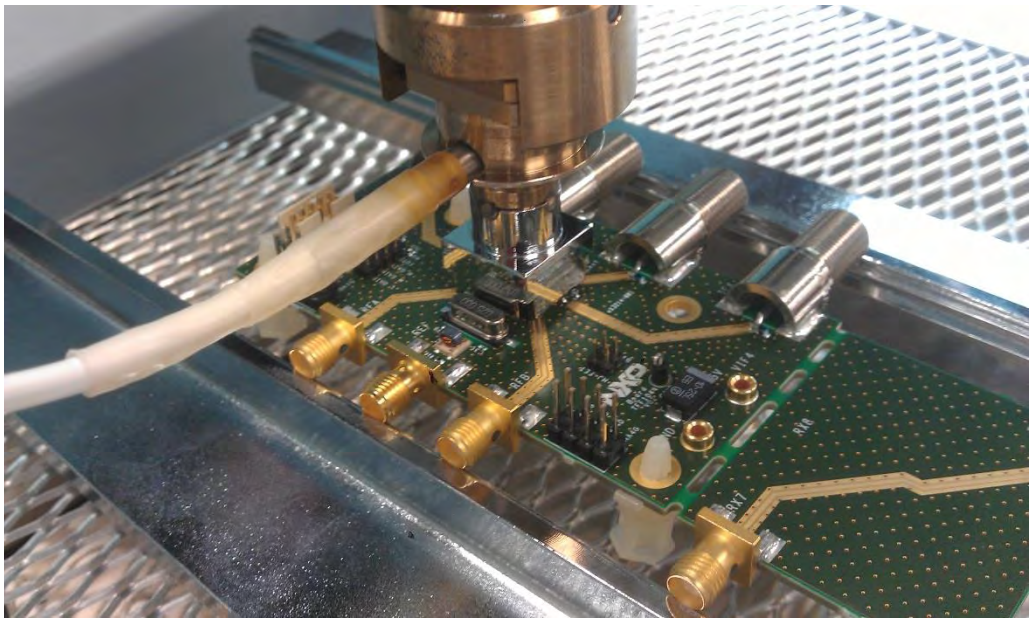

Fig 16. soldering process 2

The soldering process, applied profile

Fig 17. temperature profile applied

The soldering process, visual inspection

The soldered device

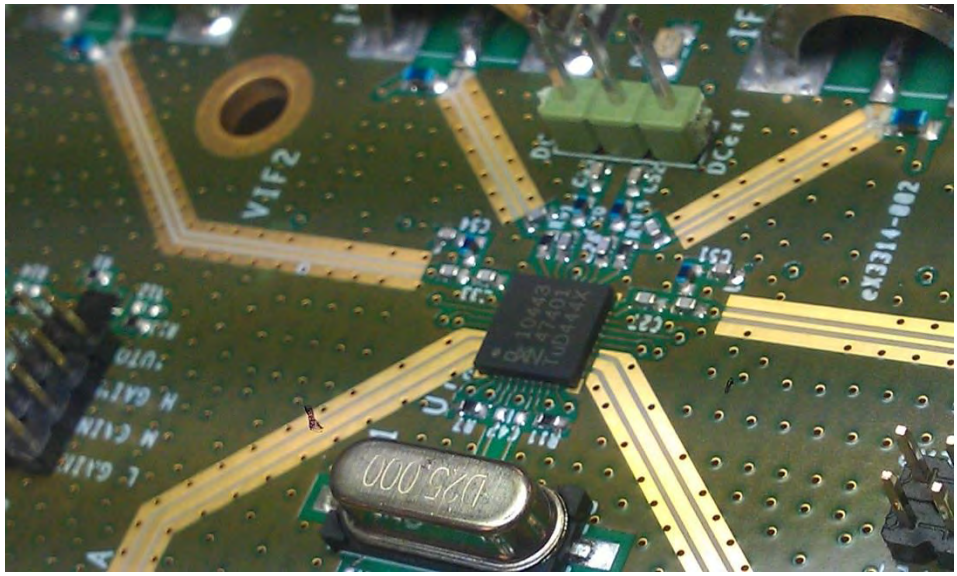

Fig 18. soldered device

The soldering process, X-ray inspection

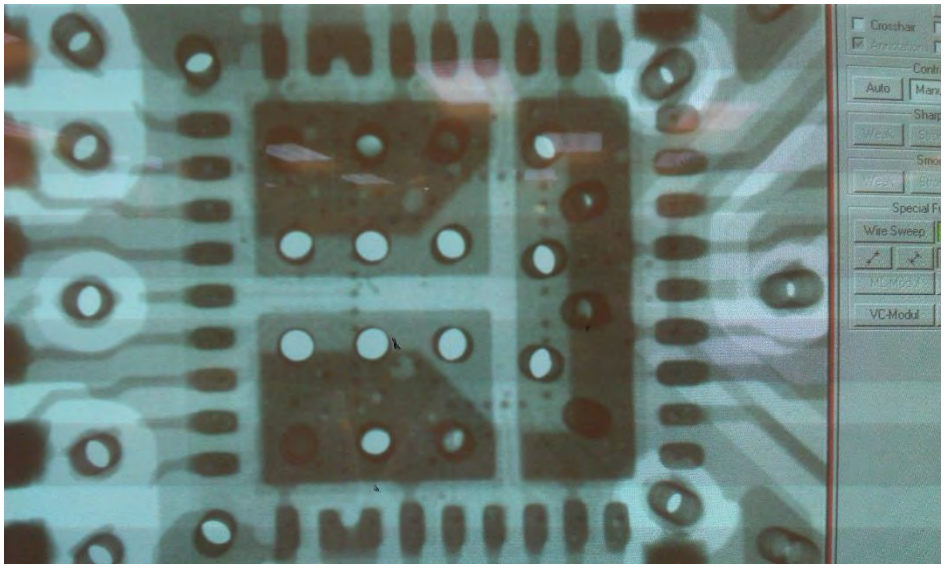

Fig 19. X-ray of soldered device

No short circuits or dry-joints observed, 100% ok!

8. Typical measurement values

8.1 DC voltages at each pin*3):

Pin	Description	Resistance to GND (Ohm)[1]	DC voltage [V][2]
1	1A_DRAIN, drain voltage 1st LNA stage input A	50k	2.1/0
2	1A_GATE, gate voltage 1st LNA stage input A	50k	-0.3[3]/-1.2[4]
3	1AB_ISET, input to set 1st LNA stage quiescent current	32k-10M	2.2[3]/0[4]
4	XOP, crystal pin 1	33k	1.7
5	2AB_TYPSEL, 2nd stage LNA type selection	4M– 5M	2.5
6	XON, crystal pin 2	33k	1.7
7	2AB_ISET, input to set 2nd LNA stage quiescent current	>100M	2.2
8	1B_GATE, gate voltage 1st LNA stage input B	50k	-1[5]/-0.4[6]
9	1B_DRAIN, drain voltage 1st LNA stage input B	50k	0[5]/2.1[6]
10	B_RF_GND, ground to RF B input	0	0
11, 12	B_RFIN	2	0
13	B_RF_GND, ground to RF B input	0	0
14	2B_DRAIN, drain voltage 2nd LNA stage input B	55k	0[5]/2.1[6]
15	2B_GATE, gate voltage 2nd LNA stage input B	65k	0.4[5]/0.8[6]
16	GAIN_SET, input to set conversion gain	80k	1.3
17	GNDIF4	0	0
18	IFOUT4, IF output nr 4	1M	3.2[7]/4.8[8]
19	VTIF4, Voltage/tone detect input for IF4	22k	Vin-0.2
20	VTIF3, Voltage/tone detect input for IF3	22k	Vin-0.2

21	IFOUT3, IF output nr 3	1M	3.2[7]/4.8[8]
22	GNDIF3	0	0
23	VCC, general device supply voltage	22K	5.0
24	GNDIF2	0	0
25	IFOUT2, IF output nr 2	1M	3.2[7]/4.8[8]
26	VTIF2, Voltage/tone detect input for IF2	22k	Vin-0.2
27	VTIF1, Voltage/tone detect input for IF1	22k	Vin-0.2
28	IFOUT2, IF output nr 2	1M	3.2[7]/4.8[8]
29	GNDIF1	0	0
30	POL_SWAP/MODE_SEL	137k	2.5
31	2A_GATE, gate voltage 2nd LNA stage input A	65k	0.8[3]/0.4[4]
32	2A_DRAIN, drain voltage 2nd LNA stage input A	55k	2.1[3]/0[4]
33	A_RFGND, ground to RF A input	0	0
34,35	A_RFIN	2	0
36	A_RFGND, ground to RF A input	0	0

9. Legal information

9.1 Definitions

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10. List of figures

11. Contents

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For sales office addresses, please send an email to: salesaddresses@nxp.com

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