AN11612

LPC11U/E6x Low Power Modes and Wake-up Times

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Document information

Info	Content
Keywords	LPC11U/E6x Low Power Modes Wake- up
Abstract	This application note introduces the low power modes of the LPC11U/E6x series and wake-up implementation. The application note also provides a software example to enter the low power modes and demonstrates how to measure the power consumption and wake-up times using the LPCXpresso11U68 board v2 Rev and v2 Rev C boards.

Revision history

Rev	Date	Description
1	20141208	Initial version.

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1. LPC11U6x Introduction

The LPC11U/E6x is an ARM Cortex-M0+ based, low-cost MCU family operating at CPU frequencies of up to 50MHz. The LPC11U/E6x supports up to 256 KB of flash memory, one 4 KB EEPROM, and 36 KB of SRAM.

The ARM Cortex-M0+ is an easy-to-use, energy-efficient core using a two-stage pipeline and fast single-cycle I/O access.

The peripheral components of the LPC11U/E6x include a DMA controller, a CRC engine, one full-speed USB device controller (on LPC11U6x only) with XTAL-less low-speed mode, two I^2C-bus interfaces, up to five USARTs, two SSP interfaces, PWM/timer subsystem with six configurable multi-purpose timers, a Real-Time Clock, one 12-bit ADC, temperature sensor, function-configurable I/O ports, and up to 80 general-purpose I/O pins.
This application note introduces the various low power modes of the LPC11U/E6x series, the steps required to enter the low power modes and wake-up implementation. This application note also provides software examples to enter and wake-up from the low power modes.
The various topics covered in this application note are as follows:

- Low Power Modes
- Enter Low Power Modes
- Wake-Up Implementation
- Low power mode demo

2. LPC11U6x Power Modes Introduction

On the LPC111U/E6x series, there are four reduced power modes: Sleep, Deep-Sleep, Power-down, and Deep power-down modes. This chapter will describe the various low power modes especially the states of the various peripherals within these power modes. Next chapter will present the details of entering and waking up from these low power modes.

2.1 Sleep mode

In Sleep mode, the system clock to the ARM Cortex-M0+ core is stopped and execution of instructions is suspended until either a reset or an interrupt occurs.

Peripheral functions when enabled in the SYSAHBCLKCTRL register continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

2.2 Deep-sleep mode

In Deep-sleep mode, the system clock to the processor is disabled as in Sleep mode. All analog blocks are powered down by default but can be selected to keep running through the power API if needed as wake-up sources. The main clock and therefore all peripheral clocks are disabled except for the clock to the watchdog timer if the watchdog oscillator is selected. The IRC is running, but its output is disabled. The flash is in stand-by mode.

Deep-sleep mode eliminates all power used by analog peripherals and all dynamic power used by the processor itself, memory systems and related controllers, and internal buses. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

2.3 Power-down mode

In Power-down mode, the system clock to the processor is disabled as in Deep-sleep mode. All analog blocks are powered down by default but can be selected to keep running if needed for waking up the part. The main clock and therefore all peripheral clocks are disabled except for the clock to the watchdog timer if the watchdog oscillator is selected. The IRC itself and the flash are powered down, decreasing power consumption compared to Deep-sleep mode.

Power-down mode eliminates all power used by analog peripherals and all dynamic power used by the processor itself, memory systems and related controllers, and internal buses. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static. Wake-up times are longer compared to the Deep-sleep mode.

2.4 Deep Power-down mode

For maximal power savings, the entire system is shut down except for the general purpose registers in the PMU, the RTC in the VBAT power domain, and the WAKEUP pin if V_{DD} is present. Only the general purpose registers in the PMU and the RTC registers are powered and can maintain their internal states.

2.5 Low Power Modes Summary

Fig 1 shows the parts of the chip that are affected by the various power saving modes.

Below are some notes in regards to Fig 1:

1) As an additional power saving measure in active and Sleep mode, the power to these components can be switched on/off via the Power Configuration Register (PDRUNCFG).

2) The RTC oscillator can be used to wake-up the CPU via interrupt from Sleep, Deep-sleep mode and Power-down mode or Deep power-down mode to provide a timed reset for the CPU from deep power-down mode.

3) The BOD can be used to issue an interrupt to wake-up the CPU from Sleep, Deep-sleep or Power-down mode and will remain at a lower power level during Deep-sleep and Power-down mode.

4) The following peripherals (WD-OSC, WWDT, USB and USART) can be used to wake-up the CPU from Deep-sleep or Power-down mode via interrupt.

5) SRAM1 is turned off by default

	sleep	deep-sleep	power-down	deep power down
cpu-clock	off	off	off	off
main-clock	on	off	off	off
IRC	software configurable (1)	on	off	off
IRC output	software configurable (1)	off	off	off
Flash	On	stand by	off	off
SRAM	On (6)	On (5)	On (5)	off
IO pins	on	on	on	off
BOD	software configurable (1)	software configurable (3)	software configurable (3)	off
PLL	software configurable (1)	off	off	off
USB	software configurable (1)	Software configurable (4)	Software configurable (4)	off
SysOsc	software configurable (1)	off	off	off
WDosc/WWDT	software configurable (1)	software configurable (4)	software configurable (4)	off
USART1/2/3/4	software configurable (1)	off; but can create wake-up in synchronous slave mode or 32kHz clock mode (4)	off; but can create wake-up in synchronous slave mode or 32kHz clock mode (4)	off
RTC	software configurable (1)	software configurable (2)	software configurable (2)	Software configurable (2)
other peripherals	software configurable (1)	off	off	off

Fig 1. Low power modes configurations

3. Entering Low Power Modes and Waking up

The power management unit (PMU) manages the lower power mode entry and wake-up of the core. The PMU is always on as long as VDD or VBAT is present.

3.1 Entering Low Power Modes

Entering and exiting the low power modes is always controlled by the ARM Cortex-M0+ core. The SCR register is the software interface for controlling the core's actions when entering a low power mode. The SCR register is located on the ARM private peripheral bus. The SCR register allows put the ARM core into Sleep mode or the entire system in Deep-sleep or Power-down mode. To enter Deep sleep or Power-down or Deep power-down modes, set bit SLEEPDEEP in register SCR to 1.

Table 1. System Control Register (SCR, address 0xE000 ED10) bit description

Bits	Symbol	Description
0		Reserved
1	SLEEPONEXIT	Indicates sleep-on-exit when returning from Handler mode to Thread mode: 0 = do not sleep when returning to Thread mode. 1 = enter sleep, or deep sleep, on return from an ISR to Thread mode. Setting this bit to 1 enables an interrupt driven application to avoid returning to an empty main application.
2	SLEEPDEEP	Controls whether the processor uses sleep or deep-sleep as its low power mode: 0 = sleep 1 = deep sleep
3		Reserved
4	SEVONPEND	Send Event on Pending bit: 0 = only enabled interrupts or events can wake-up the processor, disabled interrupts are excluded 1 = enabled events and all interrupts, including disabled interrupts, can wake-up the processor. When an event or interrupt enters pending state, the event signal wakes up the processor from WFE. If the processor is not waiting for an event, the event is registered and affects the next WFE. The processor also wakes up on execution of an SEV instruction.

In addition, the corresponding bits in PM in Power Control register (PCON) also need to set accordingly. The power control register selects whether one of the ARM Cortex-M0+ controlled power-down modes (Sleep mode or Deep-sleep/Power-down mode) or the Deep power-down mode is entered and provides the flags for Sleep or Deep-sleep/Power-down modes and Deep power-down modes respectively. See Table 2 for the description of the PCON register.

Table 2. Power control register (PCON, address 0x40038000) bit description

Bit	Symbol	Value	Description
2:0	PM		Power mode
		0x0	Default. The part is in active or sleep mode.
		0x1	Deep-sleep. ARM WFI will enter Deep-sleep mode.
		0x2	Power-down. ARM WFI will enter Power-down mode.
		0x3	Deep power-down. ARM WFI will enter Deep power-down mode.
3	NODPD		A 1 in this bit prevents entry to Deep power-down mode when 0x3 is

Bit	Symbol	Value	Description
			written to the PM field above, the SLEEPDEEP bit is set, and a WFI is executed. This bit is cleared only by power-on reset, so writing a one to this bit locks the part in a mode in which Deep power-down mode is blocked.
7:4			Reserved. Do not write ones to this bit.
8	SLEEPFLAG		Sleep mode flag
		0	Active mode. Read: No power-down mode entered. Part is in active mode. Write: no effect
		1	Low power mode. Read: Sleep/deep-sleep or power-down mode entered. Write: writing a 1 clears the SLEEPFLAG bit to 0.
10:9			Reserved. Do not write ones to this bit.
11	DPDFLAG		Deep power-down flag
		0	Not entered. Read: Deep power-down mode not entered. Write: No effect.
		1	Entered. Read: Deep power-down mode entered. Write: Clear the Deep power-down flag.

The hardware forces the analog blocks to be powered down in Deep-sleep and Power-down modes. Exceptions are the BOD and watchdog oscillator, which can be configured to remain running through this register. The Deep-sleep Configuration Register PDSLEEPCFG can be programmed to control this aspect of Deep-sleep and Power-down modes. The bits are loaded into corresponding bits of the PDRUNCFG register when Deep-sleep mode or Power-down mode is entered.

Table 3. Deep-sleep mode configuration register (PDSLEEPCFG, address 0x40048230)

Bits	Symbol	Value	Description	Reset value
2:0			Reserved	0b111
3	BOD_PD		BOD power-down control for Deep-sleep and Power-down mode	
		1	Powered down	
		2	Powered	
5:4			Reserved	0b11
6	WDTOSC_PD		Watchdog oscillator power-down control for Deep-sleep and Power-down mode	1
		1	Powered down	
		2	Powered	
31:7			Reserved	

3.1.1 Entering and Waking Up from Sleep Mode

3.1.1.1 Entering Sleep Mode

The following steps must be performed to enter Sleep mode:

1. The PM bits in the PCON register must be set to the default value 0x0.
2. The SLEEPDEEP bit in the ARM Cortex-M0+ SCR register must be set to zero.
3. Use the ARM Cortex-M0+ Wait-For-Interrupt (WFI) instruction.

3.1.1.2 Waking up from Sleep Mode

Sleep mode is exited automatically when an interrupt enabled by the NVIC arrives at the processor or a reset occurs. After wake-up due to an interrupt, the microcontroller returns

to its original power configuration defined by the contents of the PDRUNCFG and the SYSAHBCLKDIV registers. If a reset occurs, the microcontroller enters the default configuration in Active mode.

3.1.2 Entering and Waking-up from Deep-sleep Mode

3.1.2.1 Entering Deep-sleep Mode

The following steps must be performed to enter Sleep mode:

1. The PM bits in the PCON register must be set to 0x1.
2. Select the power configuration in Deep-sleep mode in the PDSLEEPCFG register.
3. Determine if the WWDT clock source must be locked to override the power configuration in case the IRC is selected as clock for the WWDT.
4. If the main clock is not the IRC, power up the IRC in the PDRUNCFG register and switch the clock source to IRC in the MAINCLKSEL register. This ensures that the system clock is shut down glitch-free.
5. Select the power configuration after wake-up in the PDAWAKECFG register.
6. Enable the interrupts in the interrupt wake-up registers and in the NVIC if any of the available wake-up interrupts are needed for wake-up.
7. Write one to the SLEEPDEEP bit in the ARM Cortex-M0+ SCR register.
8. Use the ARM WFI instruction.

3.1.2.2 Waking-up from Deep-sleep Mode

The microcontroller can wake-up from Deep-sleep mode in the following ways:

- Signal on one of the eight pin interrupts selected in the PINTSEL0 to PINTSEL7 registers. Each pin interrupt must also be enabled in the STARTERP0 register and in the NVIC.
- BOD signal, if the BOD is enabled in the PDSLEEPCFG register:

  – BOD interrupt using the deep-sleep interrupt wake-up register 1 STARTERP1. The BOD interrupt must be enabled in the NVIC. The BOD interrupt must be selected in the BODCTRL register.
  – Reset from the BOD circuit. In this case, the BOD circuit must be enabled in the PDSLEEPCFG register and the BOD reset must be enabled in the BODCTRL register.
- WWDT signal, if the watchdog oscillator is enabled in the PDSLEEPCFG register:

– WWDT interrupt using the interrupt wake-up register 1 STARTERP1. The WWDT interrupt must be enabled in the NVIC. The WWDT interrupt must be set in the WWDT MOD register.
– Reset from the watchdog timer. The WWDT reset must be set in the WWDT MOD register. In this case, the watchdog oscillator must be running in Deep-sleep mode (see PDSLEEPCFG register), and the WDT must be enabled in the SYSAHBCLKCTRL register.

- USB wake-up signal using the interrupt wake-up register 1 STARTERP1
- GPIO group interrupt signal. The interrupt must also be enabled in the STARTERP1 Register and in the NVIC.
- RTC alarm signal or wake-up signal. Interrupt must also be enabled in the STARTERP1 register and in the NVIC.

3.1.3 Entering and waking up from Power-down Mode

3.1.3.1 Entering Power-down Mode

Following steps must be performed to enter Power-down mode:

1. The PM bits in the PCON register must be set to 0x2.
2. Select the power configuration in Power-down mode in the PDSLEEPCFG register.
3. If the lock bit 5 in the WWDT MOD register is set and the IRC is selected as the WWDT clock source, reset the part to clear the lock bit and then select the watchdog oscillator as the WWDT clock source.
4. If the main clock is not the IRC, power up the IRC in the PDRUNCFG register and switch the clock source to IRC in the MAINCLKSEL register. This ensures that the system clock is shut down glitch-free.
5. Select the power configuration after wake-up in the PDAWAKECFG register.
6. If any of the available wake-up interrupts are used for wake-up, enable the interrupts in the interrupt wake-up registers and in the NVIC.
7. Write one to the SLEEPDEEP bit in the ARM Cortex-M0+ SCR register.
8. Use the ARM WFI instruction.

3.1.3.2 Waking Up from Power-down Mode

The microcontroller can wake-up from Power-down mode in the same way as from Power-down Mode:

- Signal on one of the eight pin interrupts selected in PINTSEL0 to PINTSEL7. Each pin interrupt must also be enabled in the STARTERP0 register and in the NVIC.
- BOD signal, if the BOD is enabled in the PDSLEEPCFG register:
  – BOD interrupt using the interrupt wake-up register 1 STARTERP1. The BOD interrupt must be enabled in the NVIC. The BOD interrupt must be selected in the BODCTRL register.
  – Reset from the BOD circuit. In this case, the BOD reset must be enabled in the BODCTRL register.
- WWDT signal, if the watchdog oscillator is enabled in the PDSLEEPCFG register:
  – WWDT interrupt using the interrupt wake-up register 1 STARTERP1. The WWDT interrupt must be enabled in the NVIC. The WWDT interrupt must be set in the WWDT MOD register.
  – Reset from the watchdog timer. The WWDT reset must be set in the WWDT MOD register.
- USB wake-up signal interrupt wake-up register 1 STARTERP1.

- GPIO group interrupt signal. The interrupt must also be enabled in the STARTERP1 register and in the NVIC.
- RTC alarm signal or wake-up signal. Interrupt must also be enabled in the STARTERP1 register and in the NVIC.

3.1.4 Entering and waking up from Deep Power-down Mode

3.1.4.1 Entering Deep Power-down Mode

The following steps must be performed to enter Deep power-down mode:

1. Pull the WAKEUP pin externally HIGH.
2. Ensure that bit 3 in the PCON register is cleared.
3. Write 0x3 to the PM bits in the PCON register.
4. Store data to be retained in the general purpose registers if needed.
5. Write one to the SLEEPDEEP bit in the ARM Cortex-M0 SCR register.
6. Use the ARM WFI instruction.

3.1.4.2 Wake-up from Deep Power-down Mode using the WAKEUP Pin

Pulling the WAKEUP pin LOW wakes up the part from Deep power-down, and the chip goes through the entire reset process.

1. On the WAKEUP pin, transition from HIGH to LOW.
   – The PMU will turn on the on-chip voltage regulator. When the core voltage reaches the power-on-reset (POR) trip point, a system reset will be triggered and the chip re-boots.
   – All registers except the GPREG0 to GPREG4 and PCON will be in their reset state.
2. Once the chip has booted, read the deep power-down flag in the PCON register to verify that the reset was caused by a wake-up event from Deep power-down and was not a cold reset.
3. Clear the deep power-down flag in the PCON register.
4. (Optional) Read the stored data in the general purpose registers.
5. Set up the PMU for the next Deep power-down cycle.

Remark: The RESET pin on this MCU series has no functionality in Deep power-down mode.

3.1.4.3 Wake-up from Deep Power-down Mode Using RTC

The following steps must be performed to enter Deep power-down mode when using the RTC for waking up:

1. Set up the RTC high-resolution timer. Write to the RTC VAL register. This starts the high-resolution timer if enabled. Another option is to use the 1 Hz alarm timer.
2. Ensure that bit 3 in the PCON register is cleared.
3. Store data to be retained in the general purpose registers if needed.
4. Use the ARM WFI instruction.

The part goes through the entire reset process when the RTC times out:

1. When the high-resolution timer count reaches 0, the following happens:
   – The PMU will turn on the on-chip voltage regulator. When the core voltage reaches the power-on-reset (POR) trip point, a system reset will be triggered and the chip boots.
   – All registers except the GPREG0 to GPREG4 registers and PCON will be in their reset state.

2. Once the chip has booted, read the deep power-down flag in the PCON register to verify that the reset was caused by a wake-up event from Deep power-down and was not a cold reset.
3. Clear the deep power-down flag in the PCON register.
4. (Optional) Read the stored data in the general purpose registers.
5. Setup the PMU for the next Deep power-down cycle.

3.1.5 Other power consumption reduction considerations

- Handling of unused pins. Please refer to function HandleUnusedPins() for particular handling of the LPCxpresso11U68 v2 Rev B and Rev C board. General guidelines are always putting unused pins to a know state. With the LPCXpresso11U68 board, unused pins are configured as output low with both internal pull up and pull down disabled.
- If peripheral clocks are not used, reduce the peripheral clocks before going into the low power modes also helps with the low power mode power consumption.

4. Low Power Mode Demos

This application note provides examples to enter all above mentioned low power modes and waking-up from Pin interrupt for Sleep, Deep-sleep and Power-down mode. For waking up from Deep Power-down mode, the WakeUP pin is used.

4.1 Software and Hardware Setup

4.1.1 Software

The examples are based on NXP's LPCOpen 2.06 software platform and are verified with below three the IDEs:

Keil IDE 5.12

IAR IDE 7.20

LPCXpresso IDE 7.50

Zip file "\Keil_IAR_LowPowerMode.zip" contains the software for implementation based on Keil and IAR IDE. User should unzip the Keil/IAR project to a folder for testing. For the Keil project, the CMSIS-DAP debug probe firmware is used. The Link2 Configuration Tool required to program the CMSIS-DAP debug probe firmware into the LPCXpresso11U68 board can be downloaded from lpcware at:

http://www.lpcware.com/lpclink2-config-tool

Zip file "LPCXpresso_LowPowerMode.zip" contains the software implementation based on LPCXpresso IDE. The user should import these projects to an LPCXpresso IDE workspace for testing. For the LPCXpresso IDE projects, the redlink debug probe firmware is used. User should jumper JP3 on the LPCXpresso11U68. Please refer to Fig 3 and Fig 4 for the location of JP3. IDE Optimization used for these projects is illustrated in Fig 2.

With these sample projects, the PLL output of 48MHz is used as the main clock when the system starts. Before entering any of the low power modes, the main clock is switched to

IRC at 12MHz and PLL is powered down. On waking-up from low power modes, the PLL is powered on and the main clock is switched back to the PLL output at 48MHz.

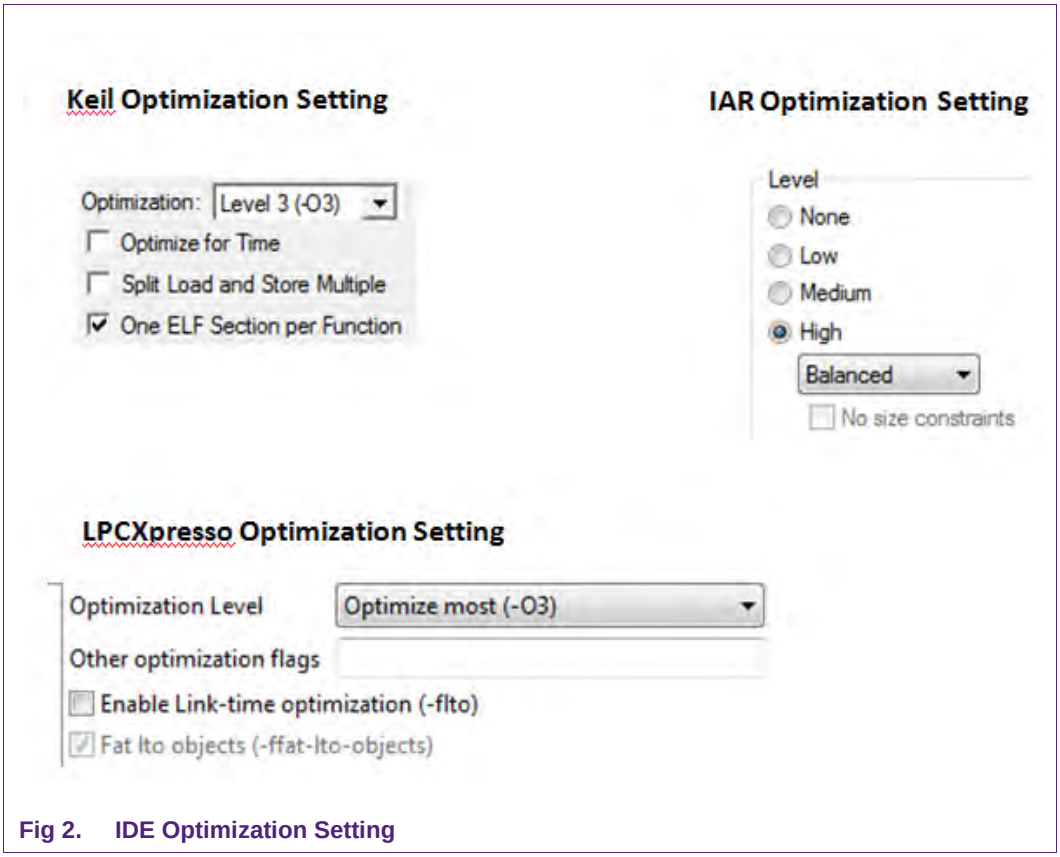

Fig 2. IDE Optimization Setting

4.1.2 Hardware

The LPCXpresso11U68 development board v2 Rev. B and v2 Rev C are used for the low power mode entry and exit example. For information on the LPCxpresso11U68 development boards see the lpcware page:

http://www.lpcware.com/LPCXpressoV2Boards

To measure the power consumption and wake-up time of LPC11U68, the following rework must be done to the v2 Rev B board.

1. R68 is removed to get rid of LED D7 power consumption (see Fig 3 for position of R68) R67 on Rev C board
2. R65 is remove so the CPU's power consumption can be measured on P3 (see Fig 3 for position of R65)
3. Install jumper at P3 to allow the current meter to be attached (see Fig 3 for position of P3)
4. Connect a wire out from WAKEUP pin at R63 to allow the wake-up time to be measured (see Fig 3 for position of R63)

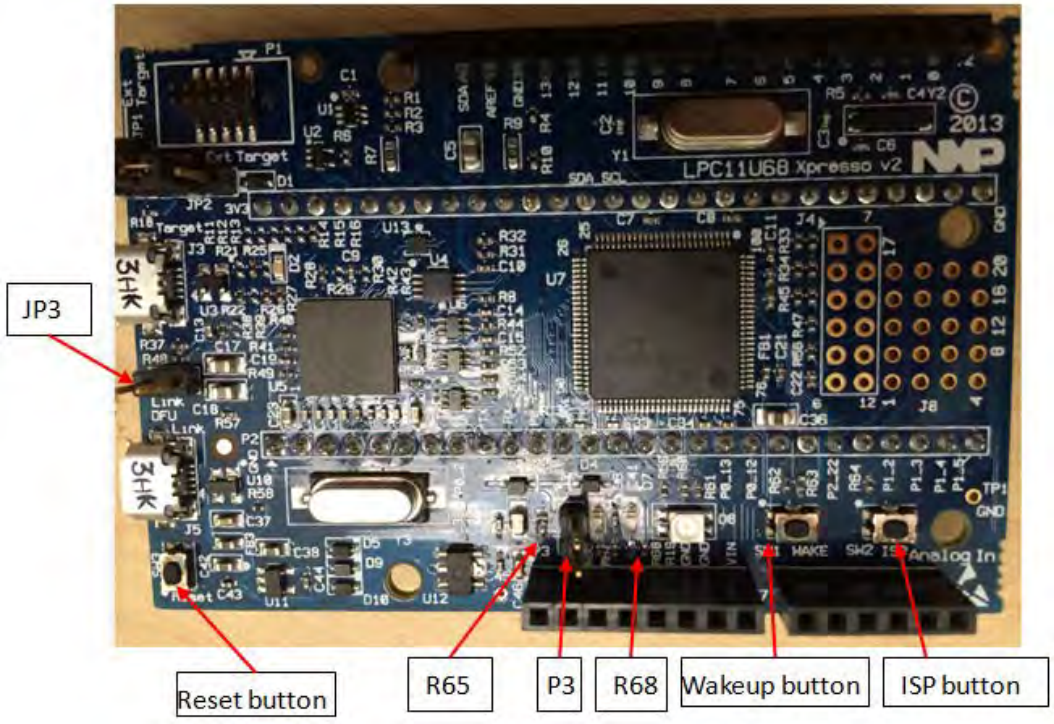

Fig 3. LPCXpresso11U68 Board v2 Rev. B

To measure the power consumption and wake-up time of LPC11U68, the following reword must be done to the v2 Rev. C board.

1. R67 is removed to get rid of LED D9 power consumption (see Fig 4 for position of R67)
2. SJ1 is remove so the CPU's power consumption can be measured on P3 (see Fig 4 for position of JS1)
3. Install jumper at P3 to allow the current meter to be attached (see Fig 4 for position of P3)
4. Install posts on GND and P0_7 (see Fig 4 for position of P0_7)
5. Connect a wire out from WAKEUP pin at R62 to allow the wake-up time to be measured (see Fig 4 for position of R62)

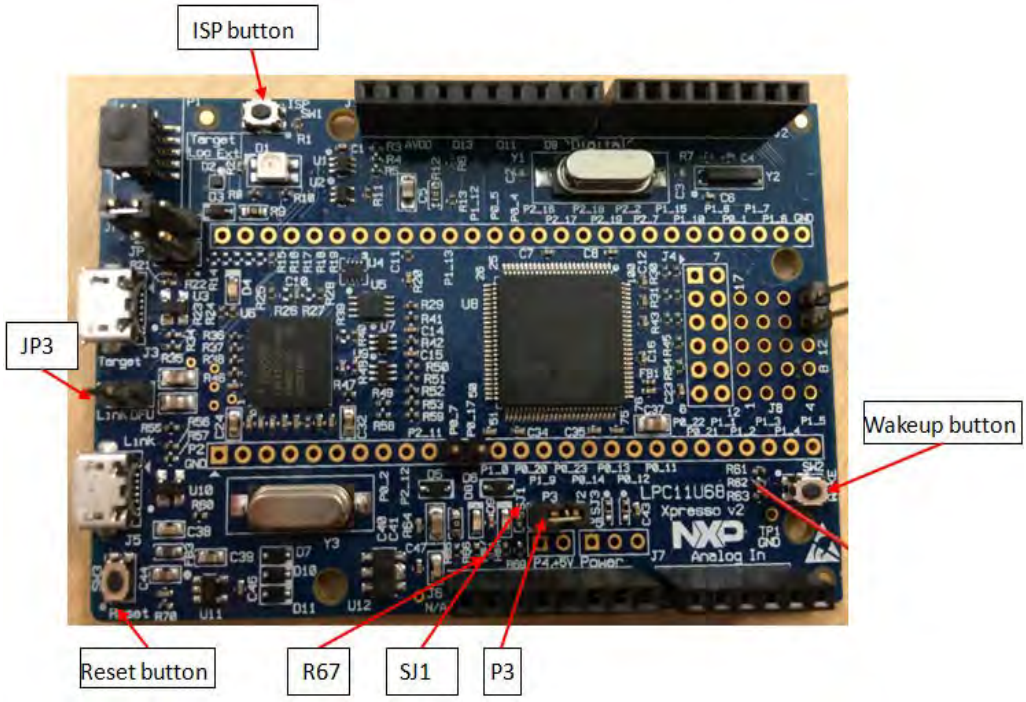

Fig 4. LPCXpressp11U68 Board v2 Rev. C

To switch the software project between Rev B and Rev C board below definition needs to be handled.

```
//define LPCxpresso11U68 _v2_RevC as 0 to select Rev B board
#define LPCxpresso11U68_v2_RevC     1
```

Fig 5. Switch between Rev. B and Rev. C

4.2 Low power mode power consumption measurement steps

Use the following steps for the low power consumption measurement. Notice that Fig 6 uses LPCxpresso11U68 v2 Rev C hookup as example.

1. Connect current meter to P3. See Fig 6.
2. Connect power and Link2 on board debugger from J5 to PC through USB cable. See Fig 6.

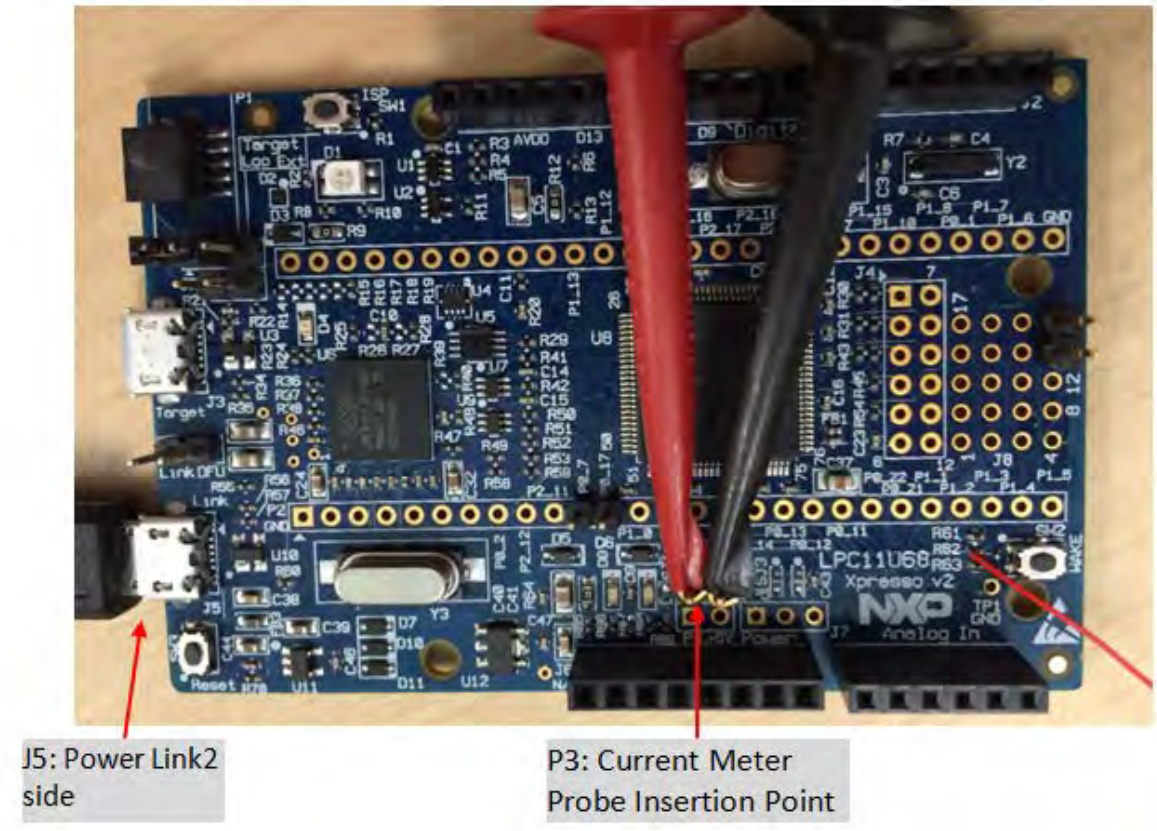

Fig 6. Current Meter Hook up and Wake-up Line Hook up with LPCXpresso11U68 v2 Rev C board

3. Select which measurement to perform by uncommenting the particular line of code. In Fig 7, the sleep mode is selected.

```
#define CURRENT_POWER_SETTING      PMU_MCU_SLEEP
// #define CURRENT_POWER_SETTING      PMU_MCU_DEEP_SLEEP
// #define CURRENT_POWER_SETTING      PMU_MCU_POWER_DOWN
// #define CURRENT_POWER_SETTING      PMU_MCU_DEEP_PWRDOWN
```

Fig 7. Selection of Low power mode

4. Define the measurement to be Power Consumption Measurement

```
#define CURRENT_MEASUREMENT_MODE 1
```

Fig 8. Define CURRENT_MEASUREMENT_MODE

5. Compile the project and download the executable to LPC11U68. Stop the debug session to disconnect the debugger.

6. Press the reset button (see Fig 4 for location of reset button)
7. Press the ISP button (see Fig 4 for location of reset button)
8. Take the current measurement from the current meter.

4.3 Wake-up Time Measurement Steps

In this application note, the wake-up time from Sleep, Deep-sleep and Power-down modes is measured from the WAKEUP IO line (P0_16) being pulled low to the first instruction executed in the interrupt service routine. This first instruction in the interrupt service routine in this demo is to pull another IO line (P0_7) from low to high.

The wake-up time from Deep power-down is measured from the WAKEUP pin (P0_16) being pulled low to the first IO line (P0_7) being pulled from low to high during system initialization.

For Cortex-M0+, the maximum interrupt latency is 15 with the zero wait state configuration. Therefore, the measured wake-up time from Sleep, Deep-sleep, Power-down mode is 1.33us longer than the LPC11U68's true wake-up time.

Use the following steps for the wake-up time measurement.

1. Short jumper P3.
2. Connect P0_16 WAKEUP pin to oscilloscope trigger input as shown in Fig 9.
3. Connect P0_7 to another oscilloscope trace as shown in Fig 9.

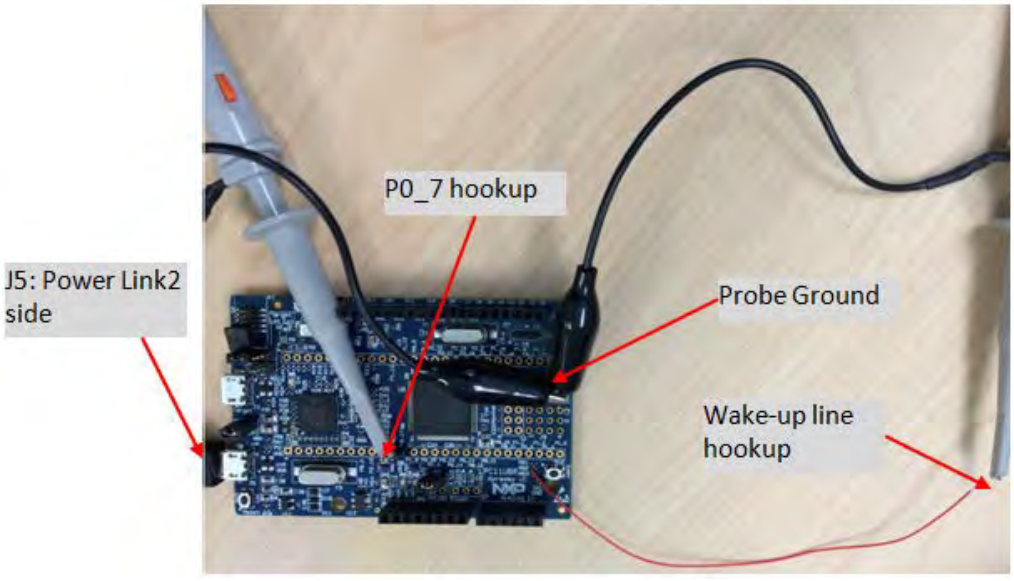

Fig 9. Wake-up Time Measurement Setup with LPCXpresso11U68 v2 Rev B board

4. Connect power and link2 on board debugger to PC through J5.
5. Select which measurement to perform by uncommenting the particular line of code as shown in Fig 7.

6. Set the Power Consumption Measurement mode to 0.

```
#define CURRENT_MEASUREMENT_MODE        0
```

Fig 10. Define CURRENT_MEASUREMENT_MODE to be 0

7. Compile the project and download. Stop the debug session to disconnect the debugger.
8. Press the reset button (see Fig 4 for location of reset button)
9. Press the ISP button (see Fig 4 for location of ISP button)
10. Press the Wake-up button (see Fig 4 for location of Wake-up button)
11. For wake-up time from Sleep, Deep-sleep, Power-down modes, measure time passed on the oscilloscope between WAKEUP pin (P0_16) going low to P0_7 going high. See Fig 11.

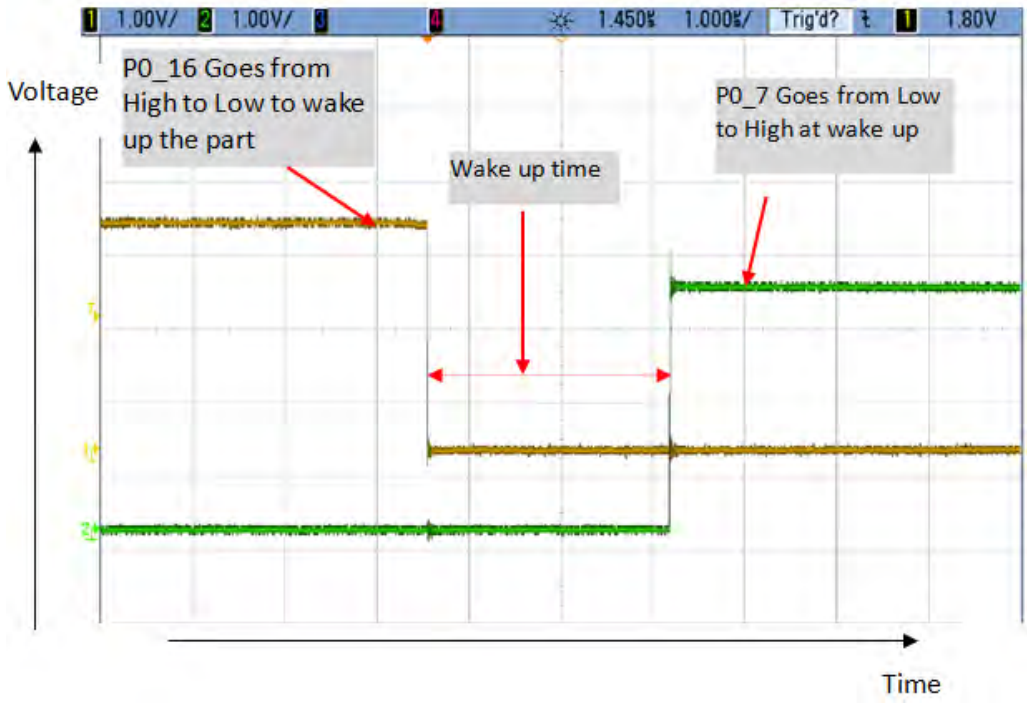

Fig 11. Wake-up Time Measurement from Sleep, Deep-sleep, Power-down Modes

For wake-up time from Deep Power-down mode, measure the time passed on the oscilloscope between WAKEUP pin (P0_16) going low to P0_7 being toggled after the chip has finished power on reset steps. See Fig 12.

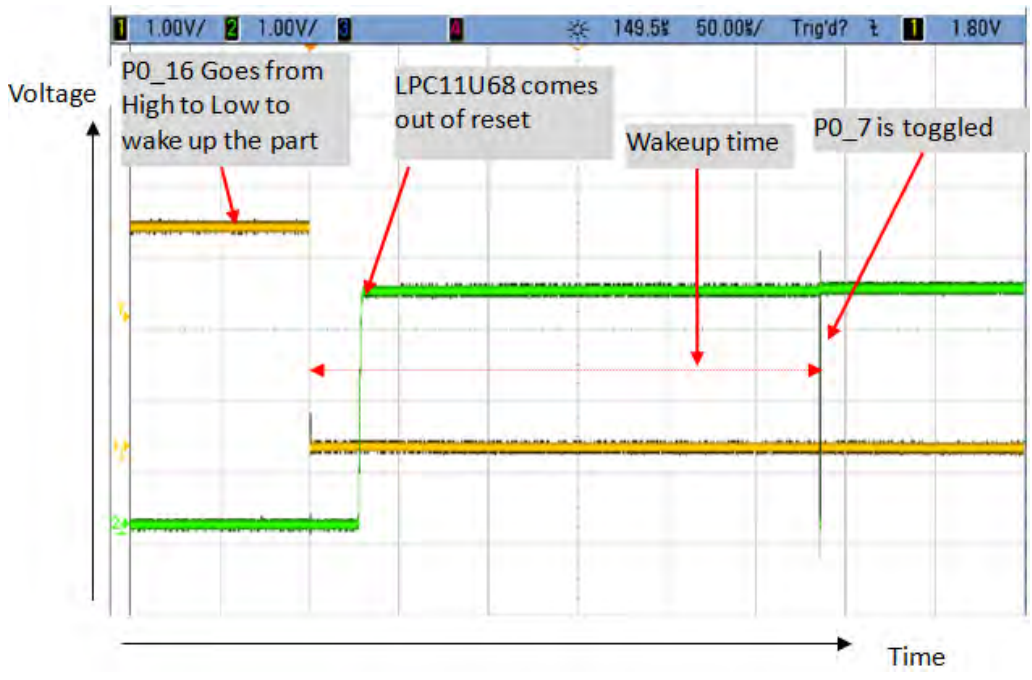

Fig 12. Wake-up Time Measurement from Deep Power-down Mode

To acquire the wake-up time from LPCXpresso IDE, the P0_7 line toggle is done in the ResetISR in cr_startup_lpc11u6x.c. See Fig 13.

```
//*****************************************************************
**********
__attribute__ ((section(".after_vectors")))
void
ResetISR(void) {

                                        …
    // Ensure that RAM1(26) and USBSRAM(27) bits in SYSAHBCLKCTRL are
set
    *SYSCON_SYSAHBCLKCTRL |= (1 << 26) | (1 <<27);
#endif

/* For Deep Power Down wake-up time measurement*/
    LPC_SYSCTL->SYSAHBCLKCTRL |= (1 << SYSCTL_CLOCK_IOCON);
     /* set pin P0.7 to output mode to do the wake-up time
measurement*/

     LPC_GPIO->DIR[0] |= 1UL << 7;
```

```
    LPC_GPIO->B[0][7] = 1;
```

Fig 13. LPCXpresso IDE ResetISR

To acquire the wake-up time from Deep Power-down from Keil/IAR, the P0_7 toggle is done in the sysinit_11u6x.c. See Fig 14.

```
void Chip_SetupIrcClocking(void)
{
    /* For Deep Power Down wake-up time measurement*/
    LPC_SYSCTL->SYSAHBCLKCTRL |= (1 << SYSCTL_CLOCK_IOCON);
    /* set pin P0.7 to output mode to do the wake-up time measurement*/
    LPC_GPIO->DIR[0] |= 1UL << 7;
    LPC_GPIO->B[0][7] = 1;

                                                    ...
```

Fig 14. Keil/IAR sysinit_11u6x.c

4.4 Typical Low Power Mode Power Consumption and Wake-up Times

Table 4 shows some measurement results with one set of LPCXpresso11U68 development boards – one v2 Rev B board and one v3 Rev C board. The wake-up time and power consumption is very close to the datasheet specification. Results with all three IDEs are very close on either board. Your result of running on a particular board may have some variation from these results.

Table 4. Low Power Mode Power Consumption and Wake-up Time (VDD=3.3V, Room Temperature) on LPCXpresso11U6x board

Low Power Mode	Wake up time (us) (all IDE correlate)	Power Consumption (v2_Rev B)	Power Consumption (v2_Rev C)
Sleep mode	2.94	1.44mA	1.44mA
Deep-sleep mode	4.87	270uA	261uA
Power-down mode	92.6	7.1uA	5.3uA
Deep power-down	282	1.67uA	1.45uA

5. Conclusion

The LPC11U/E6x series MCU provides various options for users to achieve low power consumption and wake-up flexibility. As shown in Table 1 and Table 2, the user has various low power mode options to choose from in order to achieve the desired power consumption by trading up or down the wake-up time of the device.

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