AN11491

Design and application guidelines for the COG LCD drivers PCF8538 and PCA8538

Rev. 1 — 9 January 2014　　　　　　　　　　　　　　　　**Application note**

Revision history

Rev	Date	Description
1	20140109	Initial release

Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

AN11491

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Application note **Rev. 1 — 9 January 2014** **2 of 25**

1. Introduction

The PCF8538 and PCA8538 are fully featured Chip-On-Glass (COG) Liquid Crystal Display (LCD) drivers, designed for high-contrast Vertical Alignment (VA) LCD with multiplex rates up to 1:9. They generate the drive signals for a static or multiplexed LCD containing up to 9 backplanes, 102 segments, and up to 918 elements. They feature an internal charge pump with internal capacitors for on-chip generation of the LCD driving voltage. To ensure an optimal and stable contrast over the full temperature range, the PCF8538 and PCA8538 offer a programmable temperature compensation of the LCD supply voltage. They can be easily controlled by a microcontroller through either the two-line I^2C-bus or a four-line bidirectional SPI-bus.

The PCF8538U is qualified for industrial and consumer applications; the PCA8538U is qualified according the AEC-Q100 grade 2 standard that makes the product suitable for automotive applications. For further information please refer to the appropriate data sheets.

This application note provides additional information about using these drivers. In the remainder of this document, PCF8538 and PCA8538 are also referred to as PCx8538.

2. Display technologies which can be driven

The PCF8538U and the PCA8538U are suitable to drive any monochrome LCD technology like TN (Twisted Nematic) and STN (Super Twisted Nematic), including also the newer Vertical Alignment (VA) displays, which impose stricter requirements on the driver.

Vertical Alignment is a display technology in which the liquid crystals naturally align vertically to the glass substrates. When no voltage is applied, the liquid crystals remain perpendicular to the substrate creating a black display between crossed polarizers; when a voltage is applied, the liquid crystals shift to a horizontal position allowing light to pass through and create a white display image. Compared to the traditional TN displays, VA displays have a deeper black background, a much higher contrast ratio, a much wider viewing angle and better image quality at extreme temperatures.

This display technology is particularly well suited for applications where the display is:

- exposed to sunlight, i.e. needs to be sunlight readable
- mounted on an otherwise black background, e.g. in instrument clusters in a car
- located sideways from the viewer, e.g. in the centre stack of a car, and thus needs to be viewable under a wide angle. VA displays are in growing demand for both automotive and non-automotive applications.

Compared to TN and STN displays, the VA display technologies have different requirements with respect to the drive signals, mainly in terms of higher LCD supply voltage V_{LCD} and higher frame frequency. In order to meet these requirements and to be able to drive the VA displays, the PCF8538U and the PCA8538U have been designed with higher V_{LCD} which is programmable up to 12 V, and higher frame frequency, programmable up to 300 Hz.

3. Possible display configurations

The PCF8538U and the PCA8538U are suitable to drive any display, containing up to 918 elements. The display configurations possible depend on the number of active backplane outputs (commons) required. A selection of possible display configurations is given in Table 1.

Table 1.   Selection of possible display configurations

Number of				
Backplanes	**Icons**	**Digits/characters**		**Dot matrix/ Elements**
		7-segment	**14-segment**	
9	918	114	57	918 dots (9 x 102)
8	816	102	51	816 dots (8 x 102)
6	612	76	38	612 dots (6 x 102)
4	408	51	25	408 dots (4 x 102)
2	204	25	12	204 dots (2 x 102)
1 (static mode)	102	12	6	102 dots (1 x 102)

Some examples are shown below.

3.1 Dot matrix display

The PCF8538U and the PCA8538U can drive a dot matrix display up to 9 x 102 dots. See Fig 1.

Example, not full number of columns shown.

Fig 1.   Dot matrix display
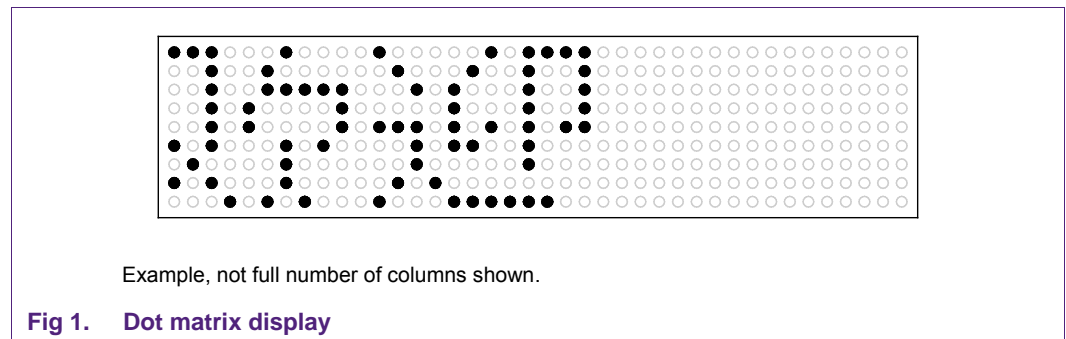
3.2 Dot matrix displays with icons

The PCF8538U and the PCA8538U can drive a dot matrix display that includes also some icons or segments, according to the specific applications. The total number of display elements (icons, segments and dots) is up to 918. This is illustrated in Fig 2.
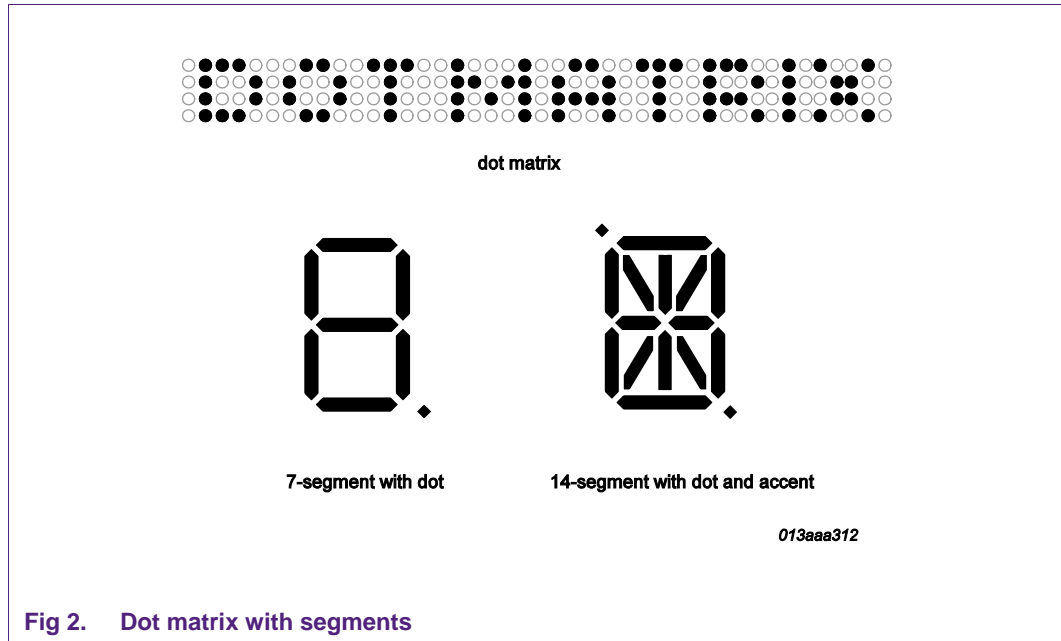
AN11491

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Application note **Rev. 1 — 9 January 2014** **4 of 25**

Fig 2. **Dot matrix with segments**

3.3 Segmented displays

The PCF8538U and the PCA8538U can drive a segmented display up to 918 segments. The example below shows a display where a considerable number of segments is used, along with a small dot-matrix section. This display is used on the demo board, refer to section 9, demo board.
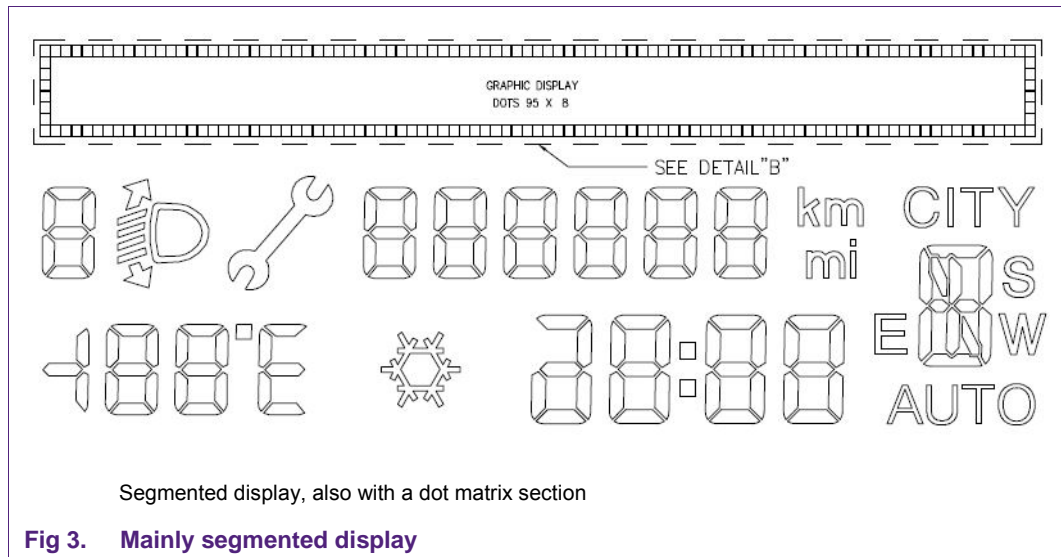

Segmented display, also with a dot matrix section

Fig 3. **Mainly segmented display**

AN11491

Application note **Rev. 1 — 9 January 2014** **5 of 25**

4. Maximum display size that can be driven

In this section, an estimation of the maximum display element dimensions (pixel, icon, segment) that can be used in conjunction with the PCx8538 is discussed. The display size is related to this. Given the maximum size of a display element and the number of display elements, the display size can be derived.

The maximum size of the display elements that can be driven by the PCF8538U or the PCA8538U depends not only on the driver but also on the display characteristics. The relevant parameters are the following:

- The output resistance of the LCD driver outputs (segment and backplane/common outputs)
- The segment and backplane ITO track resistances
- The capacitance of the display element

The various parameters are indicated in Fig 4.

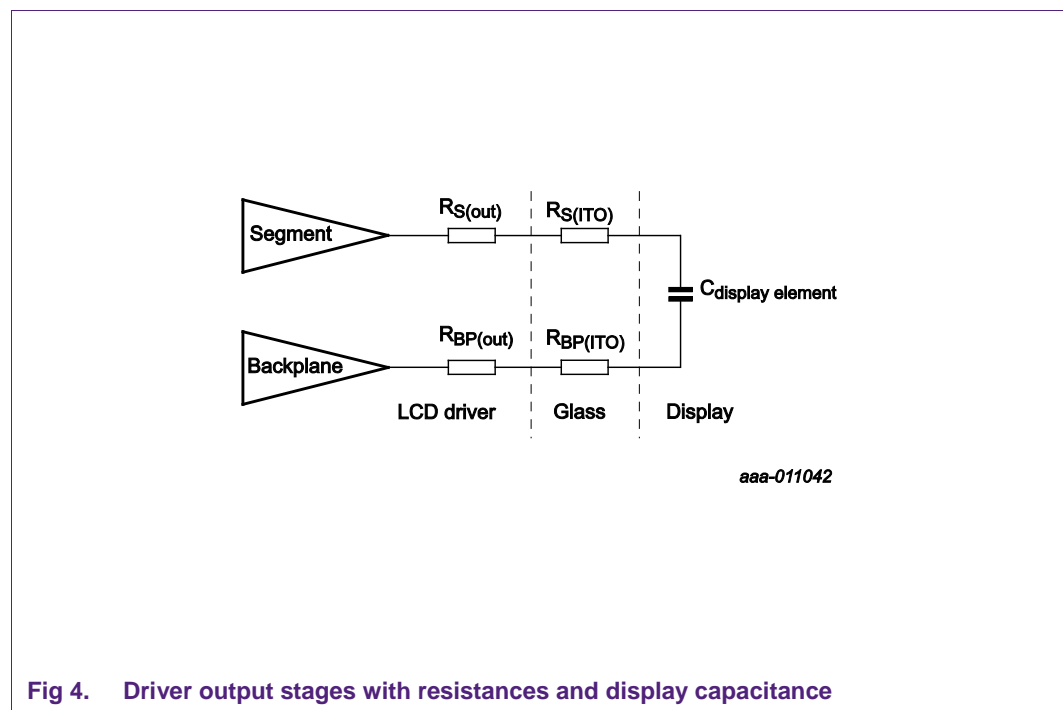**Fig 4.   Driver output stages with resistances and display capacitance**

Note: The calculations given in this example are valid for the PCF8538 and PCA8538. However, the way of working is universal and can be used to determine the maximum display element size that can be driven by any LCD driver. Obviously, the parameter values must be adapted to the actual values.

4.1 The output resistance of the LCD outputs

The output resistances of the PCx8538U are specified as follows:

- $R_{o\,(SEG)}$ = 2.5 kΩ (typ.)
- $R_{o\,(COM)}$ = 1.0 kΩ (typ.)

4.2 Segment and common ITO track resistances

The segment and common ITO track resistances depend on the module design. Factors determining the resistance are length and width of the tracks and the sheet resistance (square resistance) of the ITO, which can be influenced by varying the thickness.

For the segment ITO track, the following assumptions are made:

- One bump per segment; bump pitch: 45 μm
- SEG ITO track width: 45 μm
- SEG ITO track length: 70 mm (worst case)
- SEG ITO number of squares: 1555
- $R_{(ITO)}$ = 15 Ω / square
- $R_{SEG(ITO)}$ = 23.3 kΩ

For the common ITO track, the following assumptions are made:

- Two bumps per segment; bump pitch: 90 μm
- COM ITO track width: 500 μm
  Note: Typically, there is much more space available for a common track than for a segment track.
- COM ITO track length: 150 mm (worst case)
- COM ITO number of squares: 300
- $R_{(ITO)}$ = 15 Ω / square
- $R_{COM(ITO)}$ = 4.5 kΩ

Actual track length may be much less, which will have a positive influence on the display size that can be driven.

Note that the LCD drive section includes nine backplane outputs: COM0 to COM8. The backplanes are double implemented (two sets of outputs) to offer a higher flexibility for the glass layout. If the correspondent COM outputs are connected together, the drive strength will be further increased.

4.3 Pixel capacitance

The pixel capacitance depends on the display technology, the liquid used, the pixel size and on the state (ON or OFF). A display manufacturer could provide the value of the display capacitance per mm^2 or the value of the total display capacitance, and then the average pixel capacitance can be derived.

A pixel capacitance of 10 pF / mm^2 is a realistic value.

4.4 Drive capability

A display element forms a capacitor, and it must be charged and discharged when switching ON and OFF. As a rule of thumb, the actual waveform should be at 95% of its value within 10 % of the selection time slot, which is the pulse width. Considering the default case (multiplex mode 1:9, bias mode ¼, line inversion and frame frequency equal to 80 Hz), the selection time slot is equal to the frame period divided by 18, see Fig 5, that is about 694 μs. In general, the selection time slot is equal to the frame frequency divided by the multiplex rate n.

The total cell capacitance is hard to estimate due to the display appearing as a network, with many resistances and capacitances. A segment output will only drive a small portion of the display whereas a common output drives a much larger portion of the display. Therefore it is necessary to look at the drive capability separately.

More in to detail:

$$3 \times R_{SEG(tot)} \times C \ \le \ 10\% \times 694\mu s = 69.4 \ \mu s \qquad (1)$$

$$3 \times R_{COM(tot)} \times C \times N \le 10\% \times 694\mu s = 69.4\mu s \qquad (2)$$

Where:

- $R_{SEG(tot)}$ is the total output resistance of each segment output, which is the sum of the on-chip output resistance of the segment output driver (see section 4.1) plus the resistance of the segment ITO track (see section 4.2); that is: $R_{SEG(tot)}$ = 2.5 kΩ + 23.3 kΩ = 25.8 kΩ (typ.);

- $R_{COM\ Tot.}$ is the total output resistance of each common output, which is the sum of the on-chip output resistance of the common output driver (see section 4.1) plus the resistance of the common ITO track (see section 4.2); that is: $R_{COM(tot)}$ = 1.0 kΩ + 4.5 kΩ = 5.5 kΩ (typ.);

- N is the total number of segments per each common line, here that is 102;

- C is the pixel capacitance.

From equation (1):
$$C \le 69.4\mu s /\left(3 \times R_{SEG(tot)}\right) = 69.4 \ \mu s /77.4 \ k\Omega = \ \sim 900 \ \text{pF} \qquad (3)$$

From equation (2):
$$C \le 69.4\mu s /\left(3 \times R_{COM(tot)} \times 102\right) = 69.4 \ \mu s /1683 \ k\Omega = \ \sim 41 \ \text{pF} \qquad (4)$$

From equations (3) and (4) follows that the maximum pixel capacitance is about 41 pF. However, considering the tolerance of the semiconductor process as well as the tolerance of the ITO track resistance, it is assumed that $R_{COM(tot)}$ = 8 kΩ (max.). Using this value instead of the typical value of 5.5 kΩ, equation (4) is rewritten as follows:

$$C \le 69.4\mu s /\left(3 \times R_{COM\ Tot} \times 102\right) = 69.4 \ \mu s /2448 \ k\Omega = \ \sim 28.35 \ \text{pF} \qquad (5)$$

$$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t).$$

$$V_{on(RMS)}(t) = 0.408V_{LCD}.$$

(1) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t).$

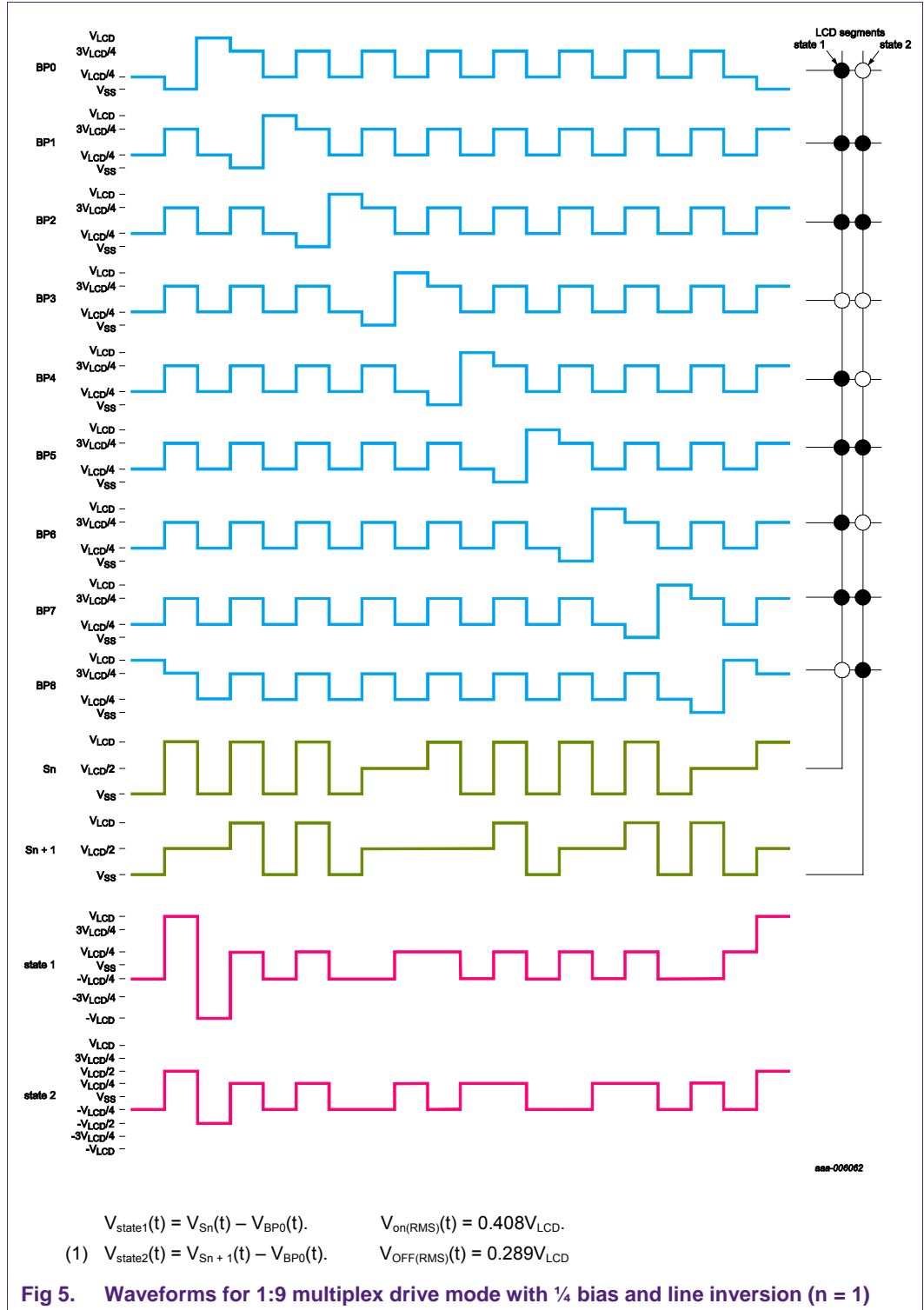$$V_{OFF(RMS)}(t) = 0.289V_{LCD}$$

Fig 5.   Waveforms for 1:9 multiplex drive mode with ¼ bias and line inversion (n = 1)

Assuming a pixel capacitance of 10 pF / mm^2 (see Section 4.3), the maximum area of the display element to be driven is about 2.835 mm^2.

AN11491

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Application note   **Rev. 1 — 9 January 2014**   **9 of 25**

For a segmented LCD, where there are different display elements with different sizes and thus different capacitances, the driving capability is better expressed as the maximum capacitance or maximum area of the display element that can be driven:

- Maximum pixel area: 2.835 mm^2.

This information is transferred into the maximum display area if a pure dot matrix display is considered, where all display elements have the same size:

- Maximum dot size: 1.684 mm x 1.684 mm

- Gap between dots: 0.05 mm

- Maximum X size: (1.684 + 0.05) x 102 = 177 mm

- Maximum Y size: (1.684 + 0.05) x 9 = 15.6 mm

- Maximum D size: ~178 mm = ~7 inches.

With all the above reasonable assumptions, the PCF8538U (or PCA8538U) can safely drive a 7" display (17.8 cm).

When the display driver is used at lower multiplex rates, the selection time is longer and therefore larger display elements can be driven. Also lowering the frame frequency from the 80 Hz value used in this example, will allow larger displays.

It is recommended to maximize the ITO track width in order to keep the resistance as low as possible. Furthermore it is recommended to balance the resistances:

- Layout the display such that the spread on the various R_{COM} is minimized (about equal values)

- Layout the display such that the values of the various R_{SEG} are about the same.

In dot matrix applications, contrast variations are more visible and therefore these recommendations should be followed especially in such applications.

5. Cascading more drivers

In large display configurations, up to four PCx8538 can be cascaded. In the context used here, cascading means combining more than one LCD driver in a design in such a way, that makes all drivers together appear to the rest of the application as one larger LCD driver, capable of driving a larger display than the individual LCD drivers would be able to. In order to appear as one LCD driver to the microcontroller, all drivers used in the cascade must use the same I^{2}C address. The individual drivers can be differentiated on the same I^{2}C bus by using a 2-bit hardware sub-address (A0 and A1). These hardware sub-addresses can be set by connecting the respective pins (A0 and A1) on the LCD driver to either V_{SS} or V_{DD}, in order to make them either LOW or HIGH.

Table 2. Addressing cascaded PCx8538

Pin A1	Pin A0	Device
0	0	0 (master)
0	1	1 (slave)
1	0	2 (slave)
1	1	3 (slave)

AN11491

Application note **Rev. 1 — 9 January 2014** **10 of 25**

5.1 Wiring common and segment outputs

When the cascaded PCx8538 are synchronized, they can share the common (backplane) signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the common outputs of only one device need to be through-plated to the common electrodes of the display. The other PCx8538 of the cascade contribute additional segment outputs. Their common outputs can either be connected together to enhance the drive capability or they can be left open-circuit. See Fig 6 where external V_{LCD} is used (common for both) and the internal clock. Alternatively, given that the common outputs of the drivers carry the same signals, some common outputs of the master can be taken and some of the slave in order to facilitate the layout of the display. High flexibility in creating the glass layout is further provided by the dual set of backplane outputs on the PCx8538.
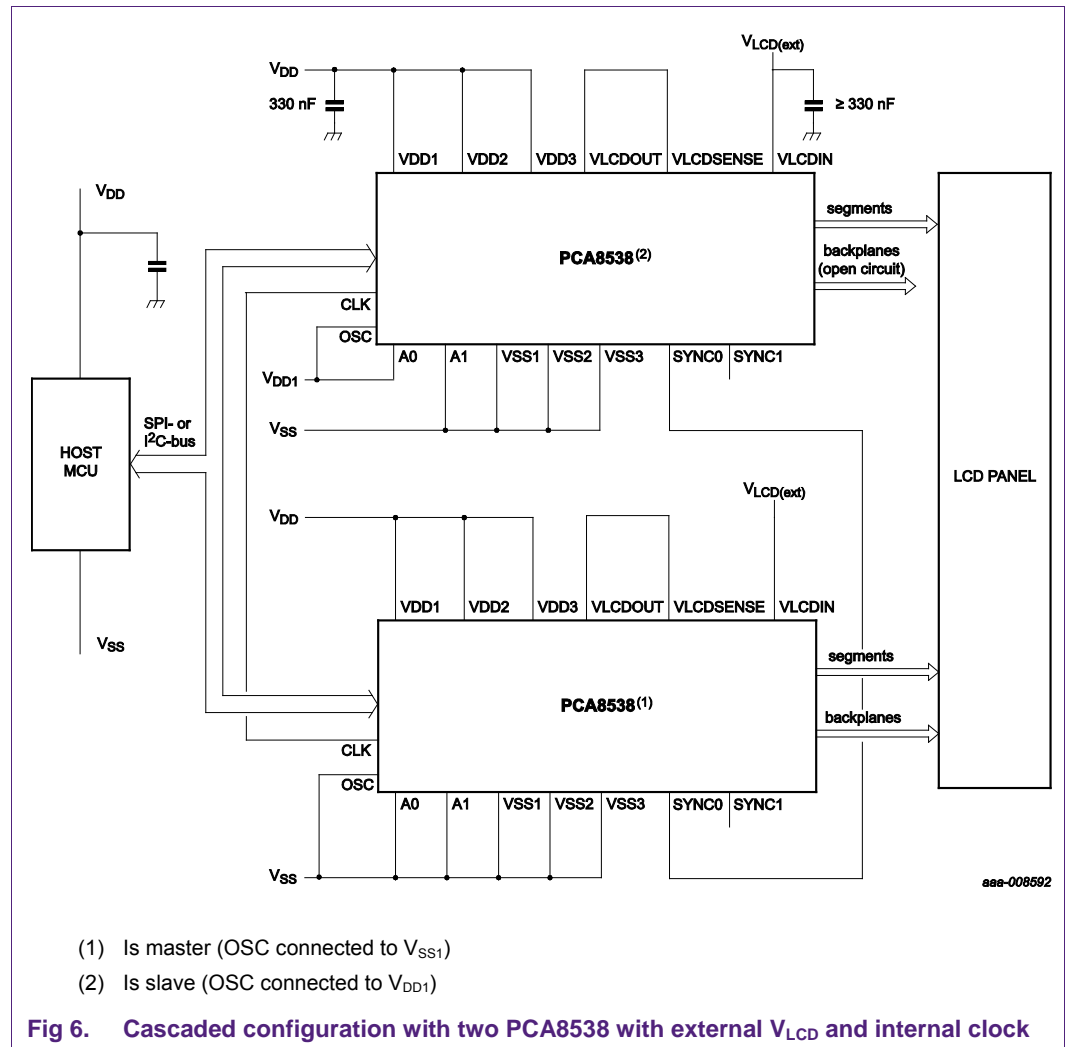

(1) Is master (OSC connected to V_{SS1})

(2) Is slave (OSC connected to V_{DD1})

Fig 6.   Cascaded configuration with two PCA8538 with external V_{LCD} and internal clock
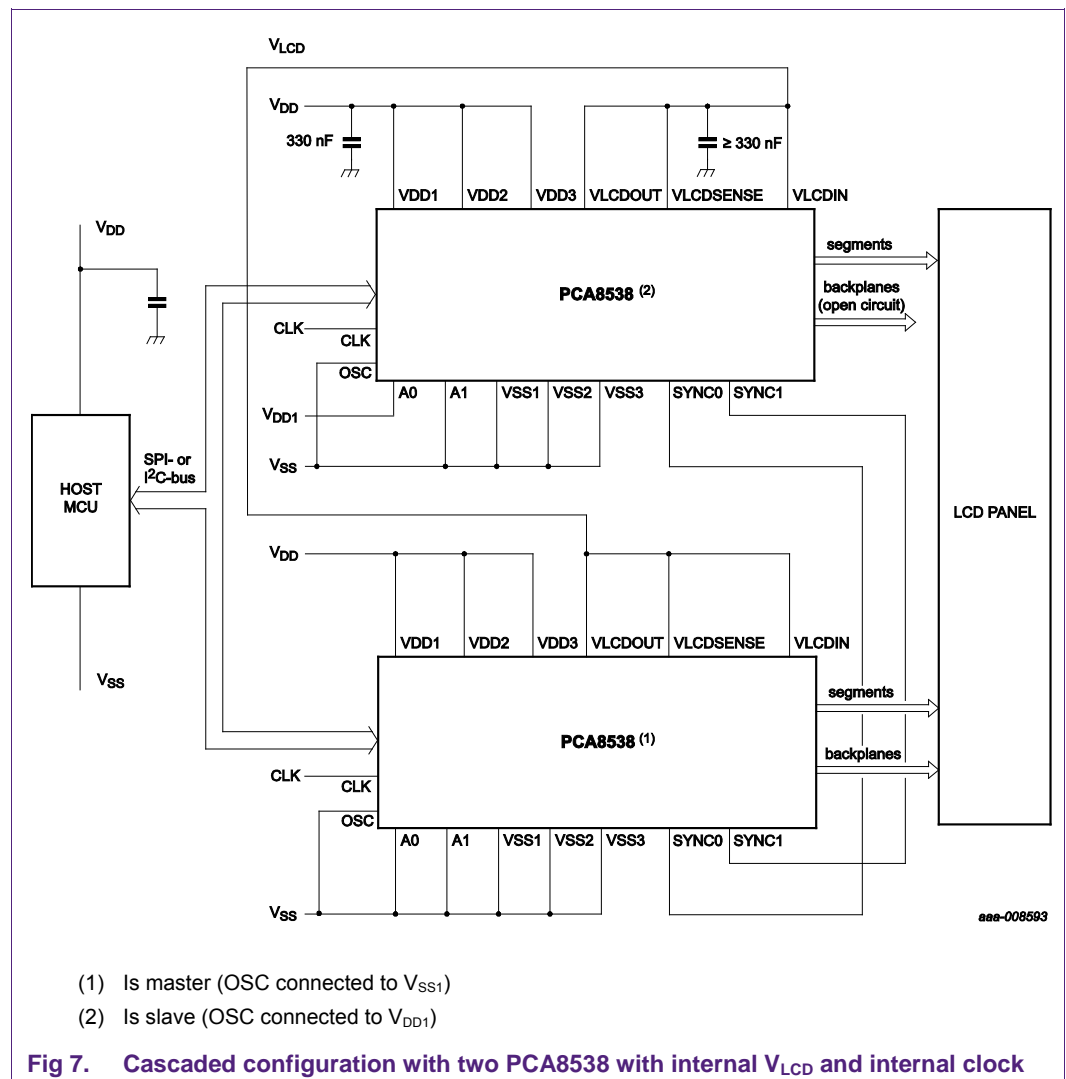
In this example (external V_{LCD}) the internal charge pump of all drivers in the cascade must be disabled. The synchronization signal SYNC1, which is provided to synchronize the charge pumps, must not be connected.

5.2 Cascading more drivers using the on-chip charge pump

Using the internal V_{LCD} charge pump is advantageous because it removes the need for an additional supply voltage, and it provides the option of temperature compensation of V_{LCD}. It will however increase the power consumption of the LCD driver.

Fig 7 shows a cascaded setup where the internal charge pump is used to generate V_{LCD}. In this setup, the internal charge pump of all drivers in the cascade must be enabled and V_{LCD} of all must be set to the same voltage. The pins V_{LCDOUT}, $V_{LCDSENSE}$ and V_{LCDIN} must be connected together, and also connected to the same pins of the other drivers. This results in the charge pumps working in parallel, thus increasing driving capability.

Synchronization signal SYNC1 is used to synchronize the charge pumps. It is organized as an input/output pin. The SYNC1 pins must be connected together if the on-chip V_{LCD} generation is used. In addition this pin must be enabled using the SYNC1_pin command.

(1) Is master (OSC connected to V_{SS1})

(2) Is slave (OSC connected to V_{DD1})

Fig 7.   Cascaded configuration with two PCA8538 with internal V_{LCD} and internal clock

AN11491

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Application note

Rev. 1 — 9 January 2014

12 of 25

5.3 Choice of oscillator and synchronization

PCx8538 offers the choice of using the internal oscillator or an external oscillator. When the internal oscillator is used, the frame frequency can be selected in the range from 45 Hz to 300 Hz, factory calibrated, with a tolerance of ± 5 Hz (at 80 Hz).

Both the internally generated clock signal or an externally supplied clock signal can be used in cascaded applications.

In cascaded applications that use the internal clock, the master PCx8538 with device address A[1:0] = 00 must have the OSC pin connected to V_{SS1} whilst the COE bit is set to logic 1, so that this device uses its internal oscillator to generate a clock signal at the CLK pin. The other PCx8538 devices are having the OSC pin connected to V_{DD1}, meaning that these devices are ready to receive an external clock signal which is provided by the master device with subaddress A[1:0] = 00.

If the master is providing the clock signal to the slave devices, care must be taken that the sending of the display enable or disable will be received by the master and slaves at the same time. When the display is disabled, the output from pin CLK is disabled too. Not providing a clock signal may result in a DC component for the display.

In cascaded applications that use an external clock, all devices have the OSC pin connected to V_{DD1} and thus an external CLK is being provided for the system. Here all devices are connected to the same external CLK.

Independent from whether an internal or external clock is used, the correct synchronization between all cascaded PCx8538 must be maintained. For this purpose the SYNC0 and SYNC1 lines are provided. The synchronization is guaranteed after the Power-On Reset (POR). SYNC0 is used to synchronize the output drive signals. SYNC1 is used to synchronize the charge pumps.

If a PCx8538 is configured as the master, its SYNC lines are configured as outputs. Only the master drives the SYNC0 and SYNC1 signals. In case the PCx8538 has been configured as a slave, the SYNC0 and SYNC1 pads are inputs.

For proper functionality of the synchronization it is important that the contact resistance between the SYNC pads of cascaded devices is within the given limits. This is especially true for the SYNC1 tracks, where the limit is lower than for the SYNC0 tracks. However, for practical purposes, the limits are considered to be equal, and thus determined by the limitation for the SYNC1 ITO track resistances. If the resistance is too high then the devices will not be able to synchronize properly. Table 3 shows the limiting values for the contact resistance.

Table 3. SYNC line contact resistance

Number of devices	Maximum contact resistance of SYNC track from master to any slave
1 to 4	10 kΩ

5.4 Display data

The storage of display data is determined by the contents of the device address register (see datasheet). Storage is allowed only when the content of the device address register matches with the hardware device address applied to the pins A0 and A1. If the content of the device address register and the hardware device address do not match, data storage is inhibited but the data pointer is incremented as if data storage had taken place. The hardware device address must not be changed while the device is being accessed on the interface.

6. Compensating V_{LCD} over temperature

Whether there is a need for temperature compensation for the LCD voltage depends on the display technology used and on the temperature range over which the display is used. Segment displays using TN technology are less sensitive to temperature changes than STN and VA displays. Therefore, with TN technology and if the temperature range is limited, it may be possible to manage with just a fixed voltage applied to V_{LCD}.

However, intrinsically the LC cell needs compensation. The values of the threshold and saturation voltage depend on the liquid crystal, the cell parameters and the temperature. The temperature coefficient is negative. The temperature characteristics of the liquid should be provided by the LCD manufacturer. In many cases, the temperature over which a display is used varies over a wide range. Furthermore, the VA technology with its improved black and contrast is more sensitive to temperature variations. It should be noted that for a correct functioning temperature compensation the driver 'needs to know' the temperature of the LC. This is not always simple and usually COG modules have better sensing conditions than modules with the driver on foil or displays with the driver on the board. PCx8538 is a COG driver and if the V_{LCD} voltage is generated internally, the integrated 8-bit temperature compensation can be used to always apply an optimal supply voltage to the display, irrespective of temperature. The temperature value can also be read by command, irrespective of whether temperature compensation is enabled or not.

In order to be able to implement an accurate temperature compensation of the V_{LCD} voltage, it is necessary to know the temperature characteristics of the liquid. The ambient temperature range is divided into six independently programmable regions, and therefore to each a different temperature coefficient can be applied.
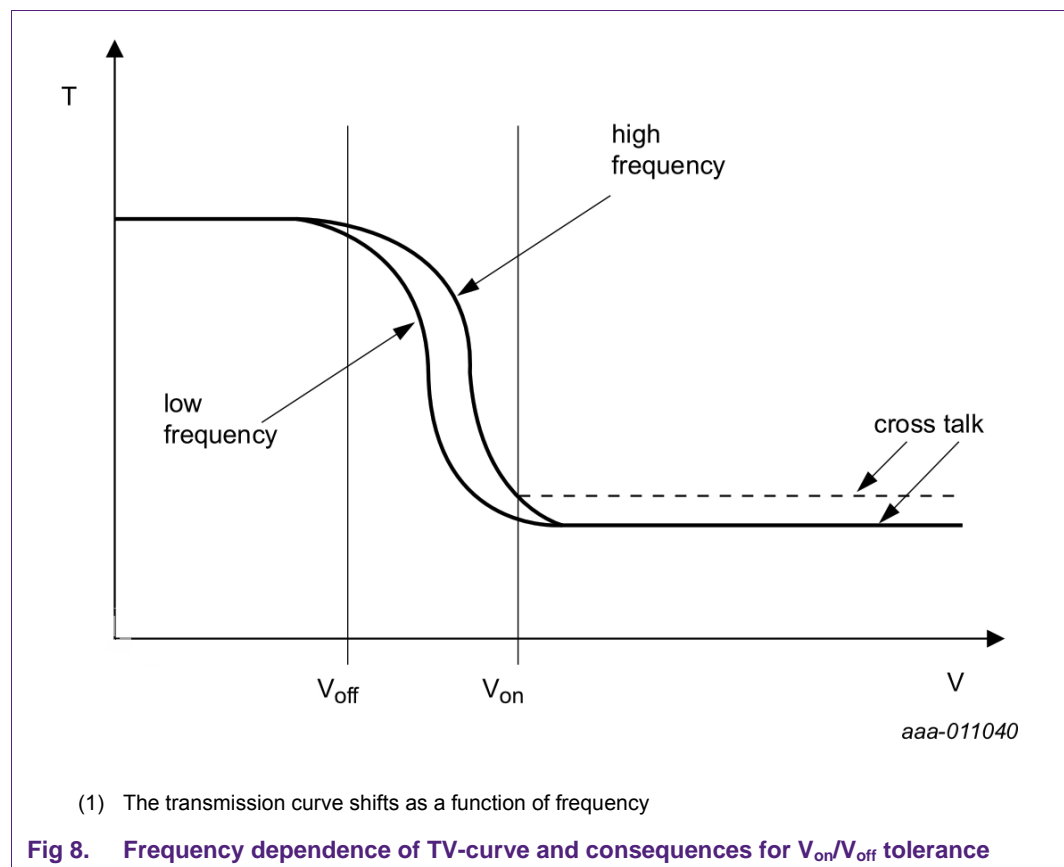
In the datasheet a detailed description of how to implement the temperature compensation is given.

AN11491

Application note **Rev. 1 — 9 January 2014** **14 of 25**

7. Compensating the frame frequency over temperature

Since PCx8538 provides an integrated temperature sensor and integrated charge pump for the generation of V_{LCD}, it is easy to implement the required temperature compensation of V_{LCD}. However, in some applications it may be preferred to not use the integrated charge pump, and to apply an external voltage V_{LCD} instead. For example, if lowest current consumption is a prime consideration for a certain application, not using the integrated charge pump will reduce the current consumption.

Implementing temperature compensation of an externally applied voltage V_{LCD} will add cost and complexity to the application. An alternative can then be changing the frame frequency as a function of temperature.

The frame frequency can be used for 'indirect' temperature compensation. At a lower temperature, the frame frequency can be lowered, because at lower temperatures the LC viscosity increases (the liquid becomes less fluid) and the LC's response time increases. The LC gets a more RMS-like behavior where flicker due to a low frame frequency is less easily seen. Because of the increase of the fluid's viscosity the TV-curve (TV-curve: Light Transmission as a function of Voltage) will shift less, and consequently there is more margin for shifts in V_{LCD} due to temperature changes.

(1) The transmission curve shifts as a function of frequency

Fig 8. **Frequency dependence of TV-curve and consequences for V_{on}/V_{off} tolerance**

Therefore it is possible to use the internal temperature sensor to read out the temperature, and depending on the temperature, set the frame frequency.

The TV curve of a typical LC depends on the frequency of the cell driving signal as shown in Fig 8.

8. Guidelines for the COG module design

In COG applications the resistance of ITO tracks must not be neglected. Special attention must be paid to the ITO layout in order to keep the side effects of track resistance to an acceptable level.

For COG applications the power supply circuits of NXP LCD driver ICs are separated internally into V_{DD1}, V_{DD2}, V_{DD3} and the corresponding V_{SS1}, V_{SS2} and V_{SS3}.

With PCx8538, V_{DD1} is the supply voltage 1, used for analog and digital. V_{DD2} is used to supply the charge pump and V_{DD3} is the supply voltage for analog. This allows the module maker to connect these supply circuits using separate ITO tracks. In this way the common (shared) part of the ITO track is minimized or eliminated. This reduces the amount of common-mode electrical noise.

For similar reasons, the LCD drive supply circuits are separated internally into V_{LCDIN}, V_{LCDOUT} and $V_{LCDSENSE}$. The shared part of the ITO supply track is thus kept to a minimum. Fig 9 represents this schematically.

(1) In this example, $V_{DD1} = V_{DD2} = V_{DD3}$

Fig 9. Typical configuration
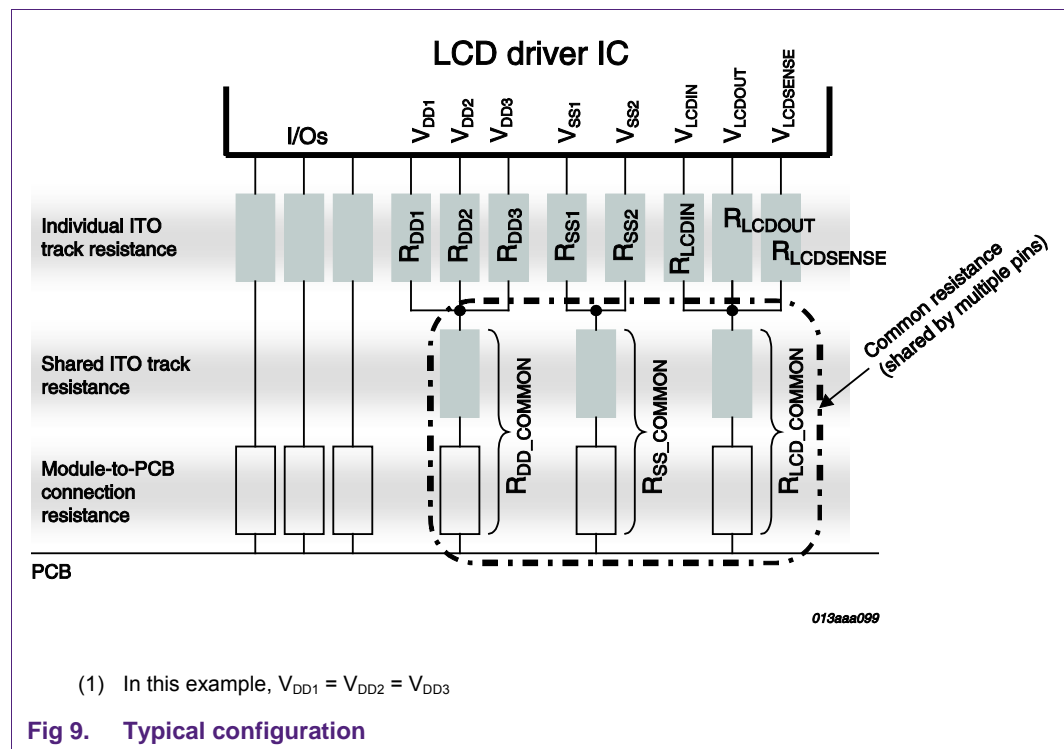
Excessive track resistance, especially common (shared) track and connection resistance can result in:

- a deterioration of the display quality

- increased power consumption

- incorrect operation

- higher sensitivity to EMI

8.1 ITO layout recommendations for ESD/EMC robustness in COG applications

The crucial factor for gaining an EMC and ESD robust application is the quality of the V_{SS1} line.

- To get an EMC/ESD robust ITO/glass layout, the $R_{ITO(VSS1)}$ has to be kept as low as possible;

- In the most common applications V_{SS1} will be connected to the pins T1, T2, A0, A1, OSC, SA0, SA1 and IFS (in the case of using the SPI interface) by using a very wide ITO connection;

- If possible, the ITO connection of V_{SS1} should be made wide, for example by fanning out the other connections;

- When the display is enabled, the charge and discharge caused by display activity affects the V_{SS1} line. This causes a dynamic current in the V_{SS1} line which means that dynamic voltage peaks in the V_{SS1} line may interfere with the low voltage part of the PCx8538. Therefore a low $R_{ITO(VSS1)}$ is also important for an improved noise immunity of the PCx8538, especially at high V_{LCD} values ($V_{LCD} > 10$ V);

- A low $R_{ITO(VSS1)}$ will also improve the communication stability with the microcontroller by reducing the effects of local ground (V_{SS1}) bounce caused by high SDAACK currents;

- It should be considered that V_{SS1} is internally connected to the IC substrate, therefore noise on the V_{SS1} line will cause noise inside the IC.

In order to keep the ITO track resistance to a minimum, pitch and position of the module connections must be selected such that the power tracks run as straight as possible to the glass edge. In order to minimize common connection resistance, use low-ohmic elastomeric connections, metal pin connections or ACF bonded foil cable.

Fig 10 and Fig 11 are showing the recommended ITO connections for a COG layout according to the interface type being used.

More detailed information about all aspects of COG layout design is given in reference [3], AN10170.
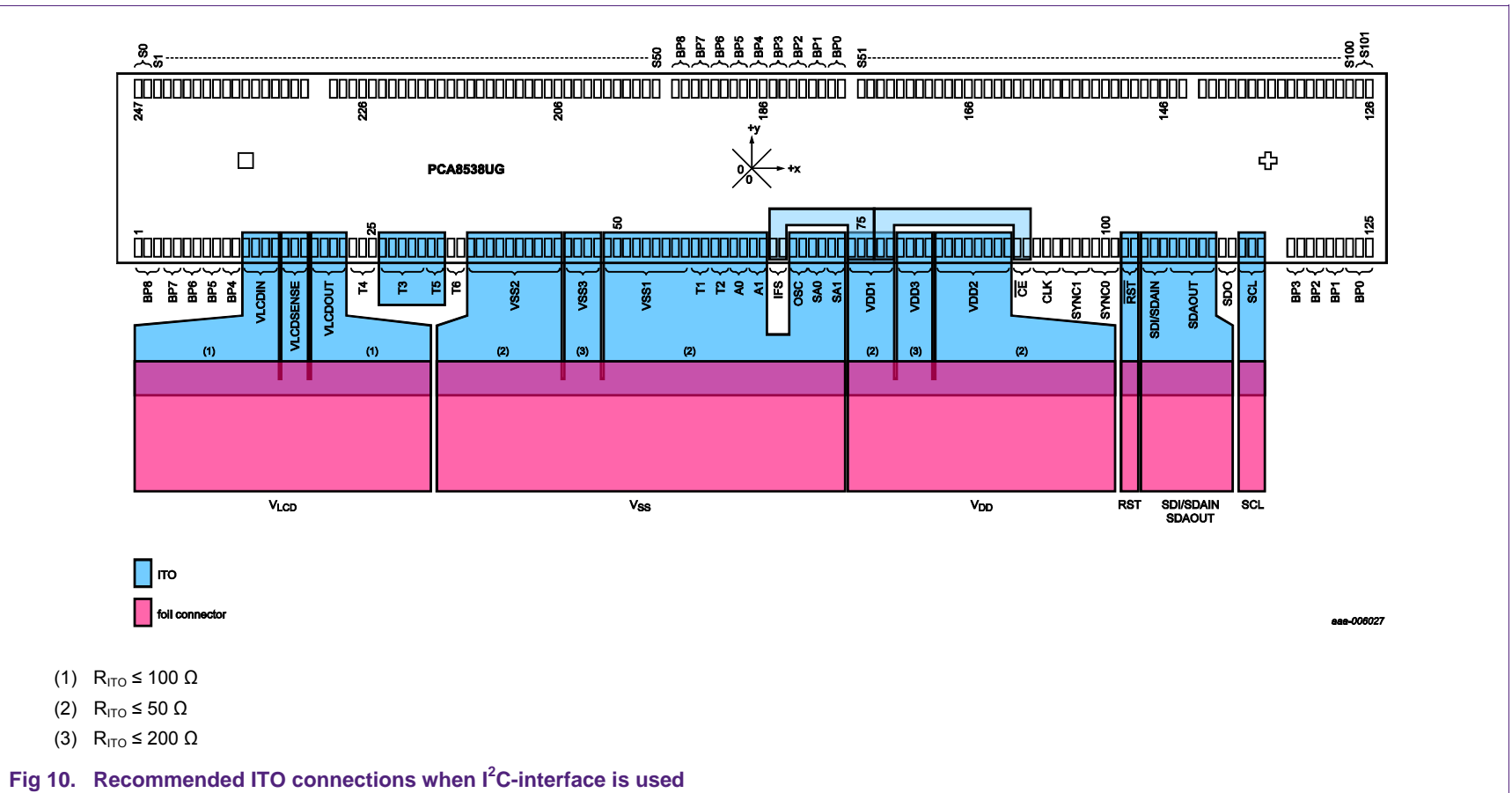
AN11491

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Application note **Rev. 1 — 9 January 2014** **17 of 25**

(1) $R_{ITO} \leq 100\ \Omega$

(2) $R_{ITO} \leq 50\ \Omega$

(3) $R_{ITO} \leq 200\ \Omega$

Fig 10. Recommended ITO connections when I²C-interface is used

(1) $R_{ITO} \le 100\ \Omega$

(2) $R_{ITO} \le 50\ \Omega$

(3) $R_{ITO} \le 200\ \Omega$

Fig 11. Recommended ITO connections when SPI-interface is used

9. Demo board

A demo board, type number OM13501, has been developed in order to provide a low cost tool to engineers, wishing to demonstrate and evaluate the PCx8538 LCD driver, and to get hands-on experience with writing code for it. Code written while using this board can serve as an example for the final application. This enables rapid prototyping. The board consists of a base board, with a plugged in LPCXpresso board which contains the microcontroller to control the display driver.

Features:

- Demonstrates PCA8538 LCD driver

- Features a vertical alignment (VA) COG display module with integrated backlight

- Includes a plugged in OM13035 LPCXpresso board with LPC1115 microcontroller

- 3 push buttons

- User modifiable firmware, In-System/In-Application Programming (ISP/IAP) via USB.

- Power supply can be either using two AA batteries, via USB or via an AC adapter/external power supply. This can also be used for external V_{LCD}.

- Jumpers allow quick selection between usage of I^2C or SPI interface

- Provisions to easily measure the current consumption to V_{DD} and V_{LCD} lines

- Provisions to easily inject an external oscillator signal

- Box contents:

  o OM13501 base board (marked on the board)

  o OM13035 LPCXpresso board

The LPCXpresso board contains a JTAG/SWD debugger called the "LPC-Link" and a target MCU, which in this case is the LPC1115. LPC-Link is equipped with a 10-pin JTAG header and it seamlessly connects to the target via USB. When the firmware needs to be updated, the LPCXpresso board will be connected using USB to the computer on which the IDE (Integrated Development Environment) is installed.

The 12NC of the OM13501 board is 9353 014 43598 and a picture is shown in Fig 12.

Fig 12.   Top view of OM13501 demo board

10. References

The documents listed below provide further useful information. They are available at NXP's website www.nxp.com.

[1]   **PCA8538 Product datasheet**

[2]   **PCF8538 Product datasheet**

[3]   **AN10170** – Design guidelines for COG modules with NXP monochrome LCD drivers

[4]   **AN11267** – EMC and system level ESD design guidelines for LCD drivers

[5]   **UM10718** – OM13501, PCA8538 demo board user manual

[6]   **R_10015** – Chip-On-Glass (COG) – a cost-effective and reliable technology for LCD displays, White paper

AN11491
Application note

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Rev. 1 — 9 January 2014

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21 of 25

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AN11491

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Application note

Rev. 1 — 9 January 2014

22 of 25

12. List of figures

13. List of tables

14. Contents