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Implementing sigma-delta ADC with LPC800 comparator

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Document information

Info	Content
Keywords	Sigma-delta ADC, sigma-delta modulation, analog comparator, Analog-to-Digital Conversion, LPC800, ARM Cortex-M0+
Abstract	This application note describes the basic implementation, along with program source code, and optimization recommendations to implement a sigma-delta ADC using the integrated analog comparator in the LPC81xM series microcontrollers. The implementation within this application note can be used to sample an input voltage that is higher than the microcontroller's supply voltage.

Revision history

Rev	Date	Description
1	20130221	Initial version.

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1. Introduction

For most modern digital applications, the sigma-delta (ΣΔ) Analog-to-Digital Converter (ADC) is the preferred ADC architecture, due to its dependency on digital processing rather than analog circuit design and component accuracy.

This application note summarizes the selection of ADC architecture that suits your application and the working principle of ΣΔ ADC along with its implementation and optimization using the LPC81xM series.

1.1 ADC architecture selection

There are plenty of ADC architectures that can be used to convert analog signals into digital encoding. Table 1 summarizes the advantages and disadvantages of several popular ADC architectures.

Table 1. ADC architecture comparison

	ΣΔ	Flash	Dual slope (Integrating)	Successive Approximation (SAR)
Conversion method	Oversampling analog signal, filtered in digital domain	Multiple analog comparators to compare the analog value	Integrate analog value, then use known voltage reference to measure the time needed to zero the integrator	Using DAC and binary tree algorithm to generate analog signal to compare with analog input
Resolution (n-bits)	High	Low	Average	Average
Sampling rate (samples / sec)	Slow	Fastest	Average	Fast
Recommended for	Slow changing signals, temperature / humidity sensors, audio signals	On / off signals, non-periodic signals, accuracy doesn't matter	DC signals, battery voltage, cap sense	Average resolution, average sampling rate applications, low power

The SAR ADC is the most common ADC since its performance is adequate for most applications. However, it needs special care for the DAC and analog accuracy. On the other hand, the ΣΔ ADC trades speed for resolution, and it doesn't need accuracy for its analog parts. This architecture can easily be built using discrete components.

1.2 ΣΔ ADC working principle

The ΣΔ ADC consists of three blocks: a ΣΔ modulator, a low pass digital filter and a decimator.

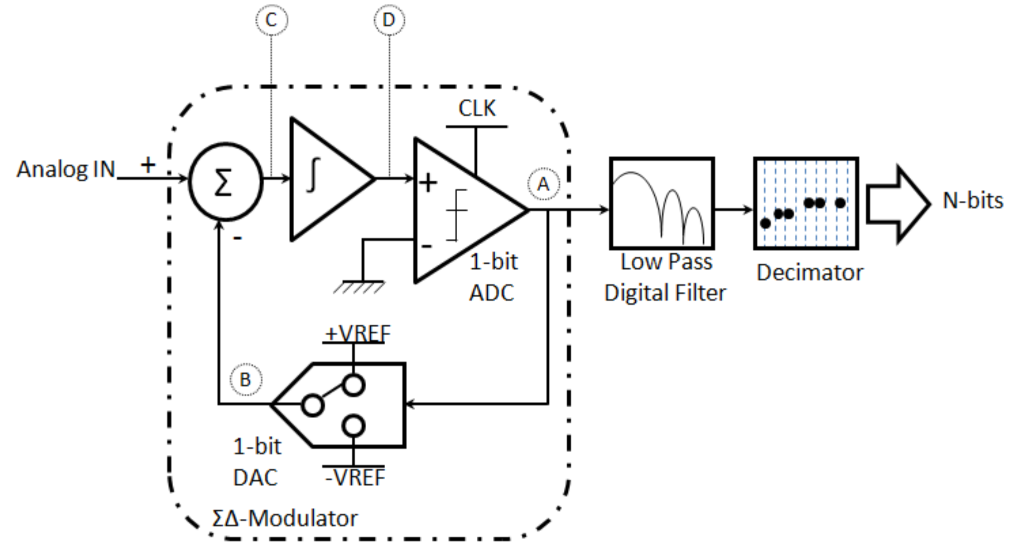


Fig 1. **ΣΔ ADC block diagram**

To see how the ΣΔ modulator works, let's assume that the analog input value is 1.1 V and the initial value of the integrator is 0 V. The 1-bit ADC will convert any voltage below 0 V to a '0' and voltages 0 V and above to a '1'. The 1-bit DAC will convert logic '0' to –3.3 V and '1' to 3.3 V. The ΣΔ modulator process can be seen in Table 2.

Table 2. **ΣΔ modulator process**

ΣΔ modulator process when Analog IN = 1.1 V, Vintegrator = 0

1-bit ADC output (Node A)	1-bit DAC output (Node B)	Summing output (Node C)	Integrator output (Node D)
'0'	–3.3 V	4.4 V	4.4 V
'1'	3.3 V	–2.2 V	2.2 V
'1'	3.3 V	– 2.2 V	0 V
'0'	–3.3 V	4.4 V	4.4 V
'1'	3.3 V	–2.2 V	2.2 V
'1'	3.3 V	–2.2 V	0 V
'0'	–3.3 V	4.4 V	4.4 V
'1'	3.3 V	–2.2 V	2.2 V

The integrator output (Node D) will generate a repeating pattern of 4.4 V, 2.2 V and 0 V. The 1-bit ADC output (Node A) will generate a repeating bitstream of '011'.

The quantization noise generated in the ΣΔ modulator is filtered out by the digital filter. The results are down-sampled by the decimator into n-bits of ADC results.

For the example above, assume that the ADC result is 3 bits in length and the digital filter is averaging the last eight 1-bit ADC bitstream results. After the 8th reading, the decimator will return the ADC result. The whole process can be seen at Fig 2.

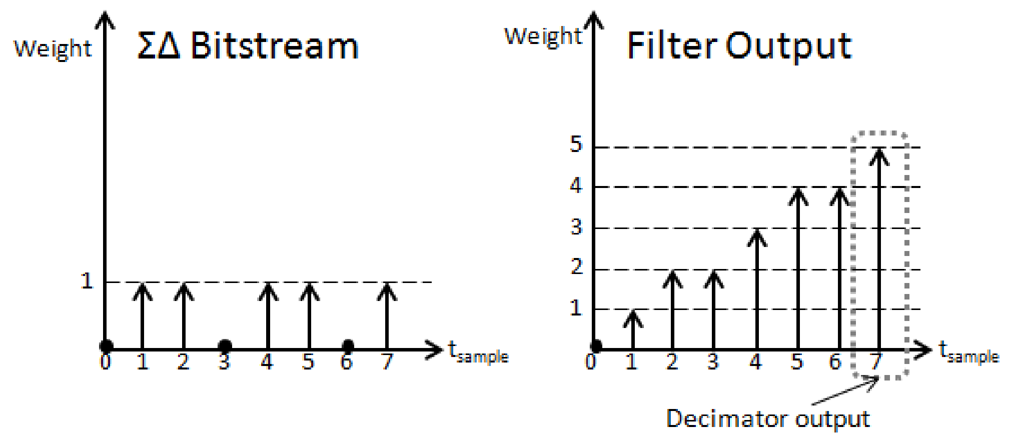


Fig 2. Digital Filter and Decimator Effect

Hence, the final ADC reading for the example above is 5 (0x05), which is equal to

$$\left(\frac{5}{8}x(VREFMAX-VREFMIN)+VREFMIN\right)=(0.675\cdot(3.3V-(-3.3V))+(-3.3V))=0.825\text{V}.$$

The error could be minimized by using higher number of bits per sample, or by employing better digital filtering. For example, if the averaging window is 1024 samples (10-bit output resolution), instead of 8 samples, the result will be

$$\left(\frac{682}{1024}x(VREFMAX-VREFMIN)+VREFMIN\right)=(0.666\cdot(3.3V-(-3.3V))+(-3.3V))=1.096\text{V}$$

2. ΣΔ ADC hardware implementation

The LPC81xM series have an integrated analog comparator and a multipurpose State Configurable Timer (SCT). By adding simple resistors and capacitor network, it can be configured as first order ΣΔ ADC (Refer to Fig 3).

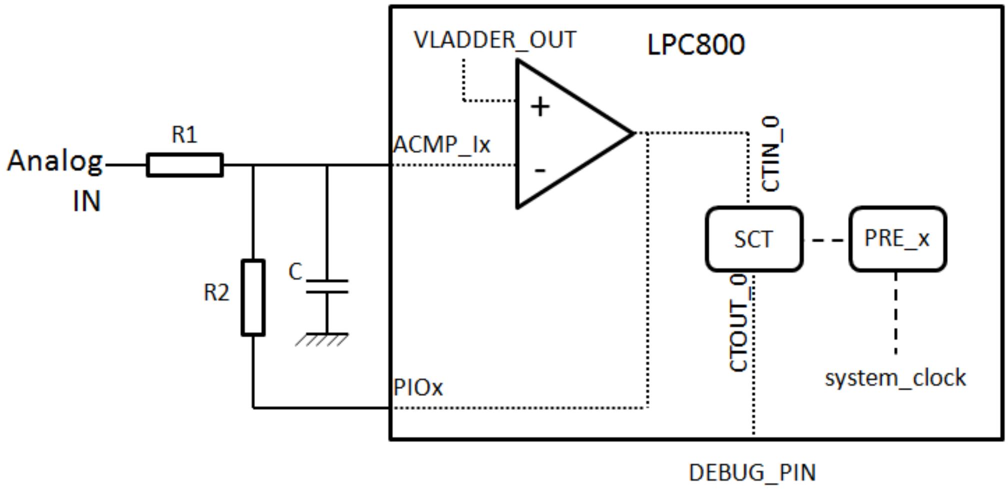


Fig 3. ΣΔ ADC implementation with LPC800

The resistors and the capacitor work as the continuous ΣΔ modulator. The R1 resistor is a simple voltage-to-current converter for the input voltage. The R2 resistor is a 1-bit DAC that converts the PIOx digital value to analog current. The current from both the input voltage and PIOx are then summed and integrated in the capacitor.

3. ΣΔ ADC software implementation

The advantage of a sigma delta ADC is that the output resolution is heavily influenced by the software, instead of the hardware. In this application note, the ΣΔ ADC that is implemented has a 10-bit resolution.

3.1 Analog comparator driver

The analog comparator driver is used to configure the analog comparator as shown in Fig 3. The analog comparator output functions as the feedback pin for the ΣΔ ADC. It needs to be connected to one of the output pins, and to the SCT's CTIN_0. This pin needs to be configured to disable its pull up / pull down resistor (or configured as open-drain if an external VREF is used. Refer to Section 5.2)

3.2 State Configurable Timer (SCT) driver

The SCT is used to sample, average and decimate the analog comparator output to generate the final ADC result.

3.2.1 Sampling the analog comparator output

The sampling process is done by connecting the analog comparator output to the SCT CTIN_0 pin in the switch matrix. The 'pinassign_acmp_o()' and 'pinassign_ctin_0()' function in the 'lpc8xx_sd_adc.c' implements this function.

The ADC sampling frequency is determined by the frequency of the SCT:

$$ADC\_Sampling\_Frequency = SCT\_Frequency = \frac{system\_clock}{PRE\_x} \tag{1}$$

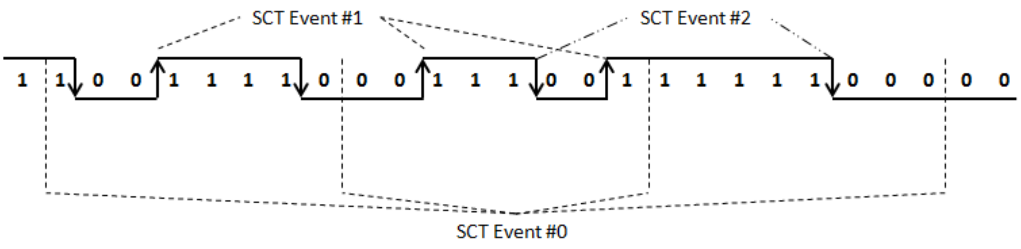
PRE_x is the SCT's prescaler register (Represented as CONFIG_SD_ADC_PRESCALER in the 'lpc8xx_sd_adc.h', in the code sample).

It is recommended to have ADC sampling frequency at least 1000 times higher than the input frequency, due to the low performance of the averaging filter. However, the sampling frequency should not go above analog comparator maximum propagation delay: 2 MHz.

3.2.2 Averaging and decimating the bitstream

Averaging is a simple low pass filter method that is easy to implement. It will also automatically decimate the bitstream, since each of averaging results will take few bit samples as input. In this implementation, the width of the averaging window determines the ADC output resolution.

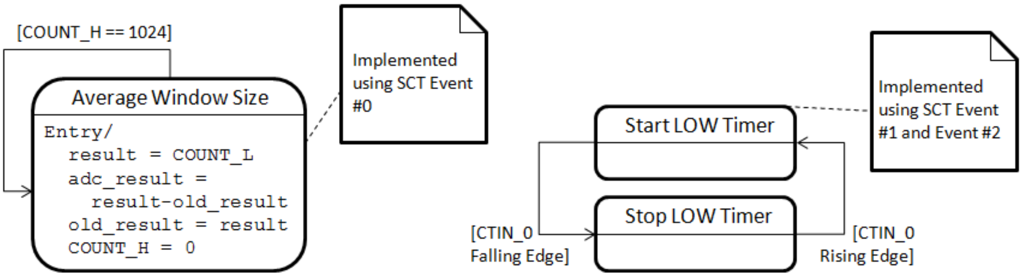
These functions are easily implemented using the SCT timer. The SCT can be used as separate dual 16-bit timers: LOW and HIGH timer. One of the timers, HIGH timer in the example, can be used to count the average window length, while the other, LOW timer in the example, is counting the number of '1's in the bitstream. The process can be seen in Fig 4.



(1) The code sample is using a window size of 1024 to generate a 10-bit ADC resolution. The SCT Event #0 will trigger every 1024 count.

Fig 4. Sigma delta average window

The diagram below shows the averaging window implementation using the SCT:

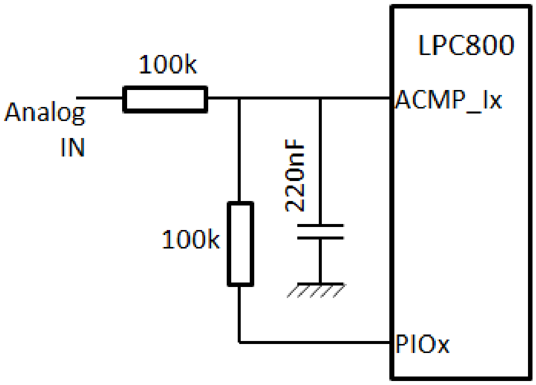


```
Entry/
  result = COUNT_L
  adc_result =
    result-old_result
  old_result = result
  COUNT_H = 0
```

Fig 5. Averaging window implementation

4. ΣΔ ADC result

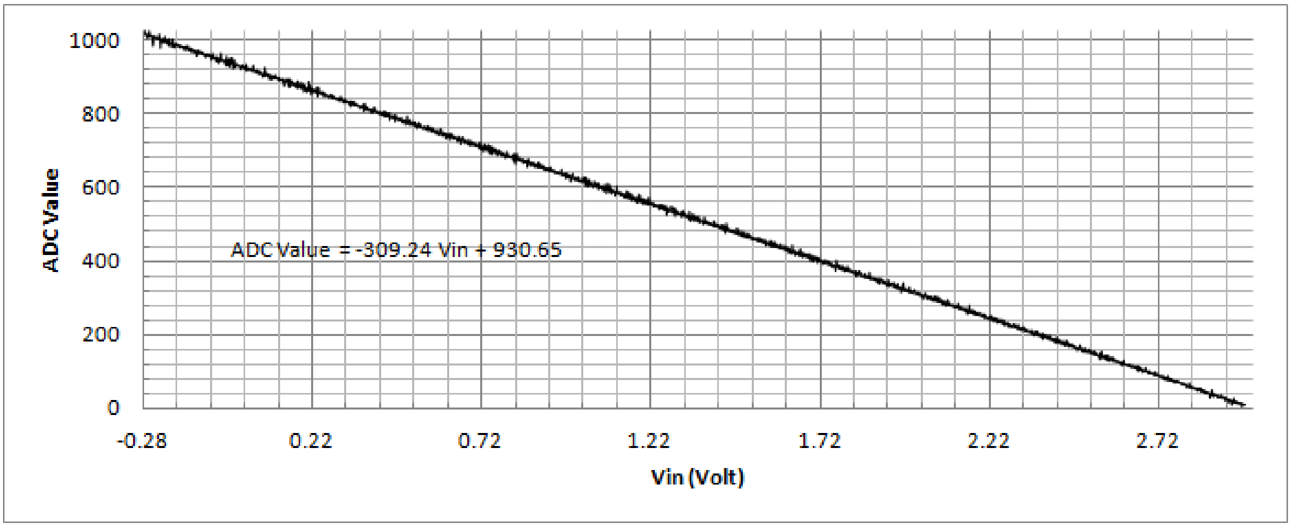
Some test results of ΣΔ ADC circuit implementation are as follows:



V_{LADDER_OUT} (Volt)	Analog In Minimum (Volt)	Analog In Maximum (Volt)
14 * 3.3V / 31	-0.275V	2.98 V
15 * 3.3V / 31	-0.065V	3.185V
16 * 3.3V / 31	0.16V	3.41V
17 * 3.3V / 31	0.365V	3.615V

Fig 6. ΣΔ ADC circuit result with 100 kOhm – 100 kOhm – 220 nF

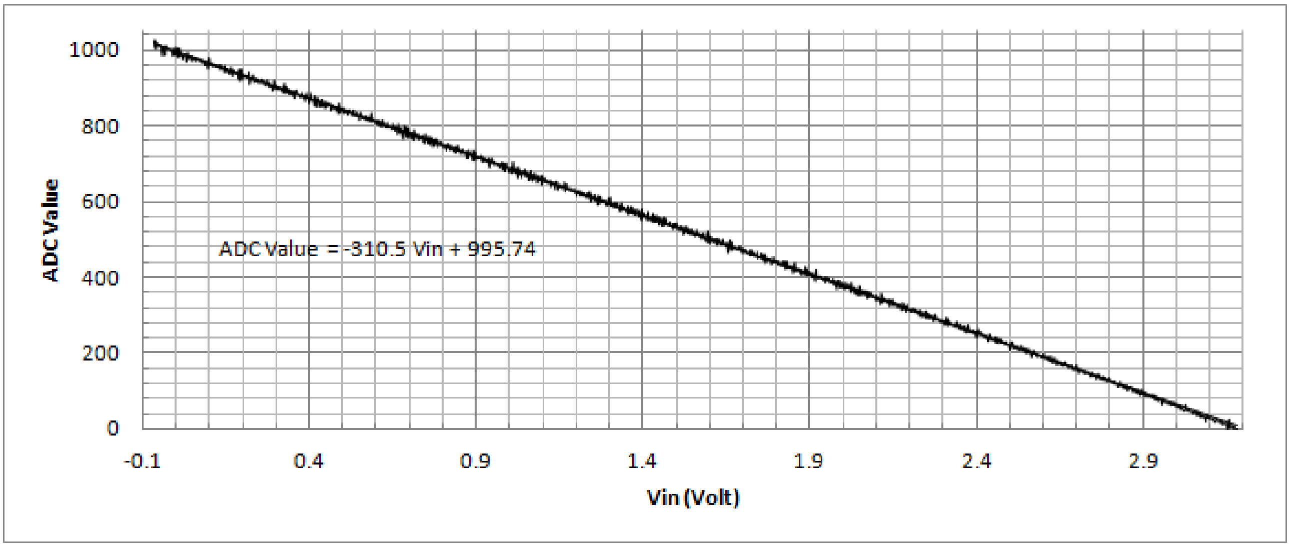
For VLADDER_OUT = (14 * 3.3 / 31), the ADC value error is about (0.39 / 1024 * 3.255V) = 1 mV above the real value.



(1) ADC value error average :0.39; ADC value error standard deviation: 7.45; F-sampling : 2 MHz; F-cutoff : 280 Hz; MCU freq : 24 MHz

Fig 7. ΣΔ ADC result for VLADDER_OUT = (14 * 3.3 / 31)

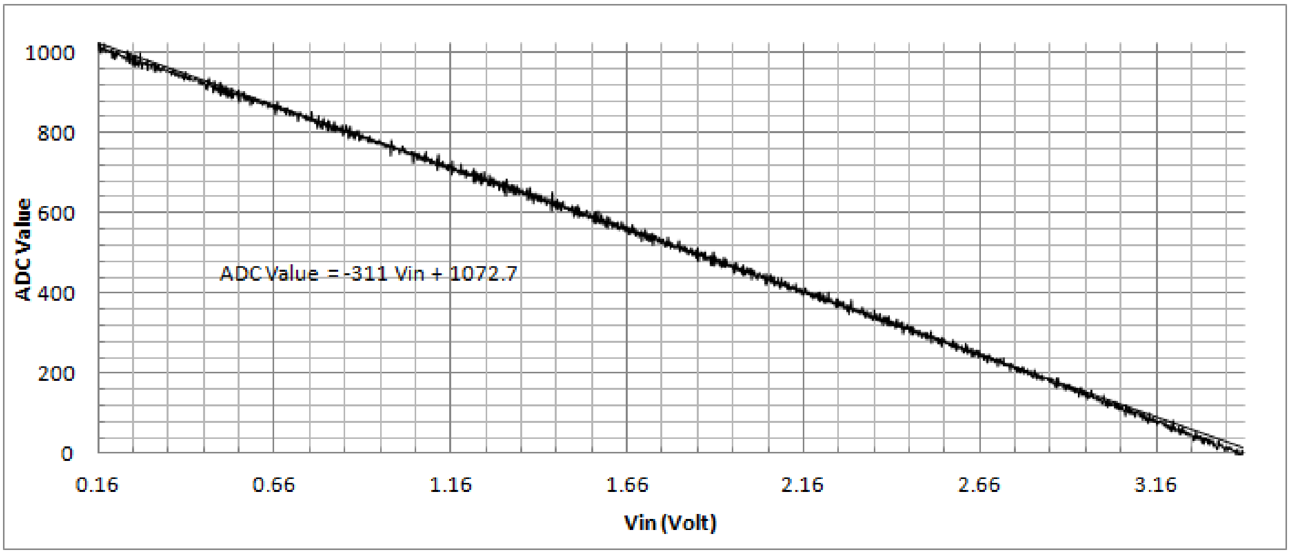
For VLADDER_OUT = (15 * 3.3 / 31), the ADC value error is about (0.65 / 1024 * 3.25 V) = 2 mV below the real value.



(1) ADC value error average : –0.65; ADC value error standard deviation: 7.70; F-sampling : 2 MHz; F-cutoff : 280 Hz; MCU freq : 24 MHz

Fig 8. ΣΔ ADC result for VLADDER_OUT = (15 * 3.3 / 31)

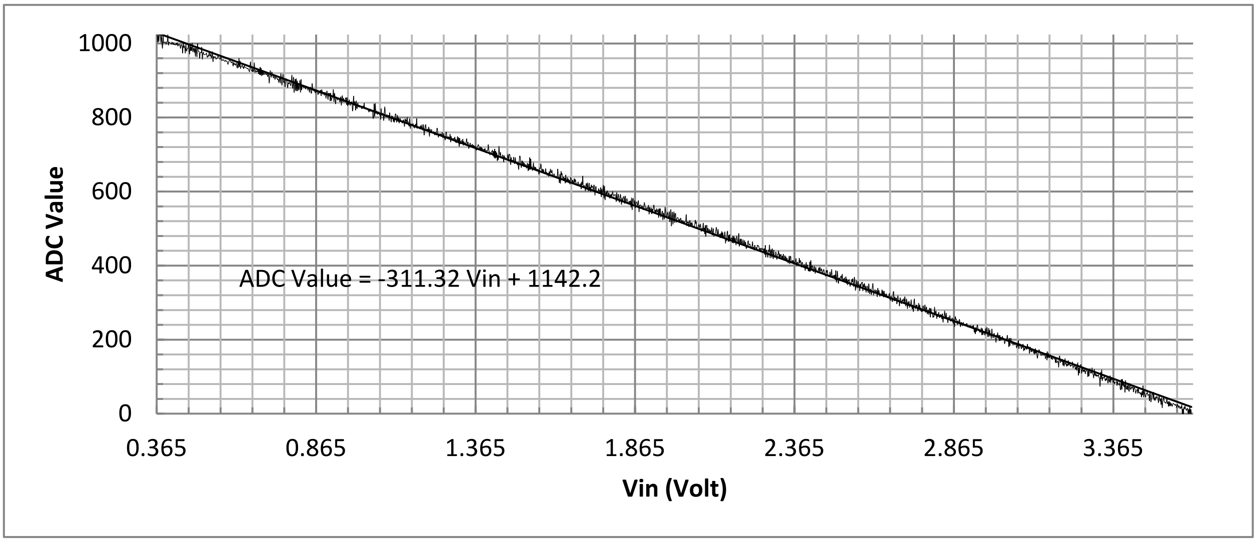
For VLADDER_OUT = (16 * 3.3 / 31), the ADC value error is about (5.57 / 1024 * 3.25 V) = 17 mV above the real value.



(1) ADC value error average : 5.57; ADC value error standard deviation: 9.29; F-sampling : 2 MHz; F-cutoff : 280 Hz; MCU freq : 24 MHz

Fig 9. Sigma delta ADC result for VLADDER_OUT = (16 * 3.3 / 31)

For VLADDER_OUT = (17 * 3.3 / 31), the ADC value error is about (10.66 / 1024 * 3.25 V) = 34 mV above the real value.



(1) ADC value error average :10.66; ADC value error standard deviation: 10.06; F-sampling : 2 MHz; F-cutoff : 280 Hz; MCU freq: 24 MHz

Fig 10. Sigma delta ADC result for VLADDER_OUT = (17 * 3.3 / 31)

5. ΣΔ ADC optimization

5.1 Configuring minimum / maximum input voltage

The ΣΔ ADC circuit above can be modified to suit a particular input voltage range. The minimum voltage of the Sigma delta ADC circuit is:

$$(R1 // R2) \cdot \left(\frac{V_{Analog\_IN(MIN)}}{R1} + \frac{VREF}{R2} \right) = V_{LADDER\_OUT} \tag{2}$$

By default, the VREF for the circuit in Fig 3 is 3.3 V. However, the microcontroller pin (the feedback pin) may not be able to supply the current needed, and will slightly limit the VREF to 3.25 V as is in the result at Section 0.

The maximum voltage of the Sigma delta ADC circuit is:

$$(R1 // R2) \cdot \left(\frac{V_{Analog\_IN(MAX)}}{R1} \right) = V_{LADDER\_OUT} \tag{3}$$

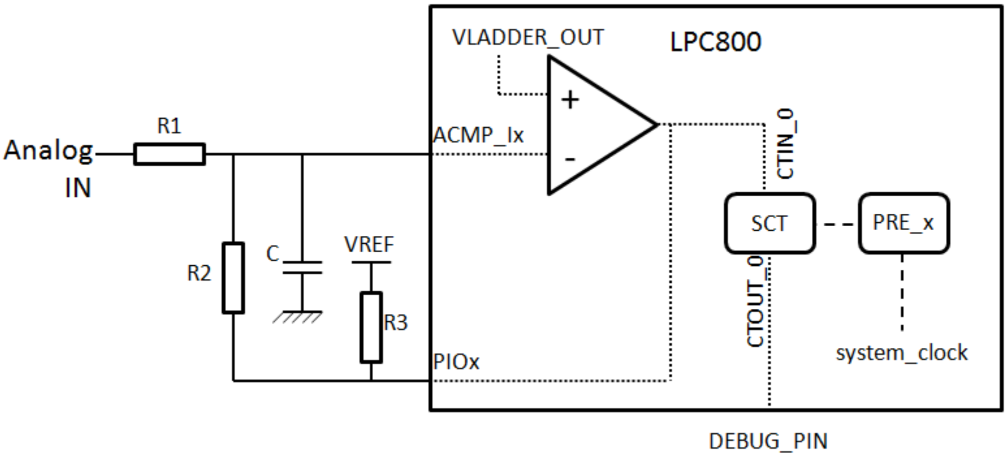
The equation is derived from the fact that when the input voltage reaches maximum, the feedback pin will constantly reach 0 V, while if the input voltage reach minimum, the feedback pin will constantly reach VREF.

5.2 Extending the input voltage range

Based on Section 5.1, the input voltage range can be defined as:

$$V_{Analog\_IN(MAX)} - V_{Analog\_IN(MIN)} = \frac{R1}{R2} \times VREF \qquad (4)$$

It is possible to extend the input voltage range value using the circuit below:



(1) The feedback pin (PIOx) needs to be configured as open drain

(2) If the VREF is above VDD, only true open-drain pins (PIO0_10 and PIO0_11 pins) that can be used

Fig 11. ΣΔ ADC implementation with external VREF

5.3 Avoiding slope overload distortion

The rate of voltage change in the input signal needs to be limited. If the input voltage is raising or falling too fast, the ADC will not be able to follow it, and will cause slope overload distortion.

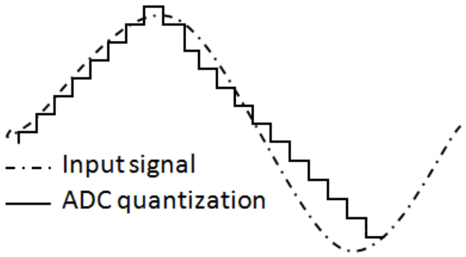


Fig 12. Slope overload distortion

By limiting the maximum rate of voltage change into the 1-bit ADC, the slope overload distortion can be avoided:

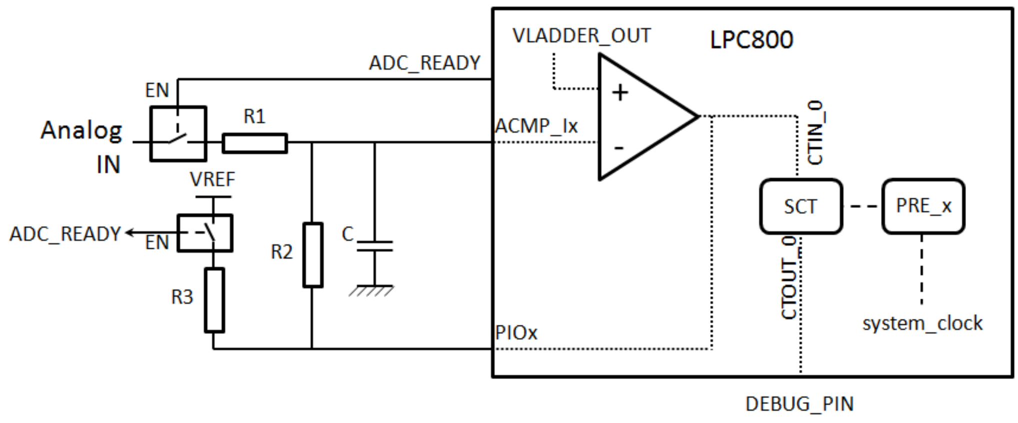
$$\frac{dV_{ACMP\_Ix}}{dt}\cdot\Delta t=\frac{1}{C}\left(\frac{V_{Analog\_IN(MAX)}}{R1}+\frac{V_{PIOx(MAX)}}{R2}-\frac{V_{LADDER\_OUT}}{(R1//R2)}\right)\cdot\Delta t\le V_{1-bit-ADC} \quad (5)$$

$V_{1\text{-bit-ADC}}$ refers to 1-bit ADC reference voltage (i.e. $\frac{V_{Analog\_IN(MAX)}-V_{Analog\_IN(MIN)}}{2^{N-bit}}$). The Δt refers to the ADC sampling period (Refer to Equation (1)). Hence, the capacitor value needs to be adjusted to suit Equation (5).

5.4 Measuring Input Voltage Higher than VDD (or Lower than VSS)

The advantage of the circuit in Fig 3 is that it can be used to measure input voltage that is higher or lower than the microcontroller's power supply, without adding an additional signal conditioner. However, care needs to be taken to ensure that these input voltages are not applied before the ΣΔ ADC pins are initialized. Otherwise, it may damage the microcontroller.

The circuit below illustrates the protection needed to guard the ADC input pin using an analog switch:



(1) The analog switch that is used must suit the ADC's minimum and maximum input voltage

Fig 13. ΣΔ ADC Implementation with Analog Switch

6. Conclusion

A simple RC network, along with an analog comparator and the SCT timer, can be used to form a 10-bit ΣΔ ADC in the LPC81xM.

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