AN11295

BGA3018 - 5 MHz to 300 MHz 18 dB reverse amplifier application

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Document information

Info	Content
Keywords	BGA3018, Evaluation board, CATV, Drop amplifier
Abstract	This application note describes the schematic and layout requirements for using the BGA3018 as a CATV reverse amplifier.

Revision history

Rev	Date	Description
1	20130214	First publication

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1. Introduction

The BGA3018 customer evaluation board enables the user to evaluate the performance of the wideband CATV MMIC amplifier BGA3018.

The BGA3018 performance information is available in the BGA3018 datasheet.

This application note describes the evaluation board schematic and layout requirements for using the BGA3018 as a CATV return path amplifier between 5 MHz and 300 MHz. The BGA3018 is fabricated in the BiCMOS process and packaged in a lead-free 3-pin SOT89 package. The BGA3018 is surface-mounted on an evaluation board with element matching and DC decoupling circuitry. The amplifier MMIC comprises a two stage amplifier with internal bias network and operates over a frequency range of 5 MHz to 1003 MHz with a supply voltage between 5 V and 8 V.

2. System features

- 18 dB gain
- Internally biased
- Flat gain between 5 MHz and 300 MHz
- Noise figure of 2.2 dB
- High linearity with an $IP3_o$ of 40 dBm and $IP2_o$ of 60 dBm
- 75 Ω input and output impedance
- Unconditionally stable
- Excellent input and output return loss

3. Customer evaluation kit contents

The evaluation kit contains the following items:

- ESD safe casing
- BGA3018 evaluation board
- BGA3018 SOT89 samples

4. Application Information

For evaluation purposes an evaluation board is available. The evaluation circuit can be seen in figure 1 and the corresponding PCB is shown in figure 2. Table 1 shows the bill of materials.

4.1 Evaluation board circuit

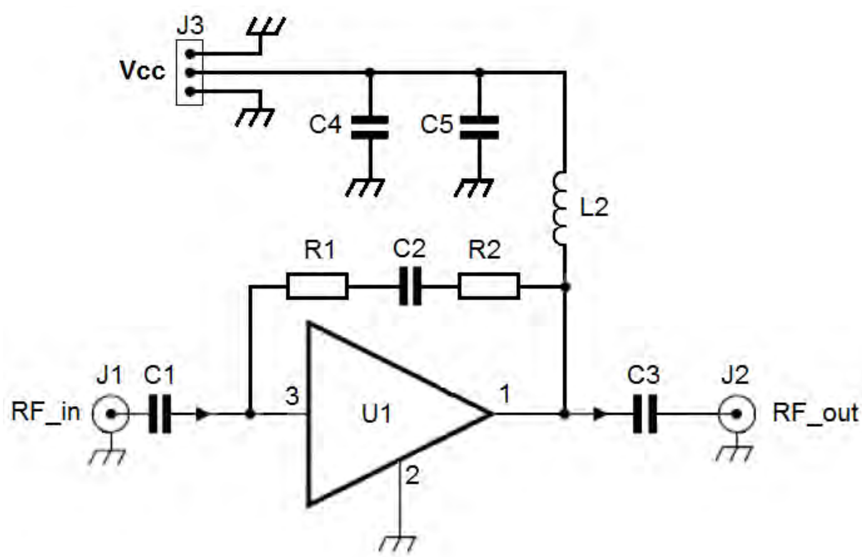
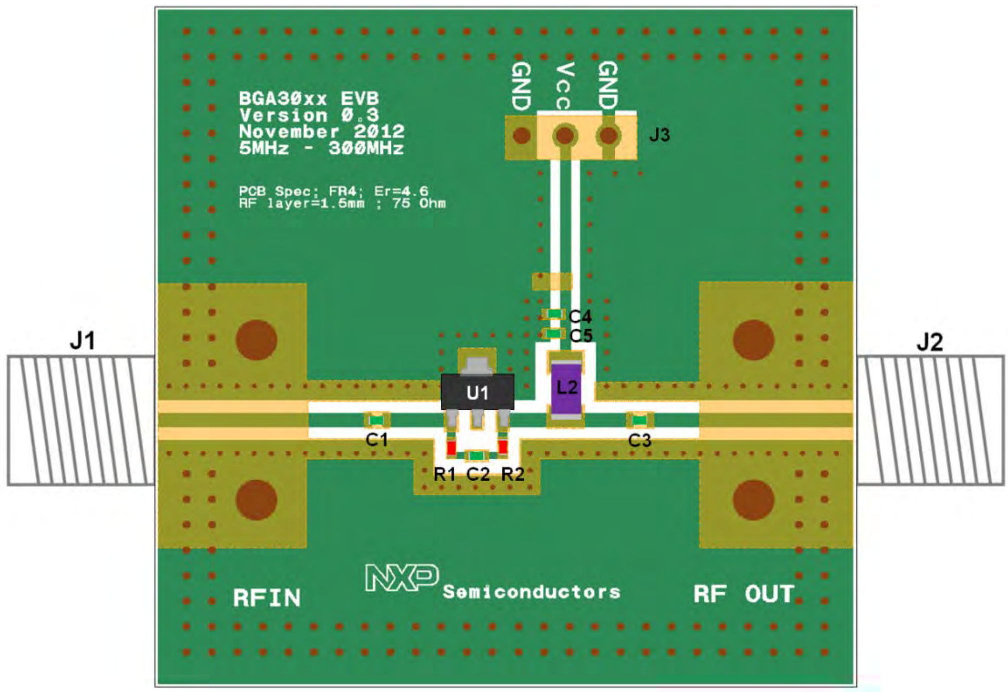


Fig 1. BGA3018 evaluation circuit

The power supply is applied on the center pin of connector J3 and is applied to the MMIC via choke L2 which provides RF blocking to the supply line. Capacitors C4 and C5 are supply decoupling capacitors.

At the F-connector J1 the RF input signal is applied where capacitor C1 provides DC-blocking. Resistors R1 and R2 are used as feedback resistors to set the gain and slope. Two resistors are used to lower the influence of the parasitic capacitance from the circuit board. Capacitor C2 provides DC-blocking between the input and output of the MMIC. Capacitor C3 provides DC-blocking before the RF signal is available at F-connector J2.

4.2 Evaluation board layout



PCB material	**= FR4**
PCB thickness	**= 1.5 mm**
PCB size	**= 40 mm x 40 mm**
ε_r	**= 4.6**
Copper thickness	**= 35 µm**

Fig 2. BGA3018 evaluation board layout

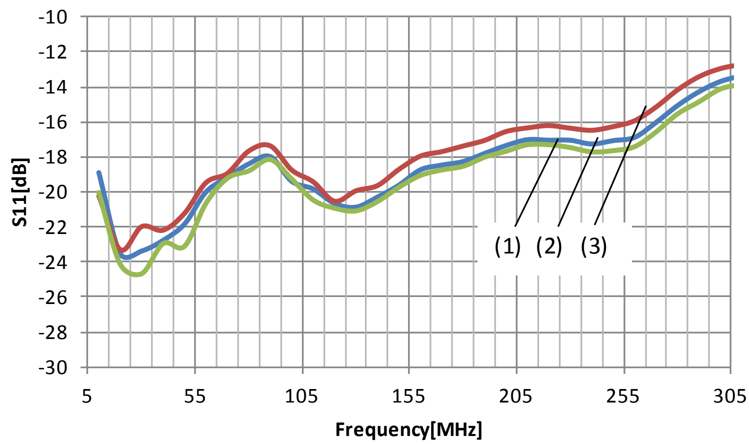
For optimum distortion performance it is important to have enough ground vias underneath and around the MMICs ground pins. This lowers the inductance to the ground plane. The evaluation board is made with two layer FR4 material.

4.3 Bill of materials

Table 1. Evaluation board BoM

Circuit Reference	Description	Qty	Mfr	Manufacturer number	Supplier	Supplier part number
U1	BGA3018	1	NXP	BGA3018	NXP	BGA3018
C1, C2, C3, C4	10 nF	4	Murata	GRM155R71E103KA01D	Digikey	490-1312-1-ND
C5	100 pF	1	Murata	GRM1555C1H101JZ01D	Digikey	490-3458-1-ND
L2	22uH	1	Murata	LQH31CN220K03L	Digikey	LQH31CN220K03L-ND
R1	470 Ω	1	Yageo	RC0402FR-07470RL	Digikey	311-470LRCT-ND
R2	300 Ω	1	Yageo	RC0402FR-07300RL	Digikey	311-300LRCT-ND
J1, J2	75 Ω F-connector	2	Bomar	861V509ER6	Mouser	678-861V509ER6
J3	Header 3	1	Molex	90121-0763	Digikey	WM8109-ND

5. Measurement results at Vcc = 8 V

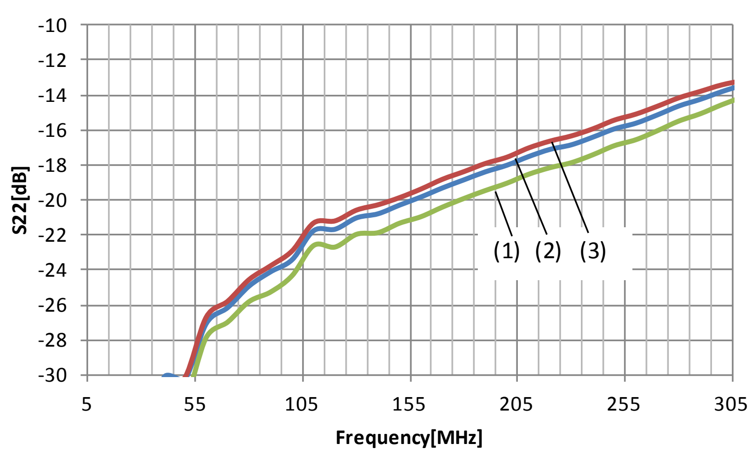


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 3. Input matching (S11); Vcc = 8 V

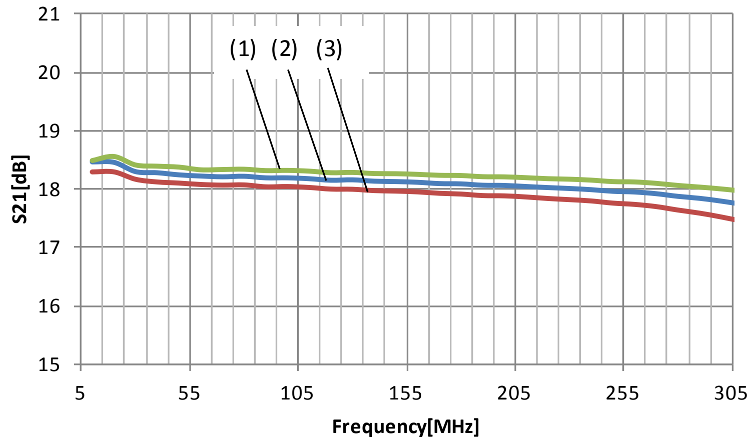


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 4. Output matching (S22): Vcc = 8 V

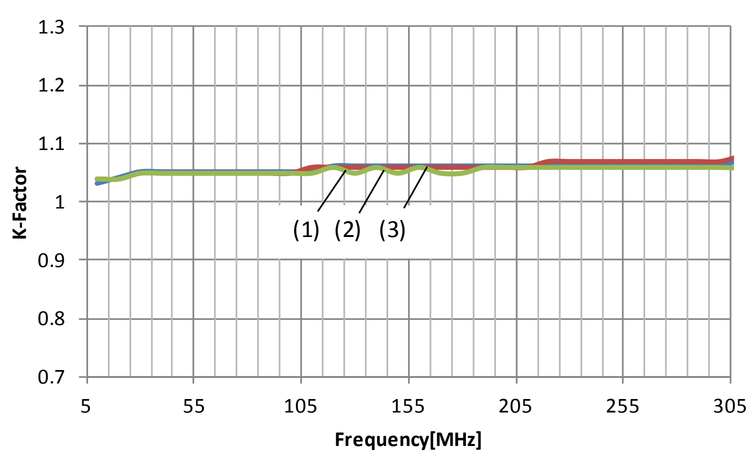


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 5. Gain (S21); Vcc = 8 V

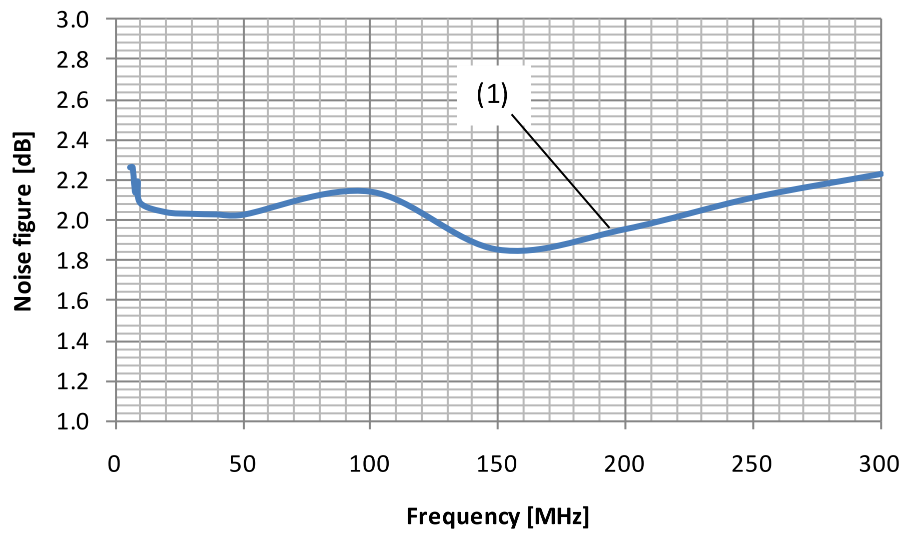


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 6. K-factor; Vcc = 8 V



(1) Tamb = +25 °C

Fig 7. Noise figure; Vcc = 8 V

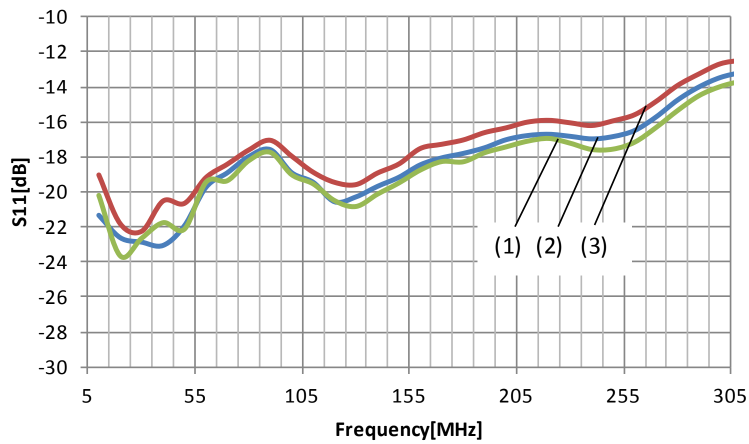
Table 2. Measurement results at Vcc = 8 V

Symbol	Conditions		-40 °C	+25 °C	+85 °C	Unit
NF	At 10 MHz		1.8	2.1	2.1	dB
	At 300 MHz		1.9	2.2	2.3	dB
$P_{L(1dB)}$	At 40 MHz		24.5	24.5	24.5	dBm
$IP3_O$	At 34 MHz	[1]	46.5	45.0	44.0	dBc
	At 74 MHz	[1]	46.5	45.5	44.0	dBc
	At 114 MHz	[1]	47.0	45.5	44.0	dBc
	At 154 MHz	[1]	47.0	44.5	43.0	dBc
	At 194 MHz	[1]	45.5	43.5	41.5	dBc
	At 234 MHz	[1]	44.5	42.5	40.5	dBc
	At 274 MHz	[1]	44.0	42.0	40.0	dBc
$IP2_O$	At 86 MHz	[2]	63.0	61.0	60.0	dBc
	At 166 MHz	[2]	63.0	61.0	59.0	dBc
	At 246 MHz	[2]	63.0	61.0	59.0	dBc

[1] The fundamental frequencies (f_1) and (f_2) lay between 40 MHz and 300 MHz. The intermodulation product (IM3) is 2 x $f_2 – f_1$, where $f_2 = f_1 \pm 6$ MHz. Input power P_i = -20 dBm.

[2] The fundamental frequencies (f_1) and (f_2) lay between 40 MHz and 300 MHz. The intermodulation product (IM20 is $|f_2 – f_1|$, with 40 MHz < $|f_1 – f_2|$ < 300 MHz. Input power P_i = -20 dBm.

6. Measurement results at Vcc = 5V

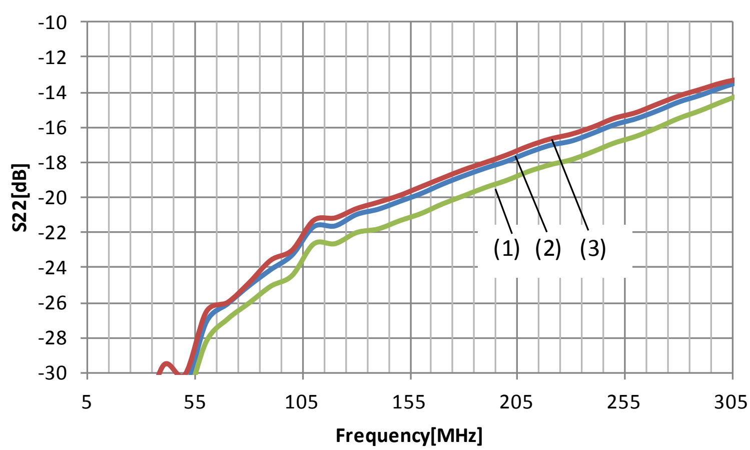


(1) Tamb = -40 °C

(2) Tamb = +25 °C

(3) Tamb = +85 °C

Fig 8. Input matching (S11); Vcc = 5 V

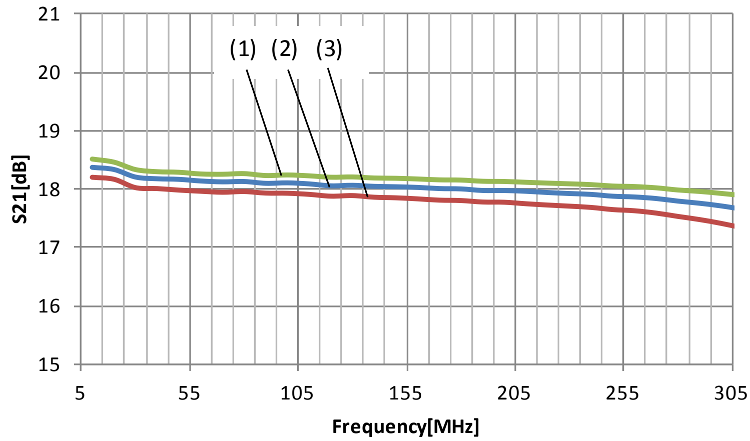


(1) Tamb = -40 °C

(2) Tamb = +25 °C

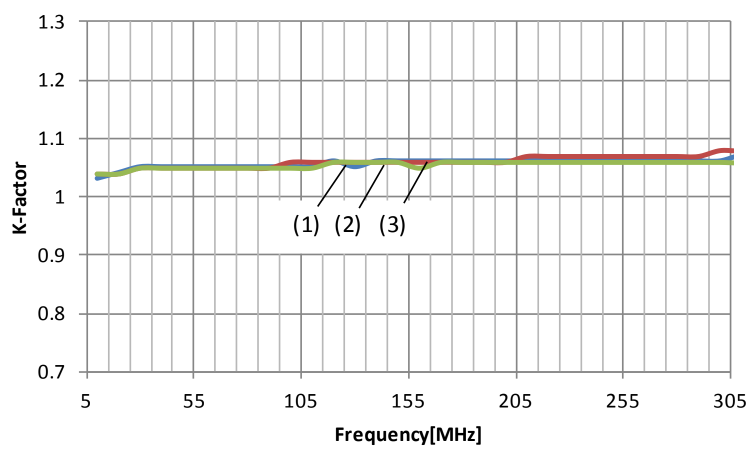
(3) Tamb = +85 °C

Fig 9. Output matching (S22): Vcc = 5 V



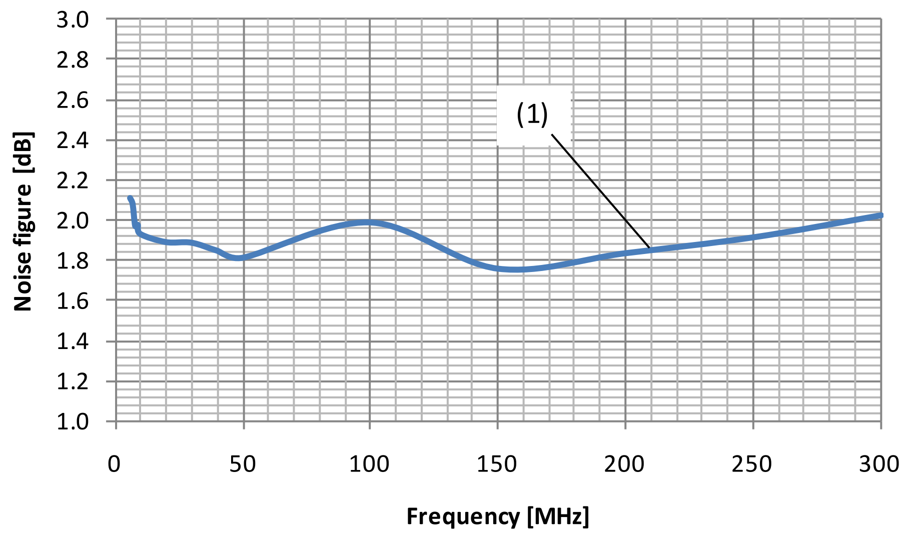
(1) Tamb = -40 °C
(2) Tamb = +25 °C
(3) Tamb = +85 °C

Fig 10. Gain (S21); Vcc = 5 V



(1) Tamb = -40 °C
(2) Tamb = +25 °C
(3) Tamb = +85 °C

Fig 11. K-factor; Vcc = 5 V



(1) Tamb = +25 °C

Fig 12. Noise figure; Vcc = 5 V

Table 3. Measurement results at Vcc = 5 V

Symbol	Conditions		-40 °C	+25 °C	+85 °C	Unit
NF	At 10 MHz		1.8	1.9	1.9	dB
	At 300 MHz		2.0	2.0	2.1	dB
$P_{L(1dB)}$	At 40 MHz		19.5	19.0	19.5	dBm
$IP3_O$	At 34 MHz	[1]	41.0	40.0	39.0	dBc
	At 74 MHz	[1]	41.0	40.5	39.0	dBc
	At 114 MHz	[1]	41.5	40.0	38.5	dBc
	At 154 MHz	[1]	41.0	39.5	38.0	dBc
	At 194 MHz	[1]	40.5	38.5	37.0	dBc
	At 234 MHz	[1]	39.5	38.0	36.5	dBc
	At 274 MHz	[1]	39.0	37.5	36.0	dBc
$IP2_O$	At 86 MHz	[2]	57.5	55.0	53.5	dBc
	At 166 MHz	[2]	57.0	54.5	53.0	dBc
	At 246 MHz	[2]	57.0	54.5	53.0	dBc

[1] The fundamental frequencies (f_1) and (f_2) lay between 40 MHz and 300 MHz. The intermodulation product (IM3) is 2 x $f_2 – f_1$, where $f_2 = f_1 \pm 6$ MHz. Input power P_i = -20 dBm.

[2] The fundamental frequencies (f_1) and (f_2) lay between 40 MHz and 300 MHz. The intermodulation product (IM20 is $|f_2 – f_1|$, with 40 MHz < $|f_1 – f_2|$ < 300 MHz. Input power P_i = -20 dBm.

[3] Measured with 10 NTSC channels Vo = 30 dBmV.

7. Abbreviations

Table 2. Abbreviations

Acronym	Description
AC	Alternating Current
CATV	Community Antenna TeleVision
DC	Direct Current
ESD	Electro Static Discharge
MMIC	Monolithic Microwave Integrated Circuit
NTSC	National Television Standards Committee
PCB	Printed Circuit Board
RF	Radio Frequency
SMD	Surface Mounted Device

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