AN11190

Application Note for the BGA7130 EVB 865 - 880 MHz

Rev. 1.0 — 2 July 2012 Application note

Document information

Info	Content
Keywords	Medium Power, 30 dBm, 865 - 880 MHz
Abstract	This Application Note describes the layout, schematics, characteristics and measurement methods of the BGA7130 tested in the 865 - 880 MHz range.

Revision history

Rev	Date	Description
1.0	20120702	Initial document

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1. Introduction

The BGA7130 is a wideband Silicon-Germanium MMIC (Monolithic Microwave Integrated Circuit) processed in NXPs mainstream Si QuBIC4+ BiCmos process. This process intrinsic inhibits high F_T figures (up to 28 GHz), while not compromising ruggedness (breakdown voltage) and noise figures. These characteristics make this device suitable for versatile RF e.g. final amplifier stages in E-Metering, MoCa (Multimedia on Coax), SMATV and ISM applications. The BGA7130 exhibits an integrated active bias circuit, to ensure almost flat performance over a temperature range from –40°C to + 85°C. No additional bias circuitry is required to bias the device; the internal bias circuit ensures stable quiescent currents (450 mA) over temperature.

The BGA7130 is packaged in the SOT908-1, and in combination with the optimized die design, gives excellent thermal performance, which leads to lifetimes of the product that fulfills the demanding applications

To ensure optimal ESD protections, all pins are ESD protected.

All above mentioned highlight makes the BGA7130 an extremely attractive device with optimal performance/cost ratio, as compared to other devices in the market.

2. Product Profile

2.1 General description

The BGA7130 MMIC is a one-stage amplifier, offered in a low-cost leadless surface-mount package. It delivers 30 dBm output power at 5 V with high linearity. Its power saving features include simple quiescent current adjustment, which allows class-AB operation and logic-level shutdown control to reduce the supply current to 4 uA.

2.2 Features

- 400 MHz to 2700 MHz frequency operating range
- Integrated active biasing
- External matching allows broad application optimization of the electrical performance
- 3 V to 5 V single supply operation
- ESD protection at all pins
- Excellent ruggedness performance:
  - withstands open / short output mismatch conditions
  - withstands voltage peaks of 8.5 V supply voltage

2.3 Applications

- Broadband CPE / MoCA
- WLAN / ISM / RFID
- Industrial applications
- Wireless infrastructure (base station, repeater, backhaul systems)
- Satellite Master Antenna TV (SMATV)

2.4 Application information

Table 1. Quick reference data

4.75 V ≤ V_{SUP} ≤ 5.25 V; -40 °C ≤ T_{case} ≤ +85 °C; p_i < -20 dBm; R3 = 523 Ω (tolerance 1 %); input and output impedances matched to 50 Ω ; pin ENABLE = HIGH; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{SUP}	supply voltage		[1]	4.75	-	5.25	V
$I_{CC(tot)}$	total supply current		[2]	390	450	510	mA
		500 Ω ≤ R3 ≤ 4.7 kΩ	[2]	50	-	550	mA
		500 Ω ≤ R3 ≤ 4.7 kΩ; pin ENABLE = LOW	[2]	-	4	6	µA
T_{case}	case temperature		[3]	−40	+25	+85	°C
f	frequency			400	-	2700	MHz
Measured at LTE-750 MHz							
f	frequency		[4]	728	748	768	MHz
G_p	power gain	728 MHz ≤ f ≤ 768 MHz		17	20	23	dB
$P_{L(1dB)}$	output power at 1 dB gain compression	728 MHz ≤ f ≤ 768 MHz		27	30.5	-	dBm
$IP3_O$	output third-order intercept point	728 MHz ≤ f ≤ 768 MHz; P_L = 19 dBm per tone; tone spacing = 1 MHz		39	42.5	-	dBm
Measured at UMTS-2140 MHz							
f	frequency		[5]	2110	2140	2170	MHz
G_p	power gain	2110 MHz ≤ f ≤ 2170 MHz		9	12	15	dB
$P_{L(1dB)}$	output power at 1 dB gain compression	2110 MHz ≤ f ≤ 2170 MHz		27	30	-	dBm
$IP3_O$	output third-order intercept point	2110 MHz ≤ f ≤ 2170 MHz; P_L = 19 dBm per tone; tone spacing = 1 MHz		40.5	44	-	dBm

[1] Supply voltage on pins RF_OUT and V_{CC}.

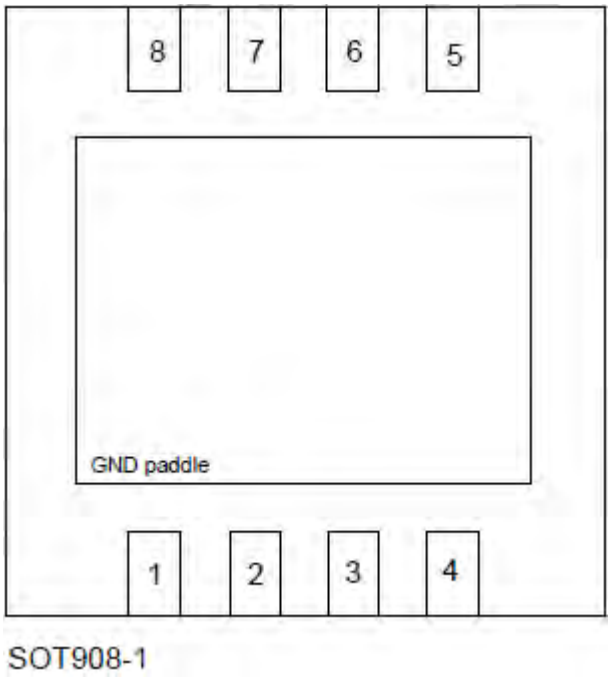
[2] Current through pins RF_OUT and V_{CC}.

[3] T_{case} is the temperature at the soldering point of the exposed die pad.

[4] Covering downlink frequency range of eUTRAN bands 11, 13, 14 and 17.

[5] Covering downlink frequency range of eUTRAN bands 1, 4 and 10.

3. Pinning information



Transparent top view

Fig 1. SOT908-1 Pin configuration

3.1 Pin description

Table 4. Pin description

Symbol	Pin	Description
n.c.	1, 4	not connected [1]
RF_OUT	2, 3	RF output and supply to the amplifier [2]
V_{CC}	5	bias supply voltage [3]
ENABLE	6	enable
RF_IN	7	RF input [2]
ICQ_ADJ	8	quiescent collector current adjustment by an external resistor
GND	exposed die pad	ground [4]

[1] This pin can be connected to ground.

[2] This pin requires an external DC-blocking capacitor.

[3] RF decoupled.

[4] The exposed die pad of the SOT908-3 also functions as heatsink for the power amplifier.

4. Functional Diagram

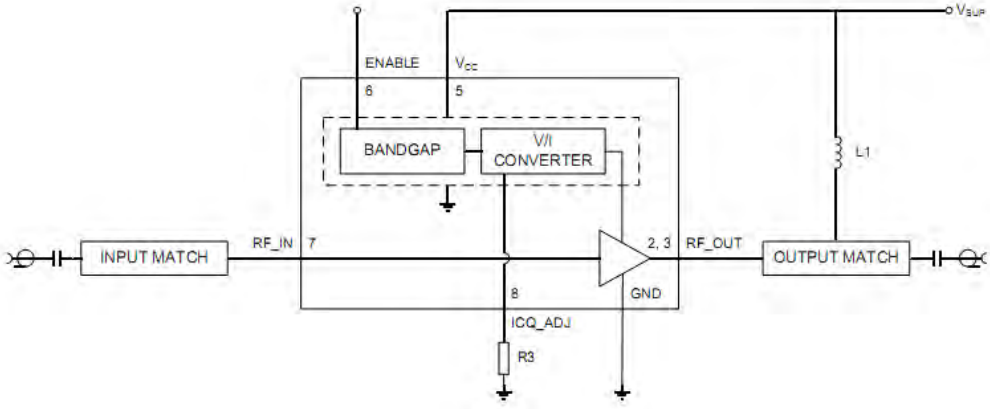


Fig 2. Functional diagram

As can be observed in Fig. 2, the bias and temperature control is fully integrated in the device, to accommodate ease of use in the application. The quiescent current can be adjusted by R3 (on the EVB R3 is a fixed resistor, but can be replaced by a trimmer potentiometer), while the RF can be switched on/off by a logic level (“0” or “1”) on the enable pin (SHDN).

5. Evaluation Board (EVB)

The BGA7130 865 - 880 MHz EVB simplifies the evaluation of the BGA7130 RF MMIC, for the frequency band 865 - 880 MHz The EVB enables testing of the device performance and requires no additional support circuitry. The board is assembled with BGA7130, including input- and output matching components, to optimize the performance. The board is utilized with SMA connectors at both input and output for connection to RF test equipment.

5.1 Application circuit.

In Fig.3 the circuit diagram of the EVB is shown.

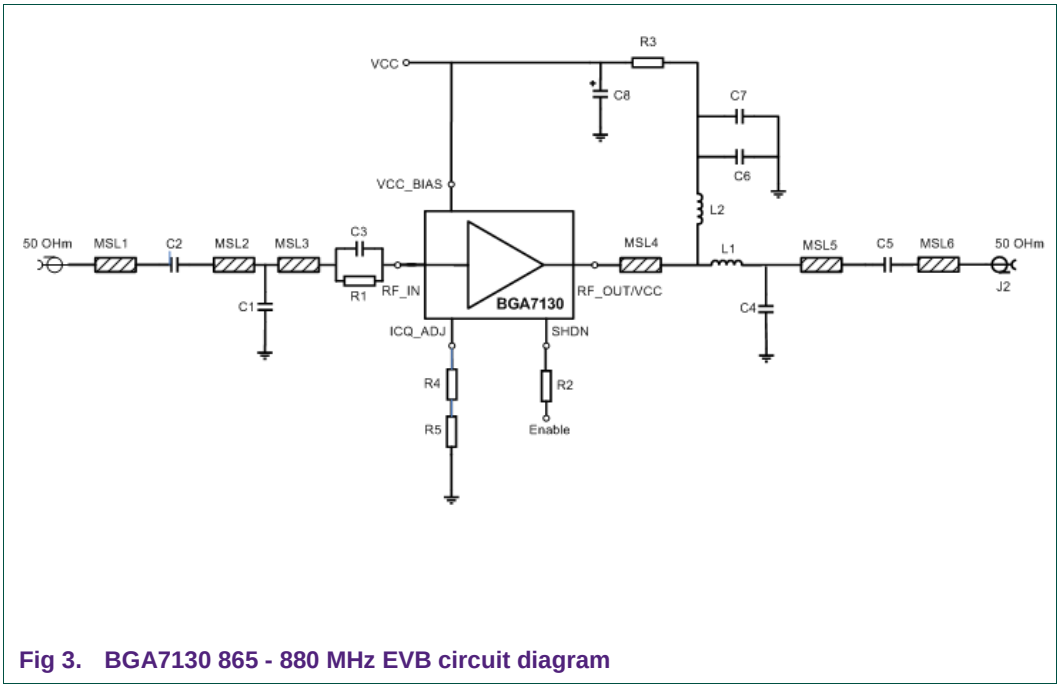


Fig 3. BGA7130 865 - 880 MHz EVB circuit diagram

5.2 Bill of Materials (BOM)

Component	Description	Value	Function	size	Remarks
J1,J2	RF connector	SMA			Emerson Network Power 142-0701-841
J3	DC connector	6 pins			
C8	capacitor	10 uF	DC decoupling		
C7	capacitor	100 nF	DC decoupling	0603	
C6	capacitor	1 nF	DC decoupling	0603	
C1,C5	capacitor	47 pF	DC blocking	0603	
C2	capacitor	15 pF	input match	0603	
C3	capacitor	47 pF	output match	0402	
C4	capacitor	10 pF	output match	0603	
R1	resistor	47 Ω		0402	
R2	resistor	270 Ω		0603	
R3	resistor	0 Ω	bias setting	0603	
R4	resistor	523 Ω	bias setting	0603	
R5	resistor	0 Ω		0603	
MSL1 [1]	micro stripline	W=1.14 mm, S=0.8 mm L=10.95 mm	50 Ohm line		
MSL2 [1]	micro stripline	W=1.14 mm, S=0.8 mm L=8.0 mm	input match		
MSL3 [1]	micro stripline	W=1.14 mm, S=0.8 mm L=1.6 mm	output match		
MSL4 [1]	micro stripline	W=1.14 mm, S=0.8 mm L=6.3 mm	output match		
MSL5 [1]	micro stripline	W=1.14 mm, S=0.8 mm L=3.4 mm	output match		
MSL6 [1]	micro stripline	W=1.14 mm, S=0.8 mm L=10.95 mm	50 Ohm line		
L1	inductor	1.5 nH	output match	0402	Murata LQW15
L2	inductor	68 nH	DC Feed	0603	Murata LQW18AN68NG10

[1] MSL1 to MSL6 dimensions specified as Width(W), Spacing (S) and Length (L)

5.3 Board layout

In Figure 4, the layout of the BGA7130 circuit, as tuned for 865 - 880 MHz is shown.

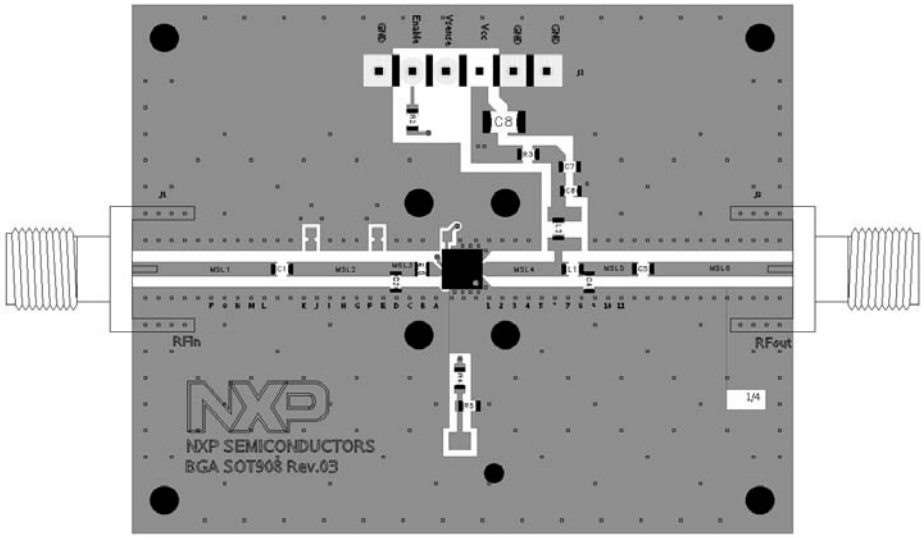


Fig 4. BGA7130 865 - 880 MHz circuit layout

5.4 PCB stack

The PCB is constructed as a four layer PCB (see Fig.5) stack. The width and the gap between the strip line and ground plane are configured such, that in combination with the RO4003C properties (ε_r , height) a 50 Ohm transmission line is defined.

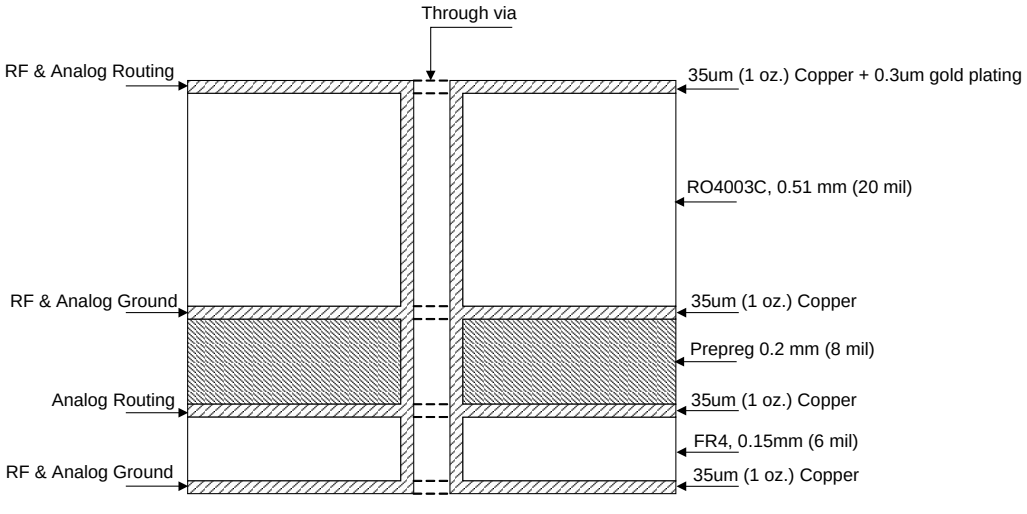


Fig 5. PCB stack build

5.5 Surface mount reflow soldering description

To ensure optimal performance- and lifetime of the device, proper soldering of the device on the PCB is a must. Proper soldering will ensure maximum heat transfer of the device to its environment (either free air or heat sink), hence minimizing the overall thermal resistance in order to keep the junction temperature low. A detailed description for surface mount reflow soldering can be found in the Application Note AN10365, on **www.nxp.com.**

6. Measurement conditions- and set-up's

In this section, the measurement conditions and measurement set-ups are described, as applied for the characterization data in this report.

6.1 Output intercept point (OIP3) or IMD3

As a figure of merit for linearity, the output intercept point (OIP3) is defined (see Fig. 6). The measurement set-up (see Fig.7) is configured to achieve best performance. After the signal generators, a low pass filter (LPF) and isolator are applied, before combining the two signals. This configuration gives best isolation between the generators, hence a pure input spectrum of your signal. IMD3 levels of the input signal < -80 dBc can be achieved, so accurate IMD3 and OIP3 measurement are feasible.

6.1.1 OIP3/IMD3 measurement conditions

The OIP3 (or IMD3) of the EVB is measured with a tone spacing $\Delta f = (f_2-f_1)$ of 1 MHz, and as function of the output power (either the average output power or output power per tone).

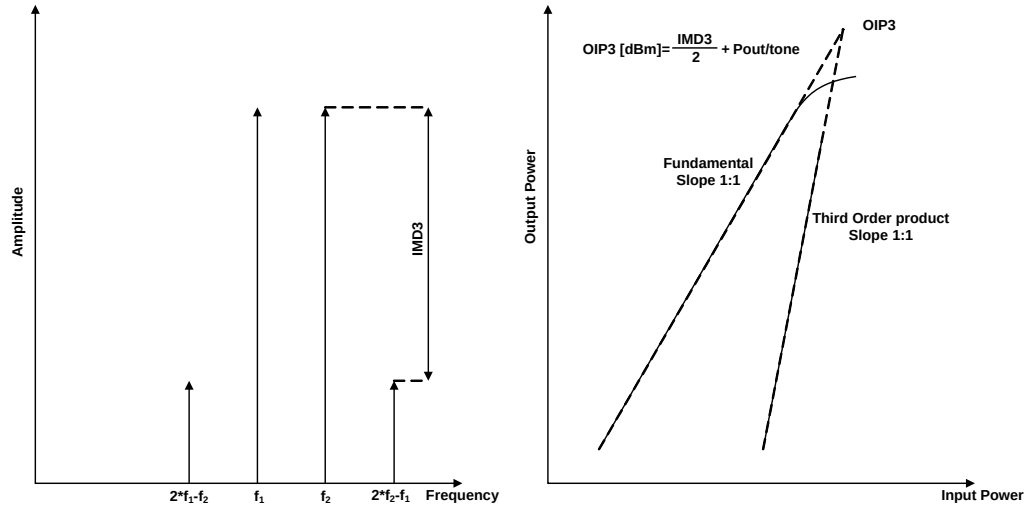


Fig 6. Output Intercept Point definition

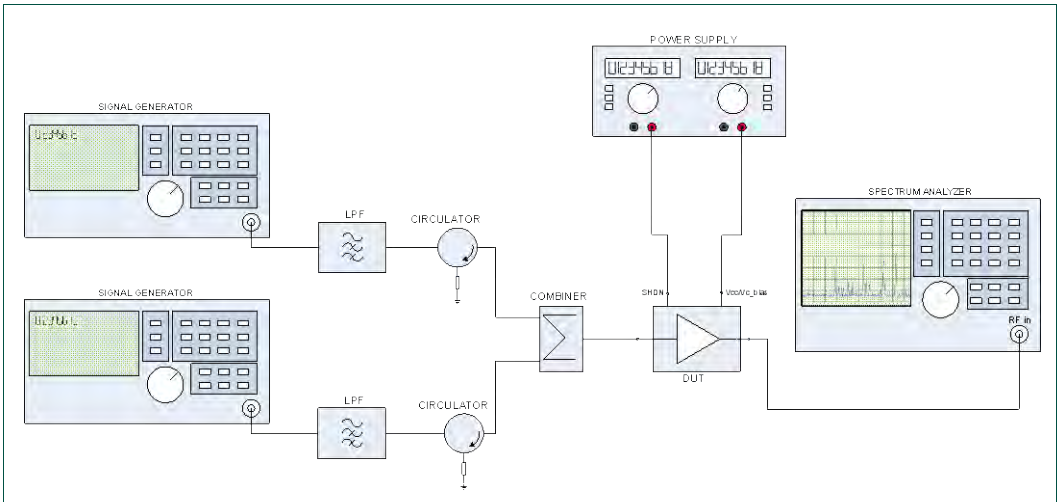


Fig 7. Output intercept Point (OIP3)/IMD3 set-up

6.2 S-parameters and output compression point (P1dB).

Both S-parameters of the EVB and the output compression point are measured with a network analyzer (NWA). The P1dB is measured by sweeping the input power, and observe where the S21 of the device has compressed 1 dB compared to the linear gain (for this measurement a input power calibration with a power head has been performed, in order to accurate measure the input power). The output power of the device is calculated by Pout=Pin*gain(=S21)). See also Fig. 8. To enhance the drive power for the EVB optional a driver amplifier can be applied, in order to prevent that output signal of the EVB drives the receiver of the NWA into compression, and output attenuator can be an option (both driver amplifier and attenuator should be included in the calibration path).

6.2.1 S-parameter measurement conditions

In order to maintain small signal conditions for the S-parameter measurements, an input power of –30 dBm is applied.

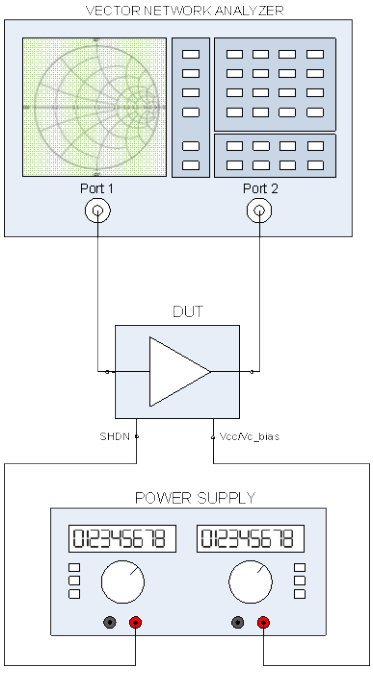


Fig 8. S-parameter and output compression power set-up

6.3 Noise Figure Measurements (NF).

The Noise Figure (NF) of the EVB is measured with a calibrated noise source (with a specified Excess Noise Ratio (ENR), and with a spectrum analyzer with noise measurement option. The system is calibrated with this noise source, in order to measure accurate noise figures (see Fig. 9).

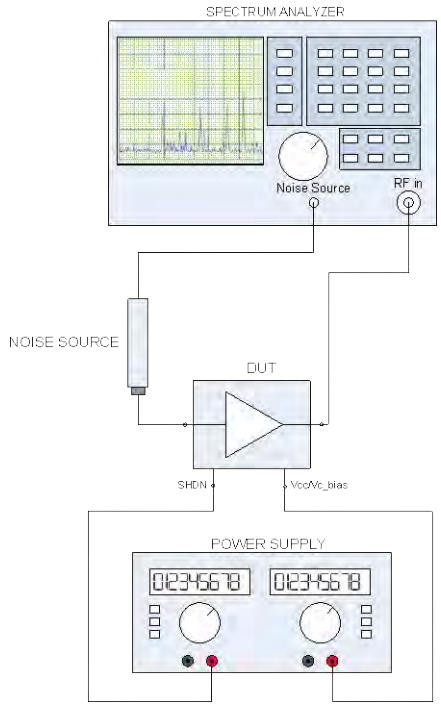


Fig 9. Noise Figure measurement set-up

6.4 Switching time measurements.

The switching times (the RF output of the BGA7130 can be switched on/off by enabling/disabling the devices via control of the SHDN pin) are measured according the set-up, as described in Fig. 10. The RF output is switched on/off by a pulse generator (which also supplies the trigger signal to the oscilloscope), while the RF response is measured with a spectrum analyzer, in the zero span mode. The envelope of the RF output signal is fed to the oscilloscope by means of the VIDEO OUT option of the spectrum analyzer.

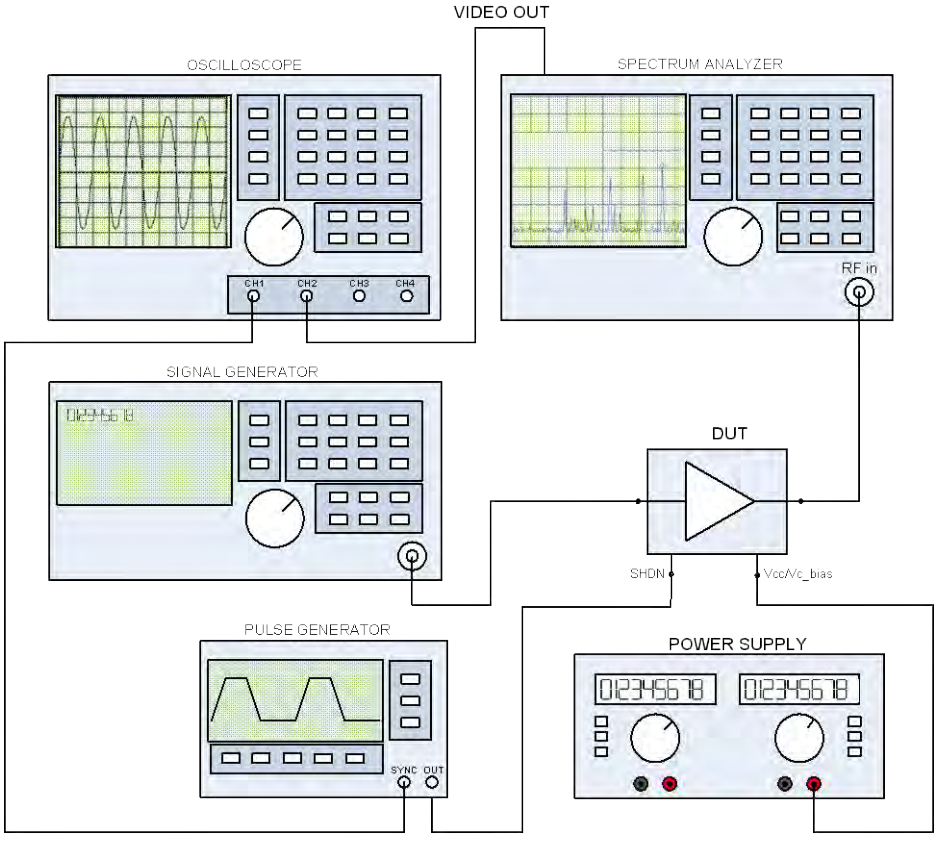


Fig 10. Switching time set-up

7. User instructions

For proper operation of the EVB, the following instructions should be followed:

To power on the device, follow the sequence below:

- Connect the ground to one of the ground pins
- Connect the 5V to the VCC pin
- Connect 5V to the enable pin

To power off the device, follow the sequence below:

- Disconnect 5V to the enable pin
- Disconnect the 5V to the VCC pin
- Disconnect the ground to one of the ground pins

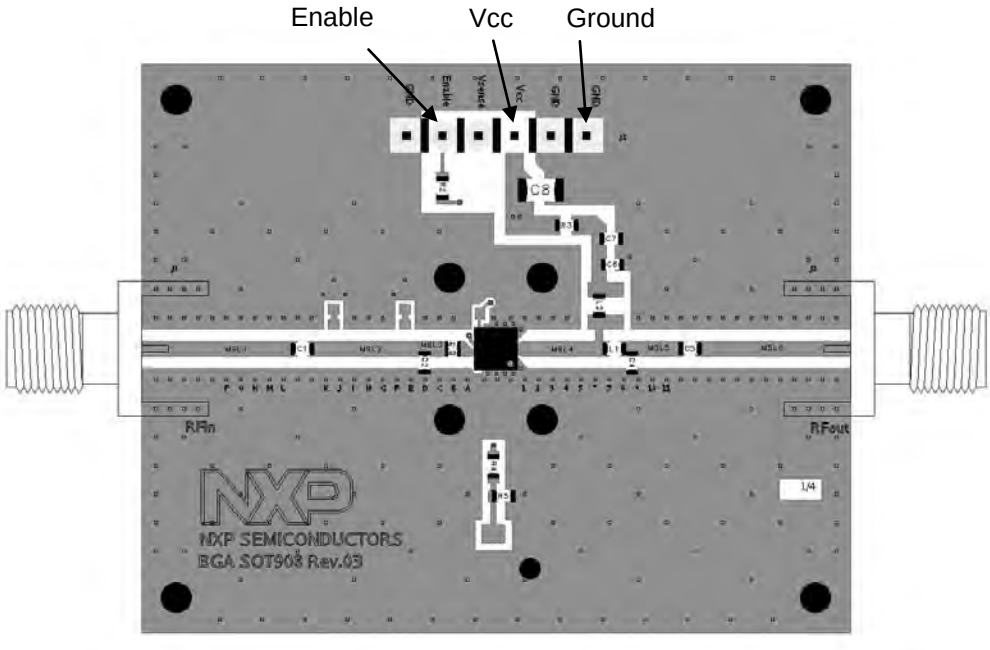
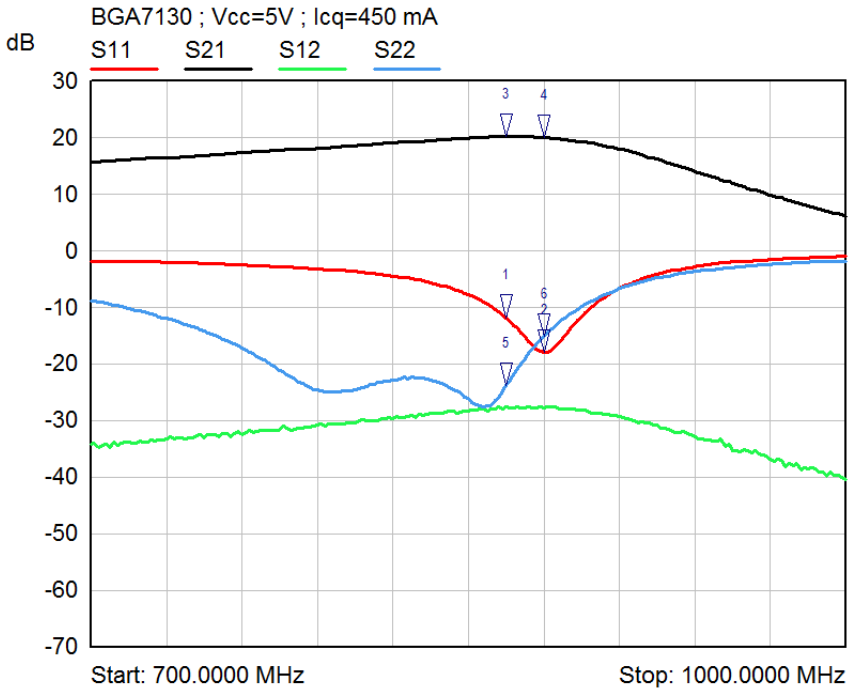


Fig 11. Device DC connections

8. Typical measurement results

8.1 S-parameters: Vcc=5V; Icc=450mA

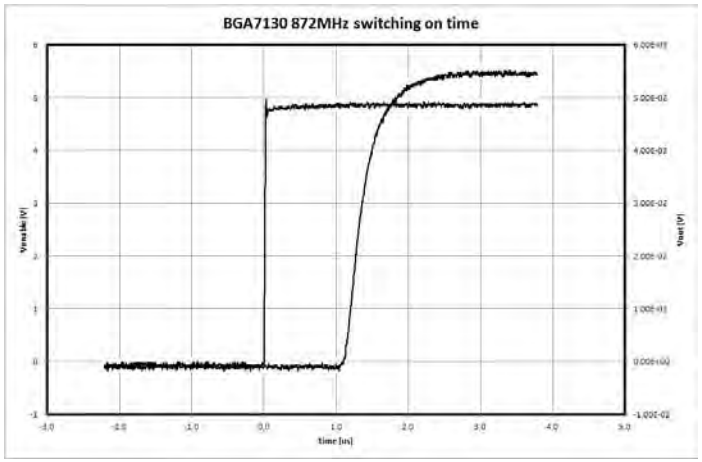


Mkr	Trace	X-Axis	Value	Notes
1	S11	865.0000 MHz	-11.87 dB	
2	S11	880.0000 MHz	-18.03 dB	
3	S21	865.0000 MHz	20.15 dB	
4	S21	880.0000 MHz	20.01 dB	
5	S22	865.0000 MHz	-23.86 dB	
6	S22	880.0000 MHz	-15.15 dB	

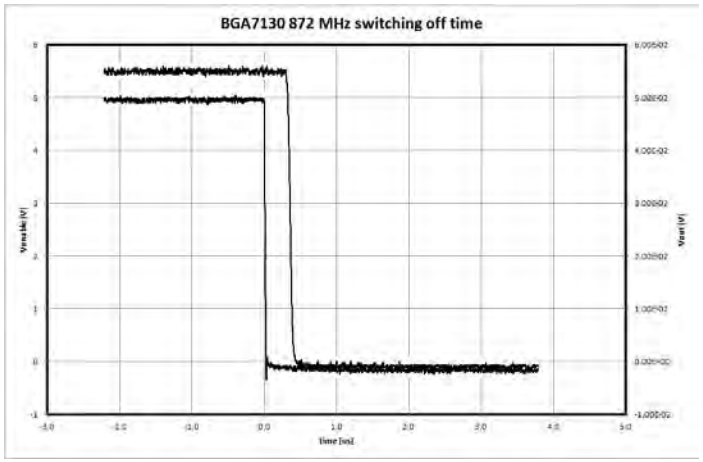
8.2 P1dB and OIP3: Vcc=5V; Icc=450 mA ; frequency = 865 - 880 MHz

freq [MHz]	P1dB [dBm]	OIP3 [dBm]
865	29.7	43
880	29.6	42.5

8.3 Switching times: Vcc=5V; Icc=450 mA ; frequency = 872 MHz



Switching time on



Switching time off

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Date of release: 2 July 2012
Document identifier: AN11190