AN11088

PTN3460 DP to LVDS PCB layout guidelines

Rev. 1 — 25 October 2012 Application note

Document information

Info	Content
Keywords	DisplayPort, LVDS, PTN3460, PCB, Layout, signal integrity, symmetry, loss, jitter
Abstract	This document provides a practical guideline for incorporating the DisplayPort receiver and LVDS transmitter ICs layout into PCB designs.

Revision history

Rev	Date	Description
v.1	20121025	application note; initial release

Contact information

For more information, please visit: **http://www.nxp.com**

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1. Introduction

This document provides a practical guideline for incorporating the NXP DisplayPort (DP) to LVDS bridge IC's layout into a Printed-Circuit Board (PCB) design.

DisplayPort interconnect is a point-to-point layout of serial differential signal trace pairs. The document provides guidelines for DP lane connection for the PCB traces, vias and AC coupling capacitors. The most important considerations are to minimize loss and jitter, and to maintain signal integrity.

These are general guidelines only. Board designers should carefully weigh design trade-offs and use simulation analysis to ensure a successful implementation.

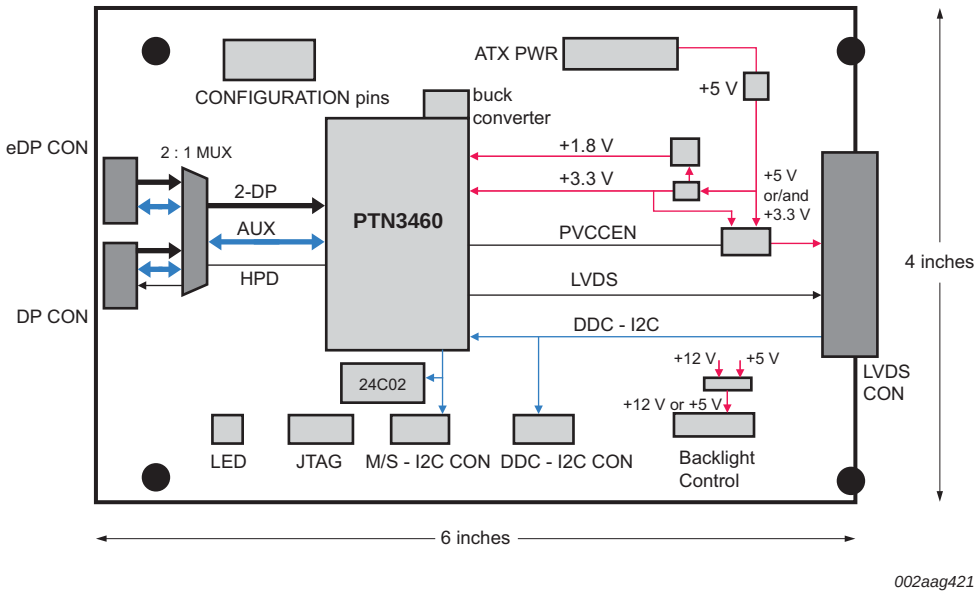

Fig 1. DP-LVDS block diagram

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2. Layout and design for optimum performance and EMI

DisplayPort is a scalable digital display interface. The interface is designed to support both internal chip-to-chip and external box-to-box digital display connections. The Main Link consists of one, two or four AC-coupled, doubly terminated differential pairs (lanes). Two link rates are supported: 2.7 Gbit/s (HBR) and 1.62 Gbit/s per lane (RBR).

2.1 Reference plane partitioning and overall supply and grounding

DisplayPort requires no new PCB technology. Generally PC system boards are designed with 4-layer FR4 stack-up, with 1080 prepreg and 47 mil core, and a 0.062 inch nominal thickness.

To minimize loss and jitter, the most important considerations are to design to a target impedance and to keep tolerance small.

A signal pair should avoid discontinuities in the reference plane, such as splits and voids. When a signal changes layers, the ground stitching vias should be placed close to the signal vias. A minimum of 1 to 3 stitching vias per pair of signals is recommended. Never route a trace so that it straddles a plane split.

2.2 PCB stack-ups

Layer 1: Top signal layer, some ground islands for PTN3460 center pad.

Layer 2: Solid ground plane.

Layer 3: Split power plane for 3.3 V, 1.8 V and 5 V. Some ground islands for DP, LVDS traces layout.

Layer 4: Bottom signal layer. Ground island around LVDS connector.

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Stack Up

PCB Stack Up				Impedance			
Layer	Type	Thickness (mil)					
Top side solder mask			0.50 mils	Single		DIFF	
L1	TOP	copper+plating	1.58 mils	8 mils , 50Ω±5Ω	53.09 Ω	6/8/6 mils , 100Ω±5Ω	101.26 Ω
		Prepreg	6.00 mils				
L2	GND	copper	1.30 mils				
		core	42.60 mils				
L3	GND	copper	1.30 mils				
		Prepreg	6.00 mils				
L4	Bottom	copper+plating	1.58 mils	8 mils , 50Ω±5Ω	53.09 Ω	6/8/6 mils , 100Ω±5Ω	101.26 Ω
Bottom side solder mask			0.50 mils				
TOTAL			61.36 mils 1.56 mm				

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Fig 2. DP-LVDS PCB stack-up example

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2.3 Traces

2.3.1 Impedance

PTN3460 I/O impedance is targeted at 50 Ω single-ended and 100 Ω differential. It is recommended that DP link PCB traces maintains 50 Ω ± 15 % single-ended and 100 Ω ± 20 % differential impedance to maintain signal integrity.

In *'Eaglelake platform design guide'*, Intel recommends 95 Ω ± 15 % differential impedance for DP and HDMI/DVI signals, and 85 Ω ± 15 % for PCIe.

The impedance target has been lowered in the Calpella platform, which is for year 2009, including docking and add-in card. For all differential signals, DP, HDMI/DVI, and PCIe, impedance is targeted at 85 Ω ± 15 %.

There are two reasons mainly for this non-100 Ω recommendation. One is the signal loss. The higher the impedance is, the more the loss is. The trace length between the chip set and the connector may be as long as 2 inches to 4 inches, which may contribute a significant amount of loss.

2.3.2 Width and spacing

The coupling of the intra-pair differential signals and increased spacing to neighboring signals help to minimize harmful crosstalk impacts and Electro-Magnetic Interference (EMI) effects. In the microstrip case, a differential trace should be 5 mils wide, with a 7 mil wide air gap spacing between the two traces of a pair.

The spacing between pairs and to all non-DP/LVDS signals should be at least four times the dielectric height. If the non-DP/LVDS signals have significantly higher voltage levels or edge rate than the DP/LVDS signal, the space should increase to 30 mils in order to avoid coupling.

2.3.3 Length and length matching

Trace length greatly affects the loss and jitter budgets of the interconnection. The PCB trace may introduce 1 ps to 5 ps of jitter and 0.35 dB to 0.50 dB of loss per inch.

Long distance traces should be routed at an off-angle to the X-Y axis of a PCB layer, in order to distribute the effects of fiberglass bundle weaves and resin-rich areas of the dielectric.

The two traces of a pair should be symmetrically routed.

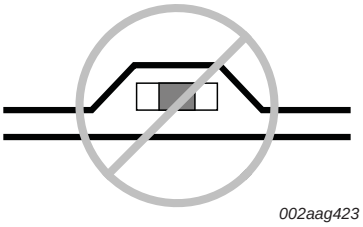

Fig 3. Non-symmetrical routing should be avoided

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The length difference between a differential pair should be limited to 5 mils maximum. Length matching is required per segment, and any length added (typically a 'serpentine' section) for the sake of matching a pair should be added near the location where the mismatch occurs.

Keep the delta in each inter-pair to be less than 0.1 inch (0.254 cm).

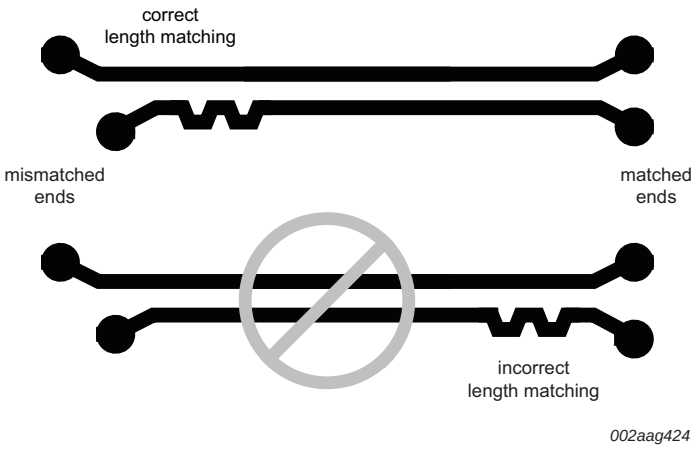

Fig 4. Length matching near location of mismatch

2.3.4 Bends

The use of bends should be kept to a minimum since a bend can introduce common mode noise into the system, which will affect the signal integrity and EMI of the differential pair.

Bends on traces should be ≥ 135°. Tighter bends should be avoided because they impact the loss and jitter budgets.

If bends are used, the following guidelines are recommended to avoid tight bends (see Figure 5).

- Keep all angles between traces (α) ≥ 135°.
- Maintain an air gap (A) of ≥ 20 mils.
- Segments such as B and C, which flank a bend, should have a length ≥ 1.5 times the width of the trace.

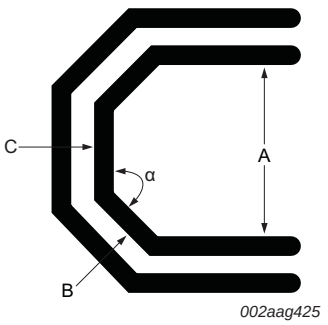

Fig 5. Trace bending guidelines

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The number of left and right bends should be as close to equal as possible, to minimize the length mismatch.

When a serpentine section is used to match one length to another, as shown in Figure 6, the length of each jog must be at least three times the trace width. The maximum distance between traces in a serpentine section should be less than two times the distance between traces in a non-serpentine section.

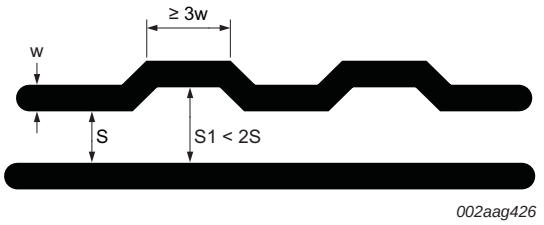

Fig 6. Serpentine section

An uncoupled section of trace routing into a pin or a ball should be ≤ 45 mils when using multiple bends, as shown in Figure 7.

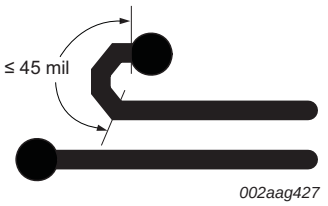

Fig 7. Uncoupled trace using multiple bends

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3. Power supply

External power supply is required to power DP-LVDS application board.

First application board is for AIO (All In One) AUO 21.5” panel, which draws a lot of power, hence an ATX switching power supply is used to anticipate the power hunger of AUO panel.

Second application board is targeted for NoteBook application, hence NB battery pack will be used for a more compact design.

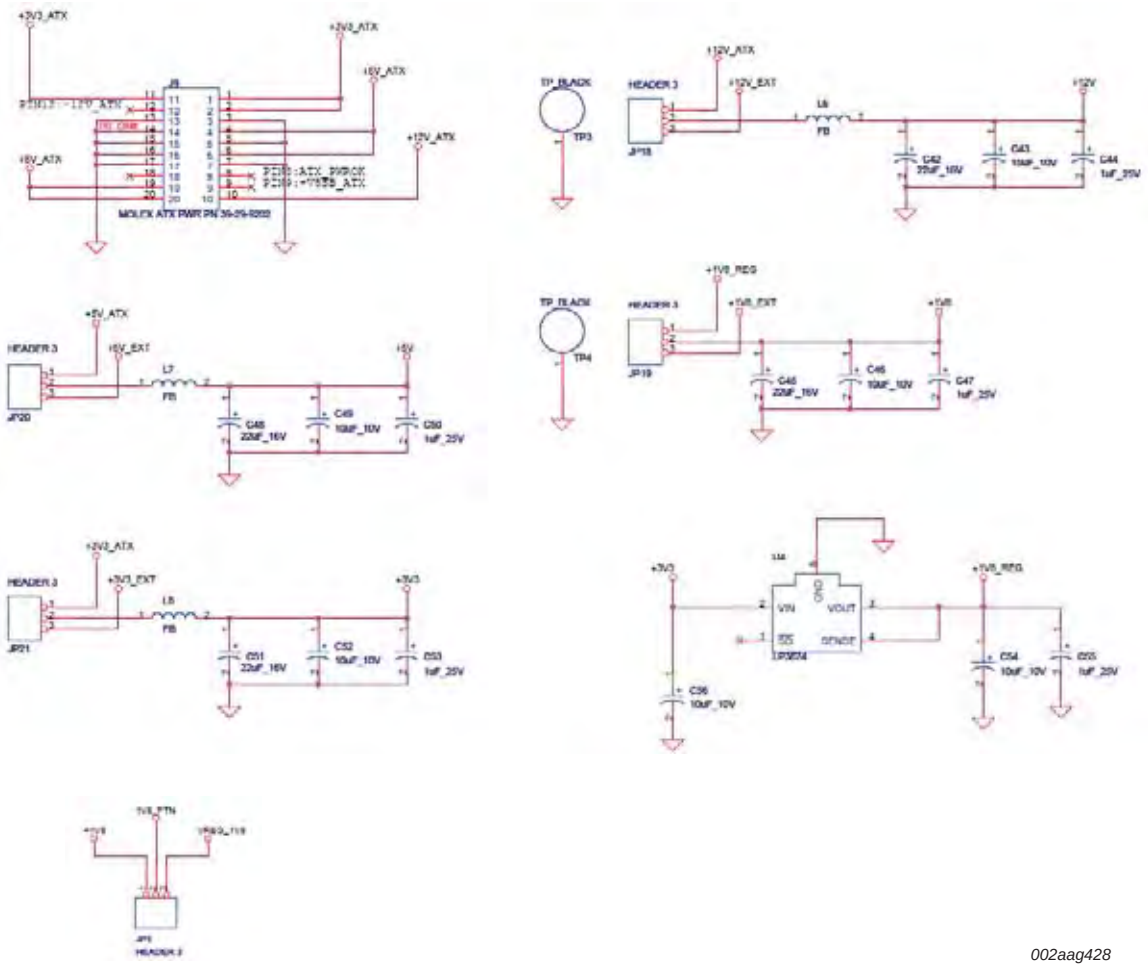

Fig 8. DP-LVDS power tree example

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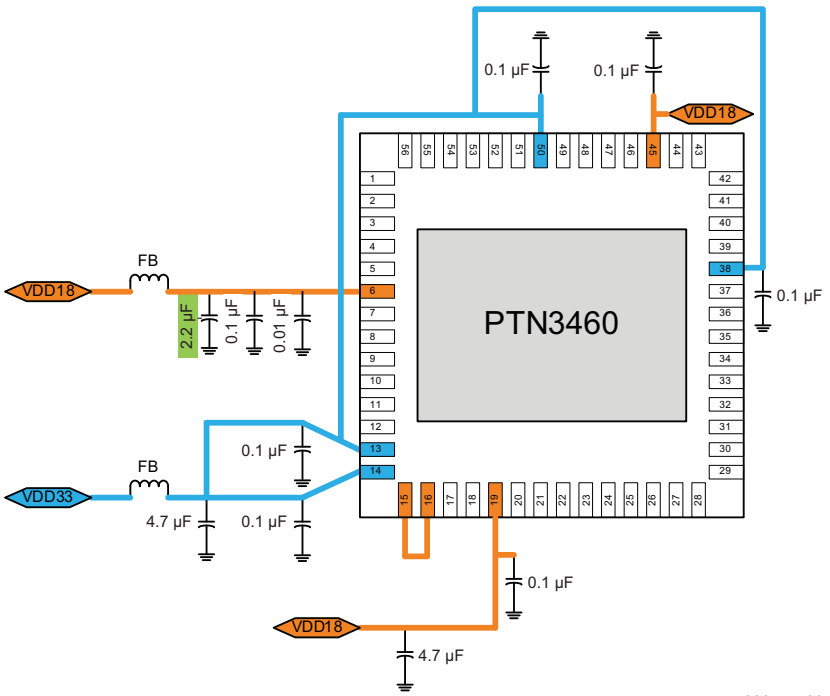
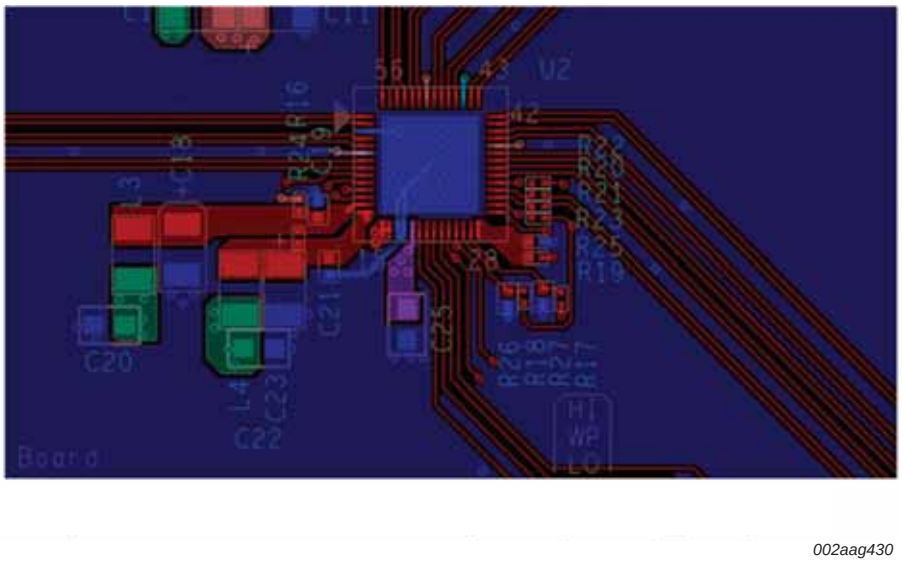


Fig 9. PTN3460 power scheme

3.1 Power supply filtering and bypass capacitors

The main power of DP-LVDS is 3.3 V. Core voltage 1.8 V can come from system board, or it can be generated from internal LDOs inside PTN3460.



C24, C26 on the back side near pin 19 (VREG_1V8).

Fig 10. Core and AUX LDO filtering example

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Use only X5R or X7R type decoupling capacitors (do not use Z5U or Y5U types). Z5U or Y5U will lose 20 % to 30 % of its capacitance value at high temperature.

Also use 10 nF (103 pF) to help suppress high frequency noise.

Bypass capacitor on 3.3 V power supply pin should be connected to the pin with a wide trace.

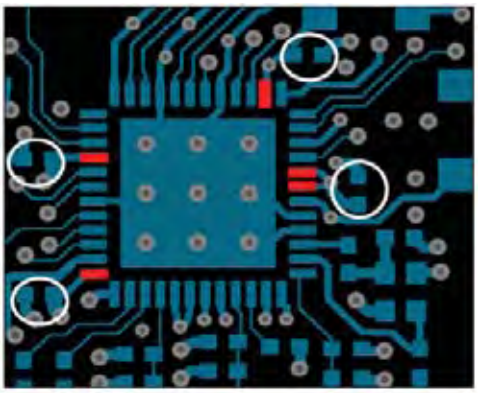

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Fig 11. Power supply filtering and bypass layout example

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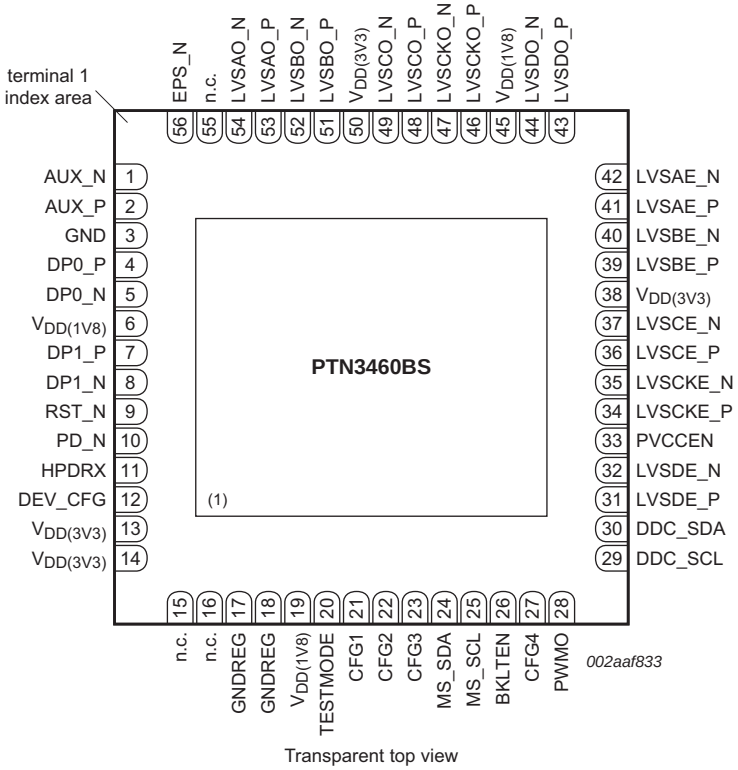
4. PTN3460 HVQFN56 package

PTN3460 is packaged in an HVQFN56 package (plastic thermal enhanced thin quad flat package; no leads; 56 terminals; body 7 mm × 7 mm × 0.85 mm; 0.4 mm pitch.



(1) Center pad is connected to PCB ground plane for electrical grounding and thermal relief.

Fig 12. PTN3460 pin configuration for HVQFN56

4.1 HVQFN exposed center pad solder lands

PTN3460 uses HVQFN56 package.

The HVQFN package exposed center pad must be soldered to a corresponding solder land on the board for enhanced thermal, as well as electrical ground, performance.

During reflow soldering, solder past melts and gas or trapped air is released, causing splattering or solder balling. Solder balling and splatter can be minimized if the solder past is printed as a number of individual dots, instead of one large deposit, and if the solder past is kept at a sufficient distance from the edge of the solder land.

The solder paste pattern area should cover 35 % of the solder land area. When printing solder past on the exposed die pad solder land, the solder past dot area should cover not more than 20 % of this solder land area. Furthermore, the paste should be printed away from the solder land edges. This is illustrated in Figure 13; the solder paste pattern area lies within the boundary indicated by the red line and it is divided by the entire solder land area.

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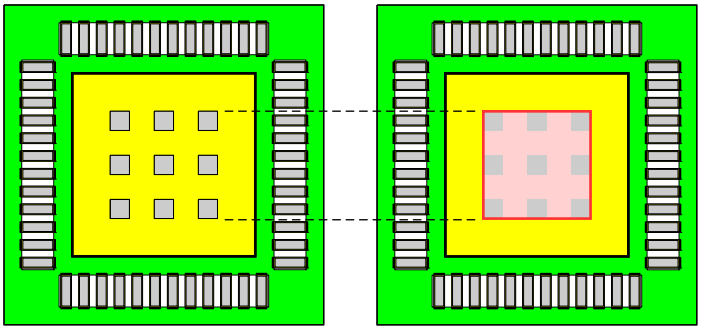

Fig 13. Solder paste dot area (left) and paste pattern area (right)

The PTN3460 exposed center pad should be connected to the ground plane as illustrated in Figure 14.

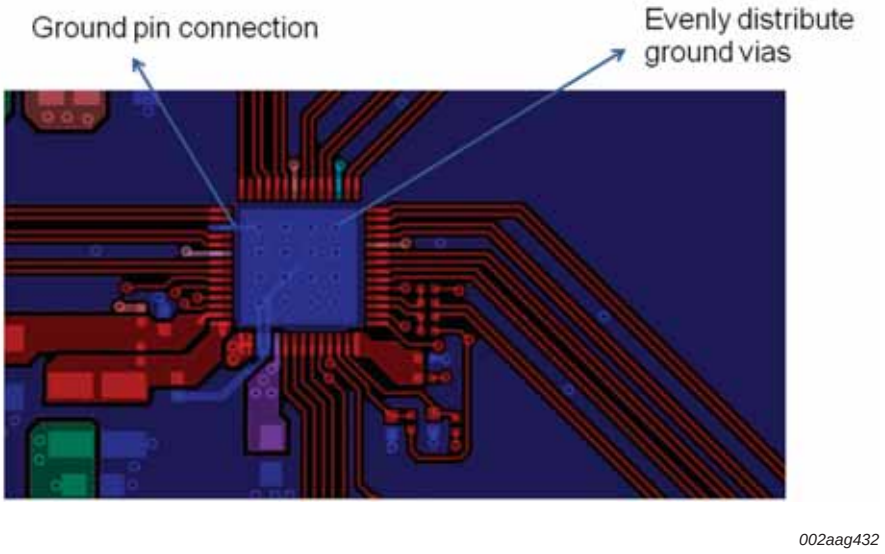

Fig 14. PTN3460 center pad connection example

5. Test points, vias and pads

Signal vias affect the overall loss and jitter budgets. Each via pair may contribute 0.25 dB of loss in some corner cases. Vias may limit the achievable maximum routing length.

Vias should have a pad size of 25 mils or less, and a finished hole size of 14 mils or less. Two vias must be placed as a symmetric pair in the same location.

Test points (which can be vias, pads or components) and probe pads should be placed symmetrically in series. Stubs should not be introduced on differential pairs. Refer to Figure 15 for illustrations of correct and incorrect placements.

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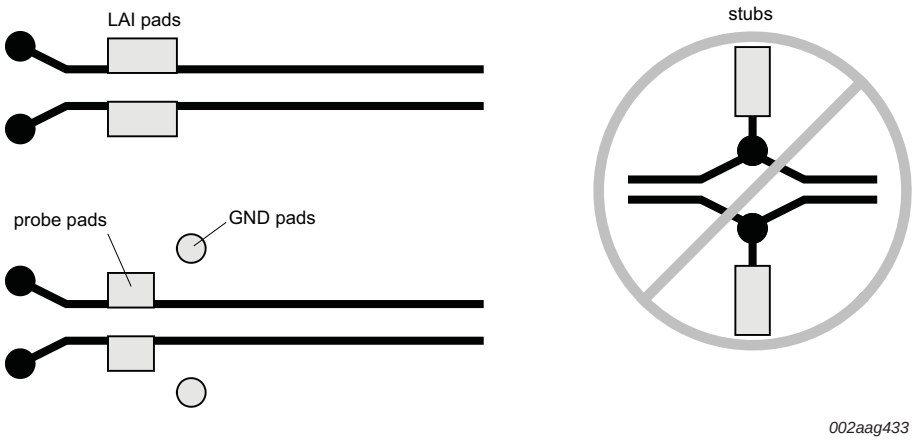

Fig 15. Test points and probe pads

6. DisplayPort receiver interface

Main differential pairs and AUX channel are routed with 100 Ω impedance. The important parameters to calculate the impedance are:

- PCB thickness
- Distance to ground plane
- Trace width
- Trace spacing
- PCB permittivity

Guard grounds are used to isolate the pair. This helps to eliminate crosstalk between traces. Trace lengths are matched on the same pair.

Fig 16. Main video lane 0, 1 layout example

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7. AC coupling capacitors

DP requires AC coupling between transmitter and receiver. The AC coupling capacitors for both differential pair signals must be the same value, same package size, and have symmetric placement. If possible, TX traces should route on the top layer.

The capacitor value must be in the range of 75 nF to 200 nF (100 nF is best). The 0402 package size is preferred, and 0603 is acceptable. C-pack is not allowed.

The breakout into and out of capacitors should be symmetrical for both signal lines in a differential pair. The trace separation for routing to pads must be minimized in order to optimize tight coupling between the signal pairs.

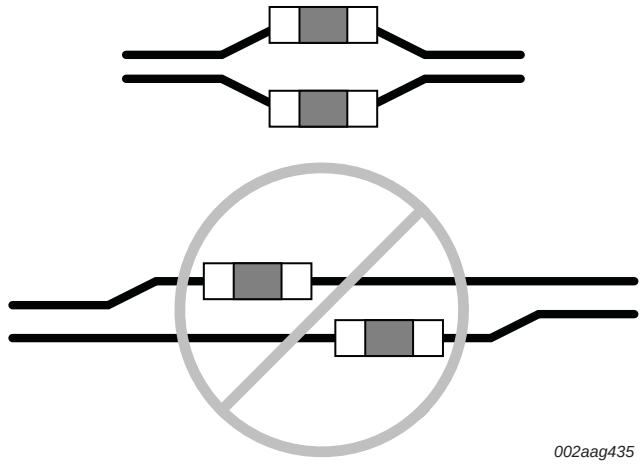

Fig 17. Placement of AC coupling capacitors

Capacitors for AUX pair should be placed close to the DP receptacle next to pin 15 and pin 17.

When signals change planes, the ground plane needs to move along to keep constant trace impedance. On DPVGA a ground island is inserted on the V_{CC} plane for this purpose.

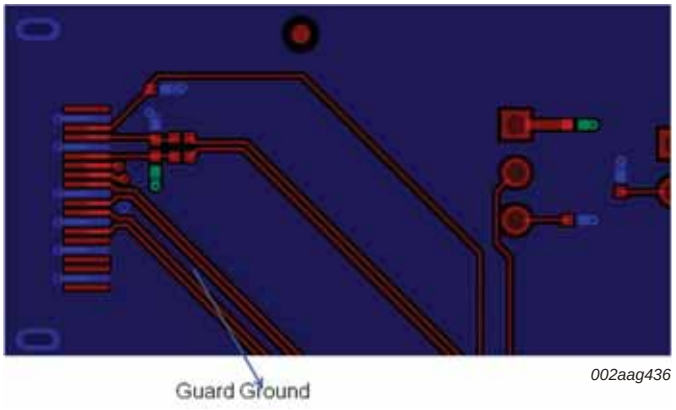

Fig 18. AUX channel layout example

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Ground pads of the DP plug footprint should be connected directly to ground plane with short traces.

8. LVDS transmitter interface

Similar to DisplayPort receiver signals, LVDS also utilizes a differential transmission scheme, two lines for every LVDS signal. They should be routed with 100 Ω impedance. For successful transmission of LVDS signals over differential traces, the following guidelines should be followed while laying out the board:

- Run the differential traces as closely as possible after they leave the driving IC to ensure minimal reflections and maintain the receiver's common mode noise rejection. Also, maintain constant distance between the differential LVDS signals over the entire length of the traces to avoid discontinuities in the differential impedance.
- Keep the electrical lengths between the differential LVDS traces the same to minimize skew.
- Minimize the number of vias or other discontinuities on the signal path.
- Any parasitic loading, such as capacitance, must be present in equal amounts to each line of the differential pair.
- To avoid signal discontinuities, arcs or 45° traces are recommended instead of 90° turns.

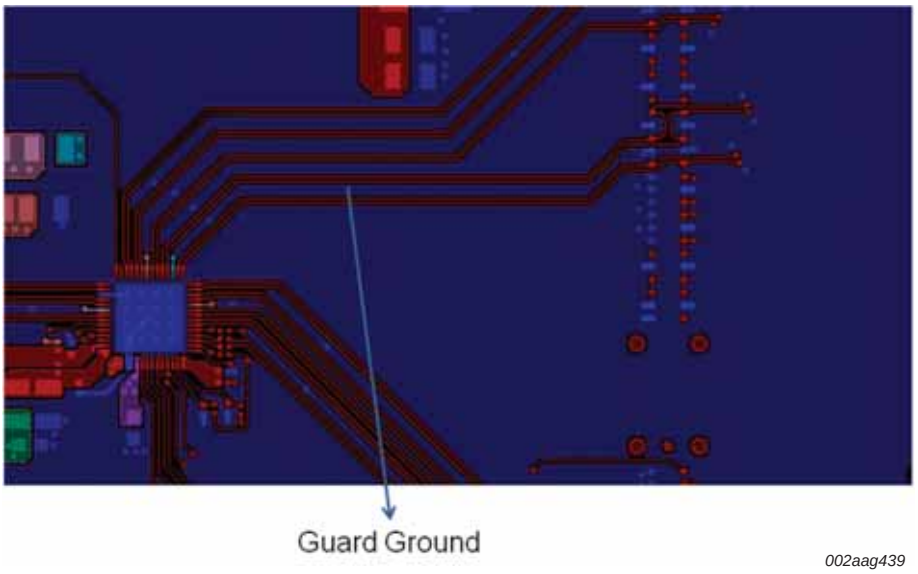

Fig 19. LVDS layout example

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8.1 Impedance matching

Impedance matching is very important for LVDS, even for very short runs. Any discontinuities in the differential LVDS traces will cause signal reflections, thereby degrading the signal quality. These discontinuities also increase the common mode noise and will be radiated as EMI. The LVDS outputs, being current mode outputs, need a termination resistor to close the loop and will not work without the resistor termination. The termination resistor is chosen to match the differential impedance of the transmission line and can range from 90 Ω to 110 Ω (typically 100 Ω). This termination resistor should be placed between the differential lines and close to the LVDS receiver buffer. See illustration below in Figure 19.

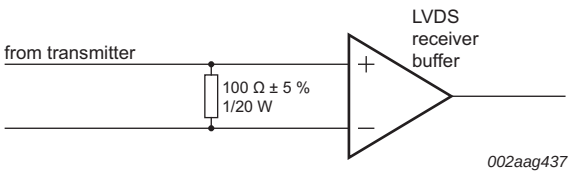

Fig 20. LVDS termination scheme

8.2 Crosstalk between LVDS and single-ended signals

To reduce crosstalk between LVDS and single-ended signals, such as LVTTL, SSTL-2 and similar standards, the differential LVDS signals must be isolated from single-ended signals. On the same PCB layer, the single-ended signals should be placed at least 12 mm from the LVDS signals to avoid crosstalk effects. The V_{CC} and ground planes can also be used to isolate the LVDS signals from the single-ended signal layers.

8.3 LVDS connectors

Connectors can be used to connect the LVDS signals from one board to another.

Figure 21 is an illustration of good connector and bad connector for LVDS.

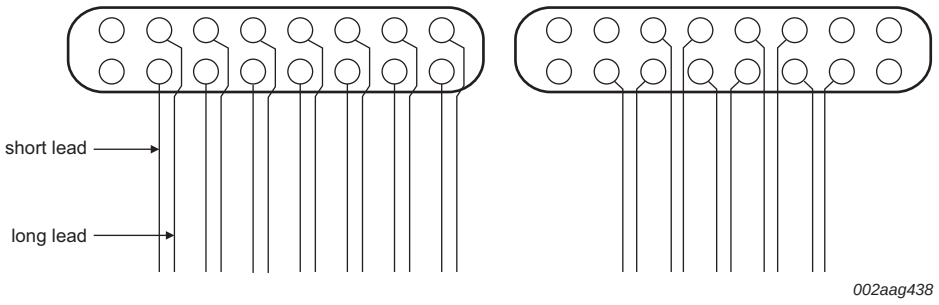

Fig 21. Bad (left) and good (right) LVDS connector

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9. General high-speed board design guidelines

The DP signals on the board work at 1.6/2.7 Gbit/s speed, the LVDS data rate can be as high as 112 MHz × 7 × 3 = 2.352 Gbit/s (112 MHz × 7 × 4 = 3.136 Gbit/s) per lane. The high data rate requires some specific implementations in the PCB layout design. The following is the summary of guideline:

- The differential pair must be routed symmetrically. Keep all differential signal traces the same length. The difference in intra-pair trace length should be less than 5 mils. The delta in inter-pair trace length should be less than 0.1 inch.
- Maintain 50 Ω ± 15 % single-ended and 100 Ω ± 20 % differential impedance.
- Do not route high speed signals over any plane split; use only one ground plane underneath the differential signals.
- Avoid any discontinuity for signal integrity. Differential pairs should be routed on the same layer. The number of vias on the differential traces should be minimized. Test points should be placed in series and symmetrically. Stubs should not be introduced on the differential pairs.
- Use caution with the exposed center pad solder land for HVQFN package.

10. Abbreviations

Table 1. Abbreviations

Acronym	Description
AUO	AU Optronics
AUX	Auxiliary channel
ATX	Advanced Technology Extended
DDC	Direct Display Control
DP	DisplayPort
DPVGA	DisplayPort Video Graphics Array
DVI	Digital Visual Interface
HBR	High Bit Rate
HDMI	High Definition Media Interface
I/O	Input/Output
IC	Integrated Circuit
LDO	Low-DropOut regulator
LVDS	Low Voltage Differential Signaling
NB	Note Book
PCB	Printed-Circuit Board
PCIe	PCI (Peripheral Component Interconnect) Express
RGB	Red, Green, Blue (refers to analog video component signals)
RBR	Reduced Bit Rate
TTL	Transistor-Transistor Logic

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13. Contents

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