AN10792

TDA8034HN - Smart Card reader interface

Rev. 1.1 — 6 June 2016 Application note

Document information

Info	Content
Keywords	TDA8034HN, Smart Card Interface, Pay TV, STB, NDS, ISO 7816-3
Abstract	This application note describes the smart card interface integrated circuit TDA8034HN. This document helps to design the TDA8034HN in an application. The general characteristics are presented and different application examples are described.

Revision history

Rev	Date	Description
1.1	20160606	Description of upgrade from C1 to C2
1.0	20121204	First official release

Contact information

For more information, please visit: http://www.nxp.com

1. Introduction

1.1 Presentation

The TDA8034HN is a smart card interface device forming the electrical interface between a micro controller and a smart card. This device mainly supports asynchronous cards (micro controller-based IC cards).

The electrical characteristics of the TDA8034HN are in accordance with NDS requirements (IRD Electrical Interface Specifications doc n° LC-T056) and also comply with ISO7816-3 for class A, B and C cards.

The TDA8034HN can be used in various applications such as pay-TV, Point-Of-Sale terminals (POS), public phones, vending machines, and many conditional access applications (i.e. internet ,...).

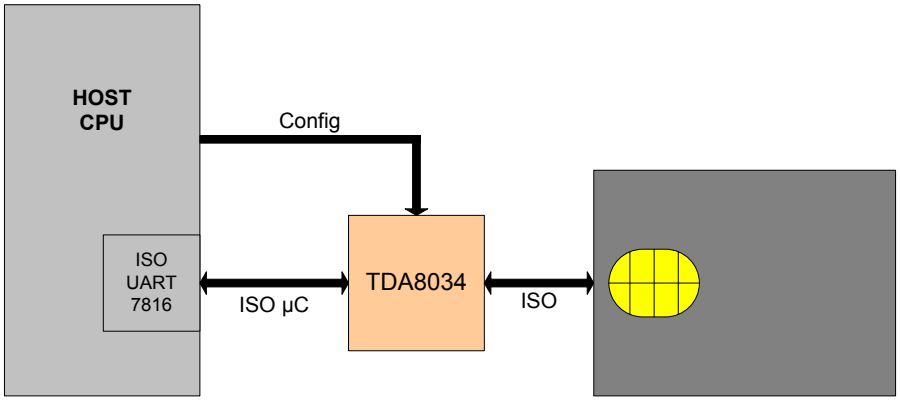


Fig 1. Simplified interfacing view

In the whole document, the TDA8034HN will be referred as TDA8034.

2. Power supply

2.1 Power supply pins

Three pins are used to supply the TDA8034: $V_{DD(INTF)}$, V_{DD} and V_{DDP}.

$V_{DD(INTF)}$ is dedicated to the interface supply. All signals which are interfaced with the host are referenced to this voltage supply.

The next table describes all the pins that must be referenced to $V_{DD(INTF)}$.

Table 1. $V_{DD(INTF)}$ referenced pins

Pin name	Comment
CMDVCCN	Smart card activation. Controlled by a microcontroller GPIO
RSTIN	RST pin management. Controlled by a microcontroller GPIO
EN5V_3VN	Choice of the smart card voltage. Can be controlled by the microcontroller or connected directly to GND or $V_{DD(INTF)}$
EN1.8VN	Choice of the 1.8V smart card voltage. Can be controlled by the microcontroller or connected directly to GND or $V_{DD(INTF)}$
CLKDIV1	Control of the clock division. Can be controlled by the microcontroller or connected directly to GND or $V_{DD(INTF)}$
CLKDIV2	Control of the clock division. Can be controlled by the microcontroller or connected directly to GND or $V_{DD(INTF)}$
PRESN	Not connected to the microcontroller but reference to $V_{DD(INTF)}$. The smart card connector presence switch must use $V_{DD(INTF)}$
OFFN	Output to the host. Must be connected to the microcontroller and therefore have the same level
IOUC	Smart card data. Controlled by the microcontroller
AUX1UC	Management of AUX1. Controlled by the microcontroller
AUX2UC	Management of AUX2. Controlled by the microcontroller

V_{DD} is used to supply the core of the TDA8034 (mainly the digital part). It must be in the range from 2.7 to 3.6 volts. In most of the application, if $V_{DD(INTF)}$ is in the range accepted by V_{DD}, V_{DD} and $V_{DD(INTF)}$ can be connected together.

V_{DDP} is the power supply for the card voltage generator. An LDO converts this voltage to the level needed on the smart card side (5V, 3V or 1.8V). As there is no step-up converter, it is mandatory that V_{DDP} is higher than the required V_{CC}.

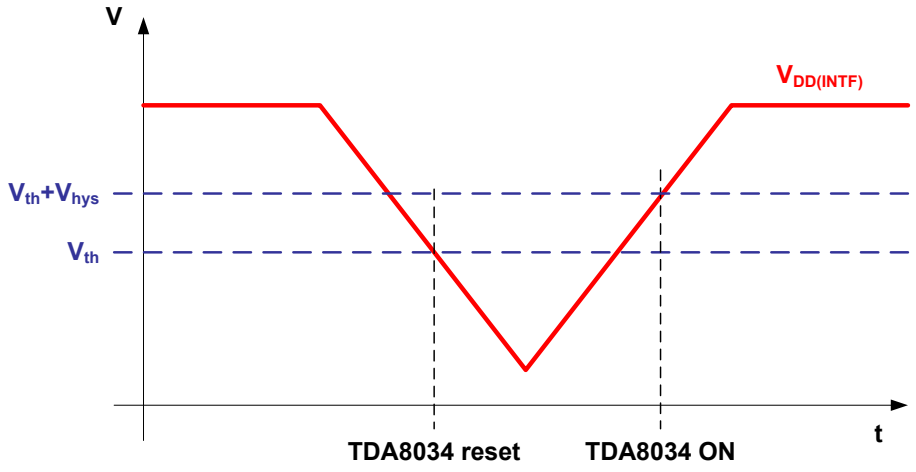
2.2 Supply supervisor

2.2.1 Main principles

The TDA8034 supervises the voltage level of V_{DD}, V_{DDP} and $V_{DD(INTF)}$. For V_{DD} and V_{DDP} supervision, the threshold is internally fixed. For $V_{DD(INTF)}$, the threshold can be fixed either internally or externally using the PORAdj pin.

The following figure explains the supervision for all the supplies.

Then the table gives the threshold values for each input.



(1) When one power supply input falls below its corresponding threshold, the TDA8034 is in reset mode. When all the levels are above their threshold + the hysteresis, the TDA8034 is ON.

Fig 2. Supply supervisor principles

The hysteresis value is null when a PORADJ resistor bridge is used to fix the threshold externally on $V_{DD(INTF)}$.

2.2.2 Supervision with PORAdj used

The TDA8034 allows to fix externally the threshold on $V_{DD(INTF)}$. This can be done by using an external resistor bridge on the PORAdj pin.

The supervision principle is given in the next two pictures:

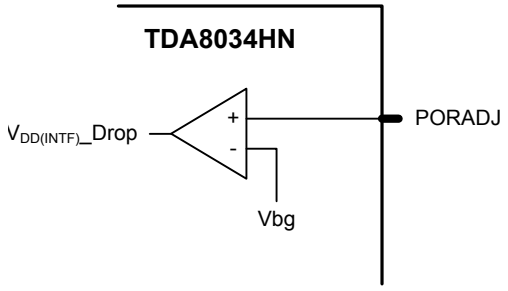


Fig 3. $V_{DD(INTF)}$ supervision – PORADJ level detector

The TDA8034 compares the pin voltage level on pin PORADJ to an internal voltage reference called Vbg.

When PORADJ falls below Vbg, the TDA8034 is reset:

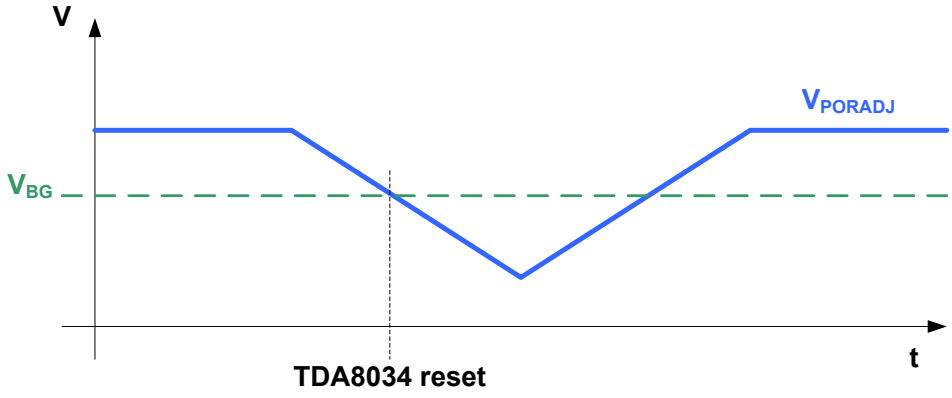


Fig 4. $V_{DD(INTF)}$ supervision – Reset when PORADJ falls

Warning: in this particular case, the hysteresis on the supervisor is null. Then the threshold is the same when the supply rises as when it falls.

To detect a drop on $V_{DD(INTF)}$, a voltage level referred to $V_{DD(INTF)}$ must be connected to PORADJ. This voltage level can be obtained with a resistor bridge:

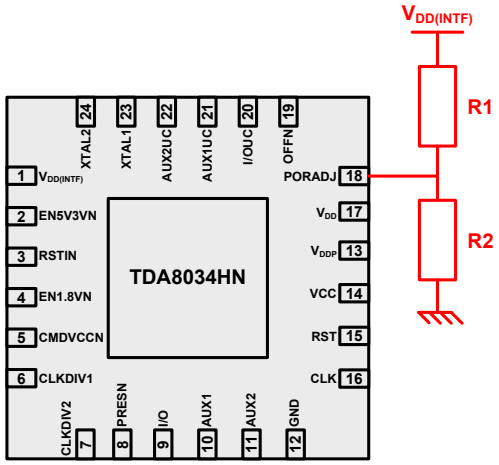


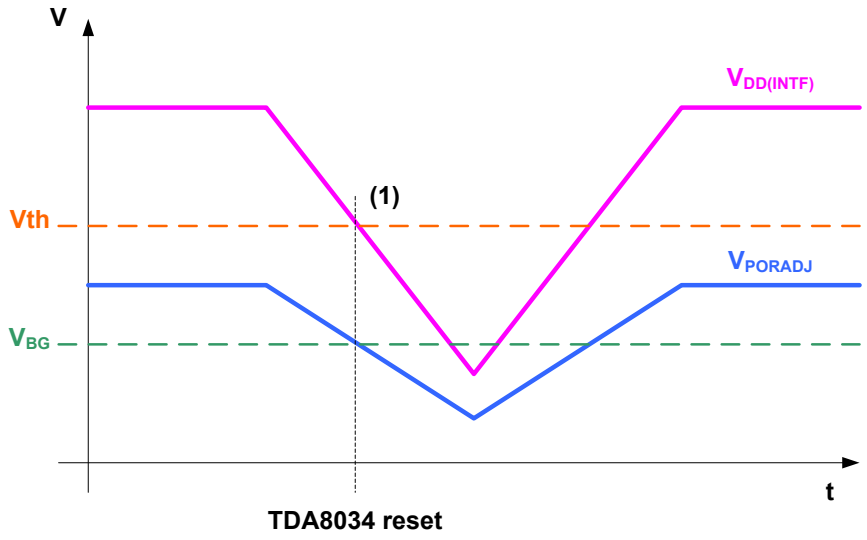
Fig 5. $V_{DD(INTF)}$ supervision – Resistor bridge

In this case $V_{PORADJ} = V_{DD(INTF)}.R2/(R1+R2)$ and $V_{DD(INTF)}$ is monitored indirectly: the TDA8034 enters the reset mode when $V_{DD(INTF)}.R2/(R1 + R2)$ falls below Vbg.

This corresponds to a “virtual” threshold on $V_{DD(INTF)}$ which value is obtained when

$Vbg = V_{DD(INTF)}.R2/(R1+R2)$ ➔ $V_{DD(INTF)} = Vbg.(1+R1/R2)$

This virtual threshold is the Vth corresponding to $V_{DD(INTF)}$. This is called virtual as $V_{DD(INTF)}$ is never compared to Vth. Only V_{PORADJ} is compared to Vbg. The following drawing shows this behavior:



(1) When $V_{DD(INTF)}$ falls below V_{th_VDDI}, V_{PORADJ} falls below Vbg then the drop-off is detected

Fig 6. $V_{DD(INTF)}$ supervision – Virtual $V_{DD(INTF)}$ threshold Vth

The resistor bridge is needed only in the case a specific threshold on $V_{DD(INTF)}$ must be chosen for the application, but in the general case, $V_{DD(INTF)}$ can be input directly on PORADJ.

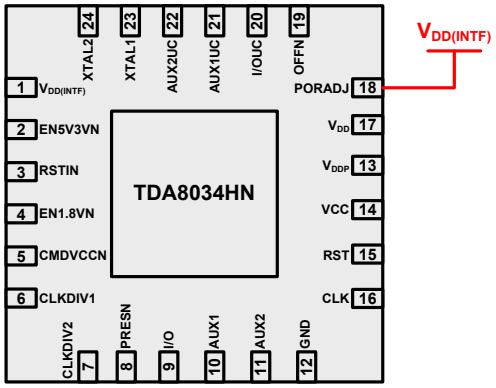


Fig 7. $V_{DD(INTF)}$ supervision – No resistor bridge

This is a particular case of the previous description with R1 = 0Ω and R2 = ∞.

Here Vth = Vbg.(1+R1/R2) = Vbg.

2.2.3 Summary

The following table gives the different threshold values for each supply input pin.

Table 2. Supply supervisor - Typical threshold values

	V_{DD}	V_{DDP} (VCC = 5V)	V_{DDP} (VCC < 5V)	$V_{DD(INTF)}$ (No PORADJ bridge)	$V_{DD(INTF)}$ (PORADJ bridge used)
Corresponding Typ. V_{th}	2.35V	4.45V	2.55V	1.22V	1.22 x (1+R1/R2)
Corresponding Typ. V_{hys}	100mV	100mV	100mV	60mV	0mV

2.3 Low consumption

The TDA8034 offers two low consumption modes: shutdown and deep shutdown.

2.3.1 Shutdown mode

The shutdown mode is the default mode when the card is not active (CMDVCCN HIGH). The typical consumption in this mode is around 30µA.

Due to this mode, the activation timing changes a bit compared to the TDA8024. Refer to the “Activation” chapter to see the exact difference induced by this mode.

2.4 Deep shutdown mode

The deep shutdown mode is a very low consumption mode (10µA typically). This mode can be entered when the card is not active (CMDVCCN HIGH) by tying EN5V3VN and EN1V8N to the LOW state.

In this mode, the supervisors are turned off, but the presence detection is still available: the OFFN pin follows the status of the presence (PRESN inverted).

This mode can for example be used when no card is present. In this case, the TDA8034 cannot be used and the host can only wait for a card insertion before activating it. The following figure gives a usage example with 5V smart cards:

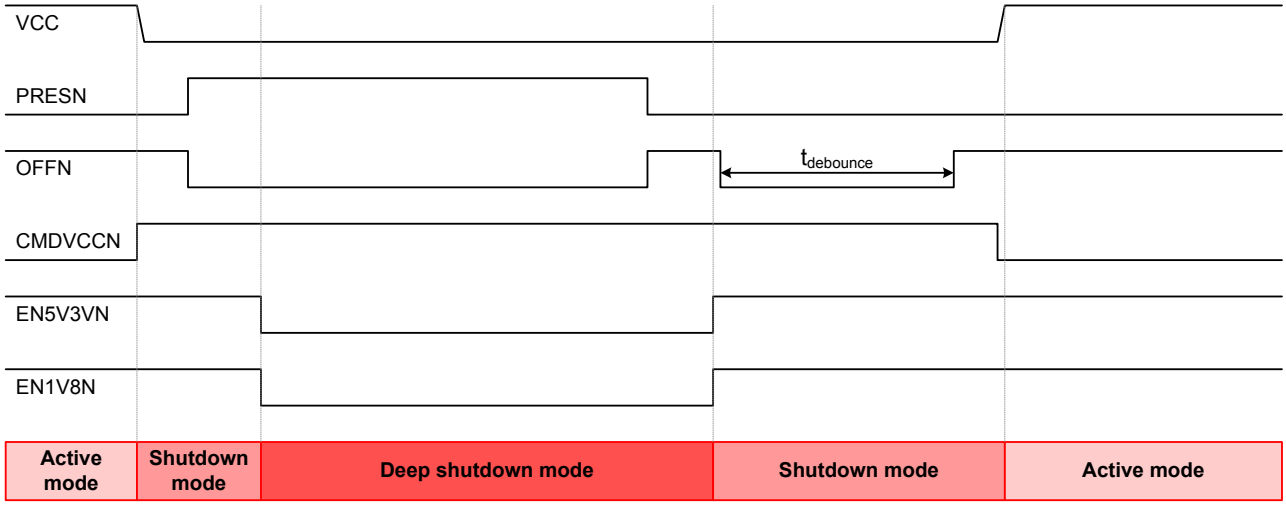


Fig 8. Deep shutdown mode example

3. Input Clock

There are two possibilities to provide the clock to the TDA8034: using a crystal or applying an external clock provided by the microcontroller.

Any value of crystal can be used from 2MHz to 26MHz.

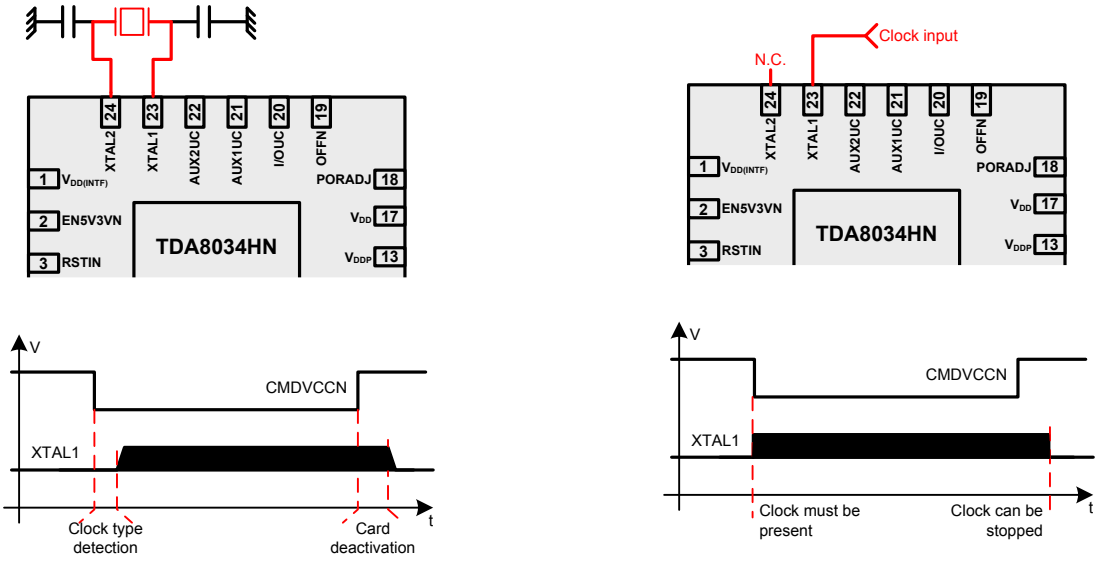
The XTAL pins are referenced to V_{DD}. In the case of a crystal, the high level of the clock is equal to V_{DD}, and in case of an input clock, it must be referenced to V_{DD}.

The type of clock is detected automatically by the TDA8034. So there is no specific configuration.

The clock is not mandatory outside of the card session. This means that if a crystal is used, it will only toggle when CMDVCCN is low. There is no activity on XTAL1 when CMDVCCN is HIGH.

If an external clock signal is applied to XTAL1, it is mandatory to start it before CMDVCCN is LOW, but it is not necessary to apply it when the card must not be activated.

The following figures represent the two configurations and the way they are used.



a. XTAL

b. External clock

Fig 9. TDA8034 clock

When the clock comes from the host (input on XTAL1), the clock generated on the smart card side is inverted:

When a falling edge occurs on XTAL1, the corresponding edge on CLK is rising, and when the clock rises on XTAL1, CLK falls.

This cannot be an issue for the communication with the smart card as the process is asynchronous.

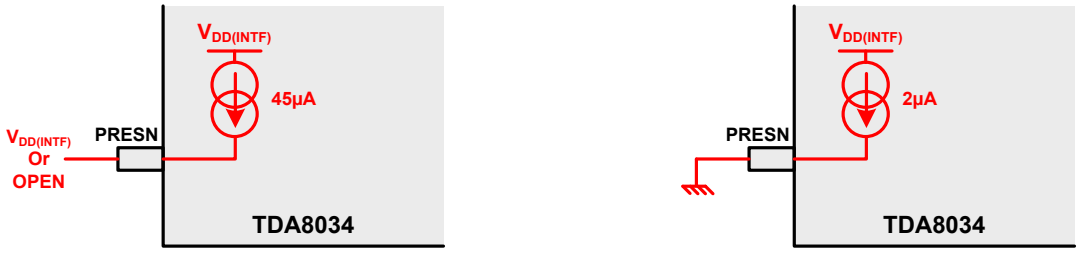
4. Card connector

4.1 Presence pin

One input pin is available to detect the card presence: PRESN.

This pin is active LOW and embeds an internal current to $V_{DD(INTF)}$. Therefore, when the pin is left open, the card is assumed to be absent.

The current sourced depends on the state of the pin. When the pin is HIGH, the current is typ. 45µA, and when the pin is LOW, the current is typ. 2µA.



a. PRESN HIGH → 45µA

b. PRESN LOW → 2µA

Fig 10. Internal PRESN source current

The way to connect the switch of a smart card connector depends on its gender (normally open or normally closed).

4.1.1 Normally open presence switch

The TDA8034 is planned to be used with this type of card connector without any external component. The connection of this card connector presence switch is shown in the next figure:

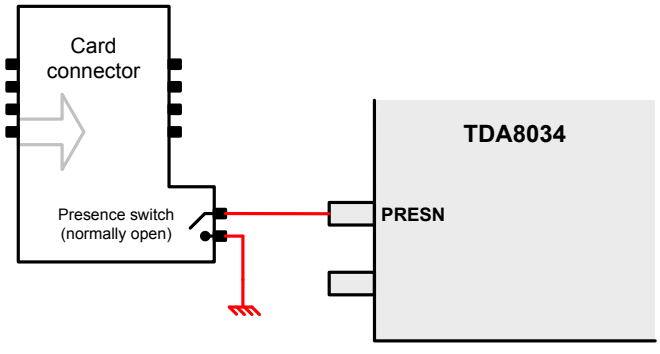


Fig 11. Normally open card connector connection

When the card is not inserted, the switch is open, and the internal current source drives the pin at HIGH level. The PRESN pin is not active and the card is assumed to be absent.

When the card is inserted, the switch is closed and the PRESN pin is connected directly to the ground. The pin is active and the card is seen as present.

4.1.2 Normally closed presence switch

To use this type of card connector, an external resistor is mandatory, and the schematics must be used as shown hereafter:

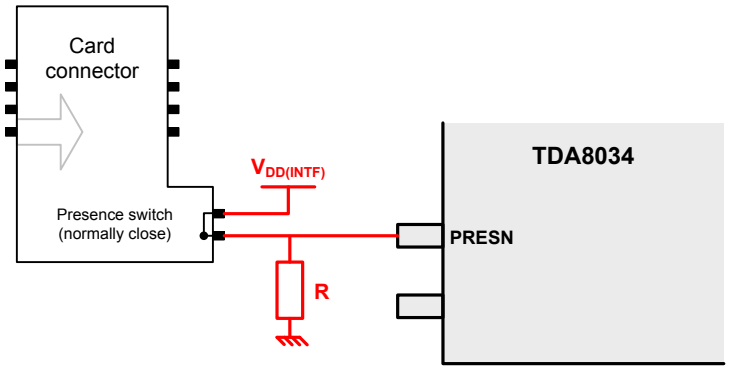


Fig 12. Normally closed card connector connection

When the card is not inserted, the switch is closed and PRESN is HIGH. The pin is not active so the card is seen as absent.

A current equal to $V_{DD(INTF)}/R$ will be consumed.

When the card is inserted, the switch will be open. Then the PRESN pin will have a typical 45µA current sourced into the resistor (the maximum value of this current I_{max}, is given to 60µA).

The resistor must be customized to have a voltage level on the PRESN pin lower than its minimum V_{IL} in order to have a LOW level on the PRESN pin.

The minimum V_{IL} (V_{IL_min}) of the PRESN pin is equal to $0.3.V_{DD(INTF)}$.

R must be customized to achieve this equation:

$R_{max}.I_{max} < V_{IL\_min}$

R_{max} = 1.2 x R. It corresponds to the maximum value of a 20% resistor.

For instance, with VDD(INTF) = 3.3V, we must have:

1.2 x R x 60.10-6 < 0.3 x 3.3

R < 13.750 kΩ. The higher standard resistor that can achieve this constraint is 13kΩ.

The following table gives the standard value to be used with these schematics, depending on the $V_{DD(INTF)}$ value.

Table 3. Pull down resistor wrt $V_{DD(INTF)}$

$V_{DD(INTF)}$	Standardized resistor value
$1.6V \leq V_{DD(INTF)} < 1.8V$	6.2kΩ
$1.8V \leq V_{DD(INTF)} < 2V$	7.5kΩ
$2V \leq V_{DD(INTF)} < 2.2V$	8.2kΩ
$2.2V \leq V_{DD(INTF)} < 2.4V$	9.1kΩ
$2.4V \leq V_{DD(INTF)} < 2.7V$	10kΩ
$2.7V \leq V_{DD(INTF)} < 2.9V$	11kΩ
$2.9V \leq V_{DD(INTF)} < 3.2V$	12kΩ
$3.2V \leq V_{DD(INTF)}$	**13kΩ**

4.1.3 Debouncing

With some card connectors, depending on the mechanical characteristics of the switch, bouncing may be seen on the PRESN pin when a card is inserted or extracted. This bouncing is managed by the TDA8034 which does not transfer exactly the PRESN state to the OFFN pin.

When the card is inserted, the TDA8034 waits for the PRESN pin to be stable for several milliseconds before assuming that the card is inserted. When the card is extracted, the chip acts as soon as the presence is not active. This behavior is summarized in Fig 13:

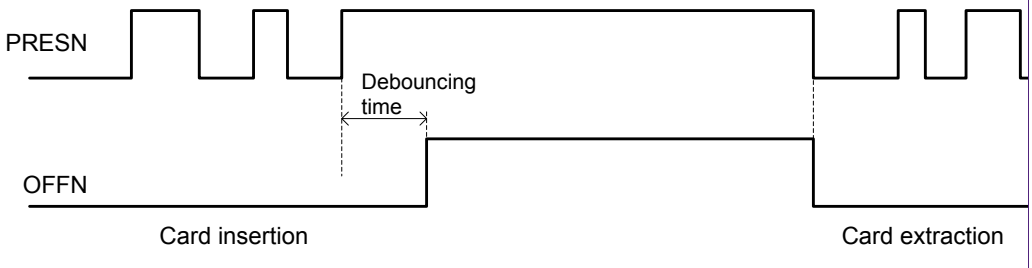


Fig 13. Debouncing feature

4.2 Schematics

To connect the smart card connector to the TDA, only two capacitors are mandatory as external components. The schematic reference is given in Fig 14.

The C1 capacitor must be placed near the TDA8034 and C2 must be connected close to the card connector.

The advised values for C1 and C2 are respectively 470nF and 220nF. These values are mandatory to have a ripple on VCC in the specified limits.

Pins C4 and C8 of the card connector (connected to pins AUX1 and AUX2) are optional. They can be left unconnected unless some specific operation using these pins is required.

It is not advised to leave pin VPP (C6) unconnected. It can be connected directly to VCC or GND in accordance with latest ISO 7816 standards. Connecting it to VCC allows it to be compliant with older cards which might not support VPP connected to the Ground.

For more flexibility, the design should include a 0 ohm serial resistor between VPP and VCC. Then the application can be easily adapted if needed.

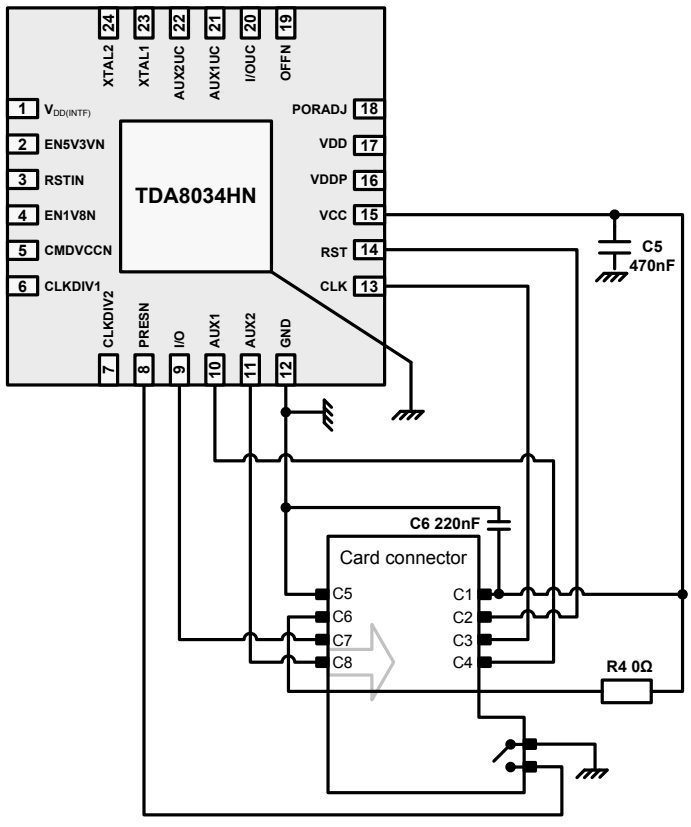


Fig 14. HVQFN24 Card connector design

5. Card configuration

The chip can be configured dynamically to operate with the connected card. Two parameters can be controlled: the voltage level and the frequency of the clock signal to the card.

5.1 Card voltage

The voltage level is configured with the following pins:

- EN_1.8VN
- EN_5V/3VN

These pins must be connected to an output of the host. This connection is recommended even for applications using a dedicated 5V card, in order to be easily compliant with the next generation cards.

The voltage level has to be configured before activation. The application MUST NOT change the value of these pins when the card is activated.

To change the voltage level of the card, the host must deactivate the card, change the voltage level value and then re-activate the card.

These pins are also used for the deep shutdown mode.

The following table gives the action of each combination of these inputs.

Table 4. Select voltage pin behavior

Command	EN5V3VN	EN1V8N
Deep Shutdown	0	0
VCC = 1,8V	1	0
VCC = 3V	0	1
VCC = 5V	1	1

5.2 Card clock

5.2.1 Frequency selection

Two signals are used to select the card clock:

- CLKDIV1
- CLKDIV2

These signals must be connected to the host and determine the division ratio of the input frequency in the clock which is sent to the card when activated.

The following table describes the frequency corresponding to CLKDIV1/2 values. f_{XTAL} is the frequency applied on XTAL1 (crystal or external source).

Table 5. TDA8034 - Clock division selection

CLKDIV1	CLKDIV2	CLK
0	0	$f_{XTAL}/8$
0	1	$f_{XTAL}/4$
1	1	$f_{XTAL}/2$
1	0	f_{XTAL}

5.2.2 Frequency switch

5.2.2.1 General behavior

CLKDIV1 and CLKDIV2 can be changed freely when the card is not active. The values will be adopted on activation.

When the card is active, the frequency applied to the card can be switched by changing CLKDIV1 and CLKDIV2 as shown in the following figure:

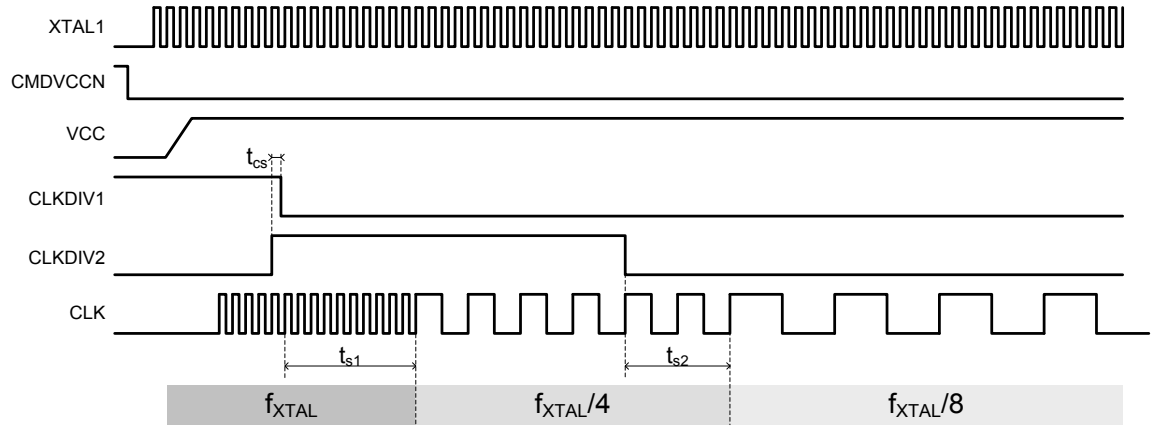


Fig 15. Clock switch during activation

The clock starts with the value specified at activation. Then the clock frequency switch occurs after a maximum of 10 XTAL1 periods after a change is seen on CLKDIV1/2 ($t_s < t_{smax}$ = 10 clock cycles).

5.2.2.2 Simultaneous change on CLKDIV1 and CLKDIV2

When both CLKDIV1 and CLKDIV2 have to be changed simultaneously, a maximum delay of 1 XTAL1 period (t_{cs}) is required between the two edges.

If this timing is not respected, an undesired frequency can be observed during the frequency switchover as shown in the next figure: a switch from f_{XTAL} to $f_{XTAL}/4$ is performed, but a frequency of $f_{XTAL}/2$ is seen during the switchover.

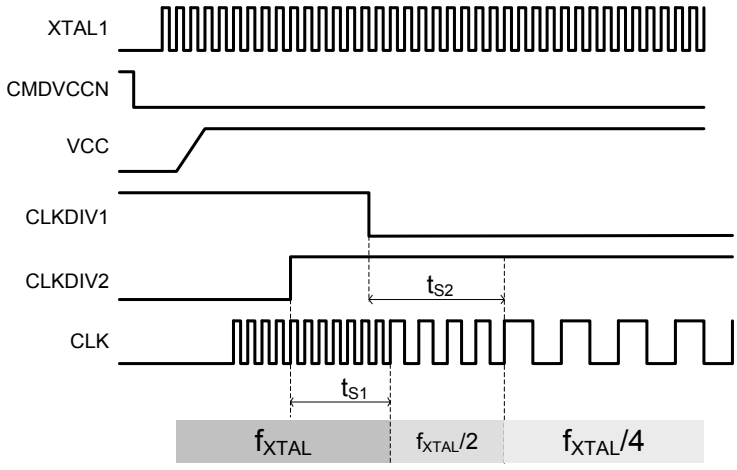


Fig 16. Unwanted frequency during the switch

6. Card Activation / Deactivation

6.1 Difference TDA8024 – TDA8034

6.1.1 Activation timing

The electrical interface between the host and the TDA is based on GPIOs and is exactly the same for TDA8034 as for TDA8024.

In the card management, the only difference between the TDA8024 and TDA8034 is the delay between CMDVCCN Low and VCC High.

This time is very low for the TDA8024 while it is equal to 3.47ms in the TDA8034 (see next chapter).

6.1.2 Software

When the TDA8034 is implemented in a design, the software already developed for the TDA8024 can be reused, with a little modification in one case:

If, for the TDA8024, the delay between VCC High and RST High had been set to a low value (below 3.5ms), this delay must be changed to a highest value, as described in the next chapter.

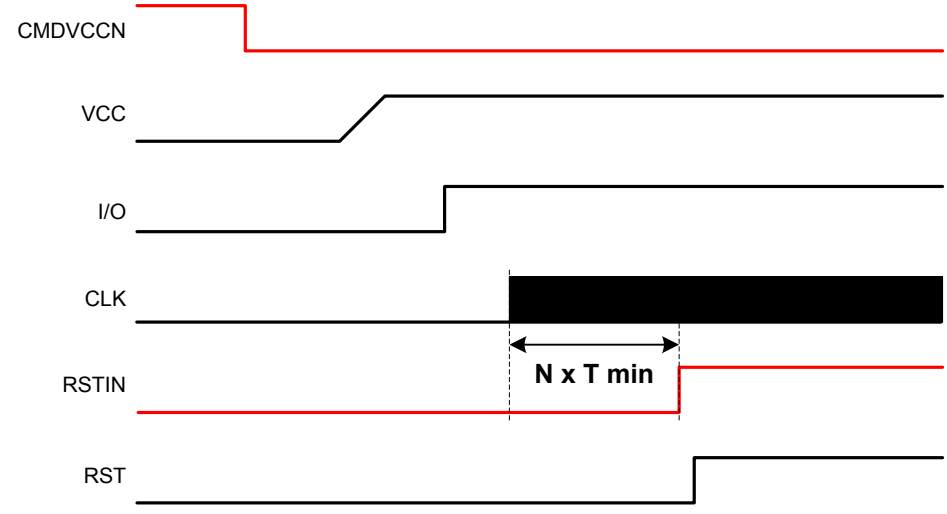
If the delay is greater than 3.5ms, then the same code can be reused without any change.

6.2 Activation

To activate the card, two signals are controlled by the host: CMDVCCN and RSTIN.

The first signal sets the card power supply, the second controls the reset pin of the card.

In the simplest mode, two actions are required from the host to activate the card: reset CMDVCCN and then set RSTIN. The activation sequence is shown in Fig 17.



(1) N = 400 for ISO, 40000 for NDS/EMV

Fig 17. Card activation sequence

The input clock must be OK for this sequence to occur. If the clock is supplied externally (no crystal), the clock must be present and stable before the falling edge of CMDVCCN.

The only constraint on the host is due to the standard specifications:

For the ISO 7816, the host must wait at least 400 clock cycles after the clock is active, before asserting RST.

In NDS and EMV specifications, the delay must be 40000 clock cycles

However in this mode, the host has no way of knowing when the clock starts. So it is not possible to count precisely the number of cycles.

To be sure that the right number of clock cycles are respected, the host must know the timing between CMDVCCN fall, VCC rise and CLK start.

These timings are given in the following figure

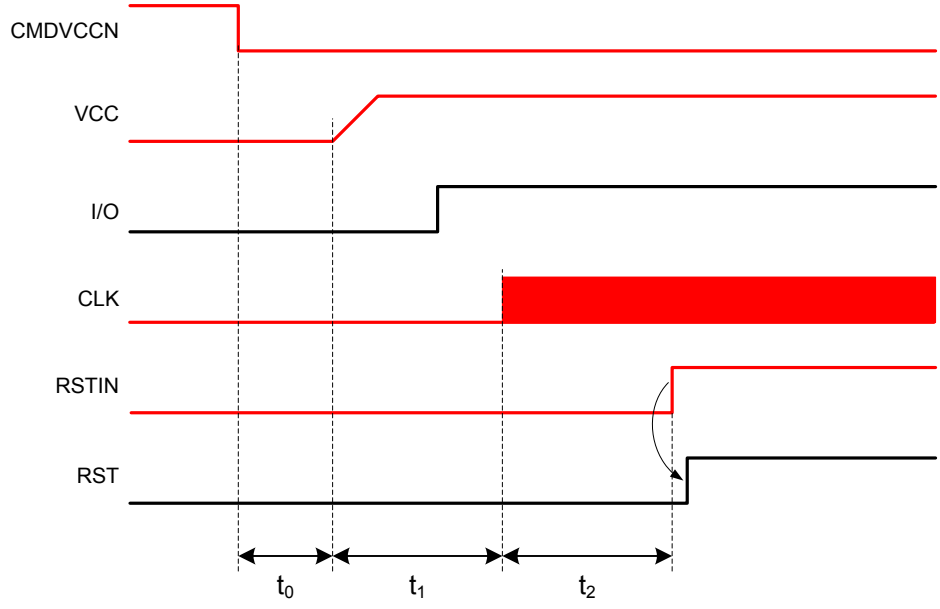


Fig 18. Activation timing

During t_0, the TDA8034 checks for the XTAL1 pin to detect if a crystal is present or if the clock is supplied from the microcontroller, and then waits for the crystal to start.

This time is fixed, even if there is no crystal, and its maximum value is 3.2ms.

t_1 is the time between the beginning of the activation and the start of the clock on the smart card side. This time depends on the internal oscillator frequency and lasts at maximum 272µs.

The host must then assume that the smart card clock doesn't start before 3.47 ms after CMDVCCN has been set to LOW.

To set RSTIN, the host must wait at least 400 (ISO) or 40000 (NDS/EMV) clock cycles after the start of CLK. Therefore t_2 depends on the input clock and on the division applied to supply the clock to the smart card and must be managed by the host.

The time between CMDVCCN low and RSTIN high, must respect this condition:

$\mathbf{t_0+t_1+t_2 > 3.47ms + 400/f_{CLK}}$ or

$\mathbf{t_0+t_1+t_2 > 3.47ms + 40000/f_{CLK}}$

6.3 Deactivation

The deactivation is managed entirely by the TDA8034 sequencer. Deactivation occurs when one of the following events happens:

- Rising edge of CMDVCCN (normal host deactivation)
- A fault is detected:
  - Card removal
  - Overheating
  - Short-circuit or high current on VCC
  - $V_{DD(INTF)}$, VDD or VDDP drop

The deactivation sequence is automatic and fully compliant with the standard. For more details on the activation or deactivation sequence and their timings, refer to the TDA8034 data sheet and ISO 7816-3 standard.

7. Card operation

7.1 I/O, Aux1, Aux2

The TDA8034 acts as a simple transceiver incorporating a voltage level shifting adaptation for these signals, once the card is activated.

As there is no other conversion, the host must manage entirely the protocol defined by ISO 7816 (Baudrate, timing, frame…).

The TDA8034 only limits the current on the pins. There is a limitation of 15mA in both directions.

- I/O is linked to I/OUC,
- AUX1 to AUX1UC, and
- AUX2 to AUX2UC.

I/OUC must be connected directly to an I/O of the host. AUX1UC and AUX2UC can as well be connected to the host or left open if C4 and C8 pin are not used on the card.

7.2 Warm reset

The host can operate a warm reset with the TDA8034: as the RST card pin is the copy of the RSTIN pin, the host just needs to apply a falling edge on RSTIN, followed by a rising edge, and the card shall send its ATR again.

8. Fault detection

The TDA8034 supervises several parameters and warns the host when a problem occurs. The OFFN pin is used to manage this communication with the host. The table below gives the state of the chip in accordance with CMDVCCN and OFFN values.

Table 6. Chip state regarding CMDVCCN and OFFN

CMDVCCN	OFFN	State	Comment
HIGH	HIGH	Card is present and not active	
HIGH	LOW	Card is absent	
LOW	HIGH	Card is active and no fault has been detected	This is the state of all card sessions
LOW	LOW	A fault has been detected (card has been deactivated)	The cause of the deactivation is not yet known.
Rising edge	Stays LOW	The fault detected was the card removal	Setting CMDVCCN allows checking if the deactivation is due to card removal.
Rising edge	Rising edge	The fault detected was not a card removal (card is still present)	In this case the OFFN pin will stay low after CMDVCCN is high. If OFFN follows CMDVCCN, the fault is due to a supply voltage drop, a VCC over-current detection or overheating.

9. Electrical design recommendations

9.1 Decoupling

To ensure proper behavior of the TDA8034, some external components have to be used. All supply pins must be protected against noise.

VCC pin (card contact) needs to be connected to two capacitors: 470nF plus 220nF as described in chapter 4: one near the TDA8034 chip and one near the card connector. These capacitors type must be low ESR.

$V_{DD(INTF)}$and VDD must be protected by 100nF.

VDDP must be protected by two capacitors: one 100 nF to protect particularly against high frequency noise and one 10 µF to absorb slower variations.

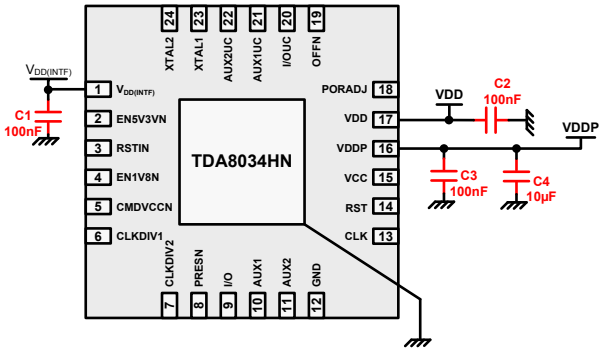


Fig 19. Power supply decoupling strategy

9.2 Layout

For noise reduction optimization, the layout of the design must adhere to the following guidelines.

9.2.1 Decoupling capacitors

Capacitors are mandatory to protect the supply pins as well as the VCC pin (TDA8034 pin and Card connector pin).

Place decoupling capacitors as close as possible to the pin that they protect.

This means that the capacitor must be physically soldered near the chip or the card connector pin, but also with a short and good connection (low resistance) between the protected pin and its capacitor.

The connection between the capacitor pin and the ground must be short low resistive as well.

9.2.2 Clock wires

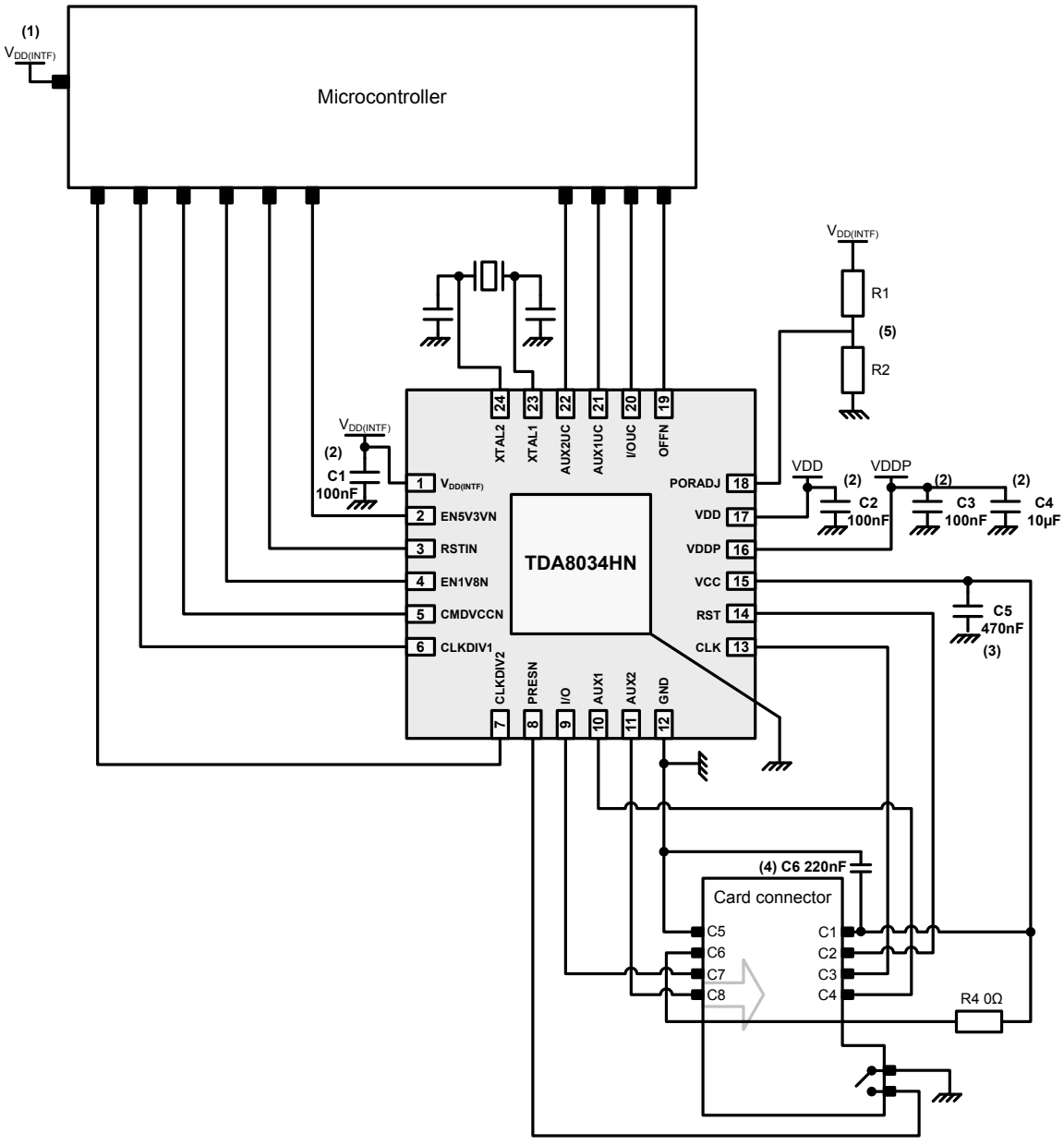
Clock (card) or oscillator signals can cause crosstalk to other signals. It is advised to isolate these signals: make the connections as short as possible and keep them far from other signals.

The best is to shield these signals with ground when possible.

9.2.3 Card ground connection

There is no ground pin dedicated to the smart card connector on the TDA8034. Therefore the C5 pin of the card connector must be connected to the main ground layer with a short and low resistive connection.

9.3 Summary



(1) Microcontroller and TDA8034 must use the same $V_{DD(INTF)}$ supply

(2) Place these capacitor close to the pin they protect ($V_{DD(INTF)}$, VDD, VDDP)

(3) Low ESR 470nF capacitor. Must be placed close to the chip's VCC pin

(4) Low ESR 220nF capacitor. Must be placed close to the C1 contact of the card connector

(5) Optional resistor bridge. If this bridge is not required, connect PORAdj pin to $V_{DD(INTF)}$

Fig 20. Reference design with TDA8034HN

10. Hardware Update

10.1 Change from version C1 to C2

End of 2015, EMVCo introduced a new Analog test suite, following the EMVCo 4.3 specifications. This new test suite now implements a Vil test on I/O line, corresponding to the EMVCo 4.3 specifications: The I/O Vil must be set to 0.2 x VCC at maximum.

For TDA8034/C1, the margin with this new limit on VIL is very narrow depending on production batches (close to 1V for Vcc=5V) and a hardware upgrade has been done to avoid any issue during EMVCo certification; new part numbers have been created.

The Hardware change modifies the Vil of TDA8034. It was set to 0.8V max in TDA8034/C1 version, and is now set to 1V max in TDA8034/C2 version.

The TDA8034/C2 version can be used as a direct replacement of TDA8034/C1 without any other change on the application, either SW or HW.

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Date of release: 6 June 2016
Document identifier: AN10792