AN10771

Using the LPC24xx EMC peripheral to drive SDRAM

Rev. 01 — 1 December 2008

Application note

Document information

Info	Content
Keywords	LPC24xx, External Memory Controller(EMC), SDRAM
Abstract	This application note describes how to use LPC24xx External Memory Controller (EMC) peripheral to drive external SDRAM.

founded by Philips

Revision history

Rev	Date	Description
01	20081201	Initial version

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1. Introduction

The LPC2400 External Memory Controller (EMC) is an ARM PrimeCell™ MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM and Flash, as well as dynamic memories such as Single Data Rate SDRAM. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

Following is a block diagram of the EMC.

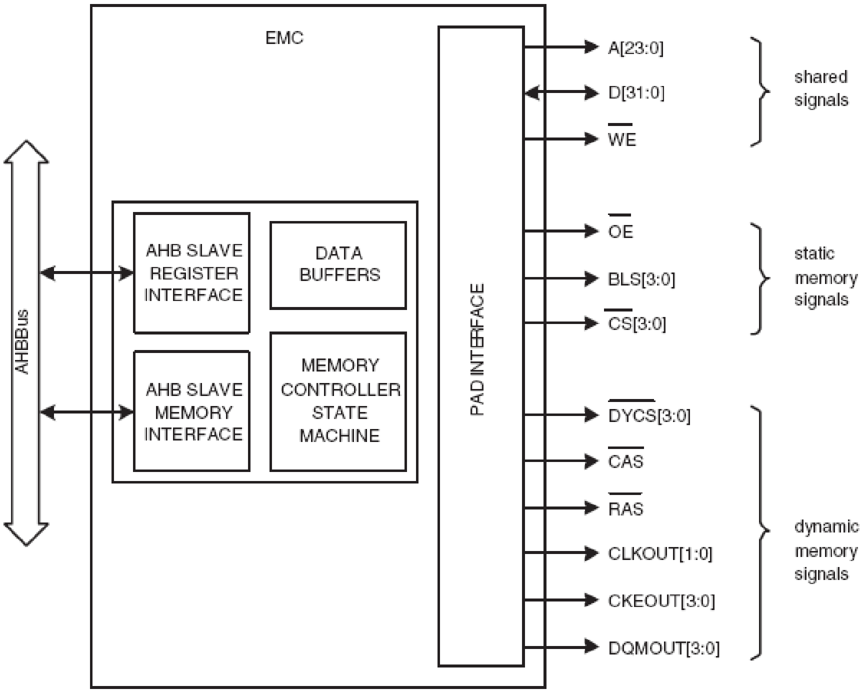

Fig 1. EMC block diagram

To control a SDRAM memory, the EMC provides the following possible features:

- 16 bit and 32 bit wide chip select SDRAM memory support.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control CKE and CLKOUT to SDRAM.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2 kbit, 4 kbit, and 8 kbit row address synchronous memory parts.

Eight independently-configurable memory chip selects are supported:

- Pins CSn3 to CSn0 are used to select static memory devices.
- Pins DYCSn3 to DYCSn0 are used to select dynamic memory devices.

The following table shows the address ranges of the chip selects.

Table 1. Memory bank selection

Chip select pin	Address range	Memory type	Size of range
DYCS0	0xA000 0000 - 0xAFFF FFFF	Dynamic	256 MB
DYCS1	0xB000 0000 - 0xBFFF FFFF	Dynamic	256 MB
DYCS2	0xC000 0000 - 0xCFFF FFFF	Dynamic	256 MB
DYCS3	0xD000 0000 - 0xDFFF FFFF	Dynamic	256 MB

The memory controller comprises a static memory controller and a dynamic memory controller. For the EMC register definition, please refer to Table 5–58 of LPC24xx user manual.

2. Hardware connection

Table 2 gives the correspondence between the SDRAM memory pins and the EMC pins and also shows the GPIO configuration for each EMC pin.

In the case of an 8-bit SDRAM memory, the data bus is 8-bit wide and D8-D15 should not be connected to the EMC.

Table 2. SDRAM(K4S561632H) signal to EMC pin correspondence

Memory signals	EMC signals	Pin / Port assignment	Signal description
SCLK	CLKOUT0	P2[18]	SDRAM System Clock
SCKE	CKEOUT0	P2[24]	Clock Enable
A0 ~ A12	A0 ~ A12	P4[0] ~ P4[12]	Address
BA0 ~ BA1	A13 ~ A14	P4[13] ~ P4[14]	Bank Select Address
DQ0 ~ DQ15	D0 ~ D15	P3[0] ~ P3[15]	Data Input/Output
nSCS	nDYCS0	P2[20]	Chip Select
nRAS	nRAS	P2[17]	Row Address Strobe
nCAS	nCAS	P2[16]	Column Address Strobe
nWE	nWE	P4[25]	Write Enable
L(U)DQM	DQMOUT0/1	P2[28]/ P2[29]	Data Input/Output Mask

Figure 2 shows a typical connection between an LPC24xx microcontroller and the Samsung K4S561632H SDRAM memory.

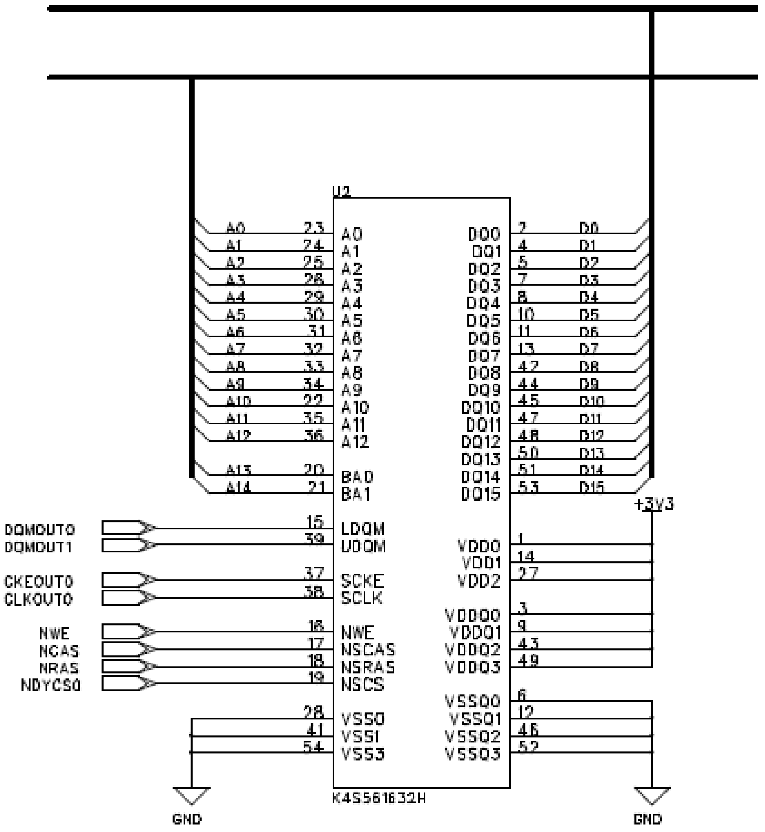

Fig 2. 16-bit SDRAM: K4S561632H connection to LPC24xx

3. SDRAM operation and timing

3.1 SDRAM introduction

SDRAM stands for **Synchronous Dynamic Random Access Memory**. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. A wide range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

The following is SDRAM functional block diagram.

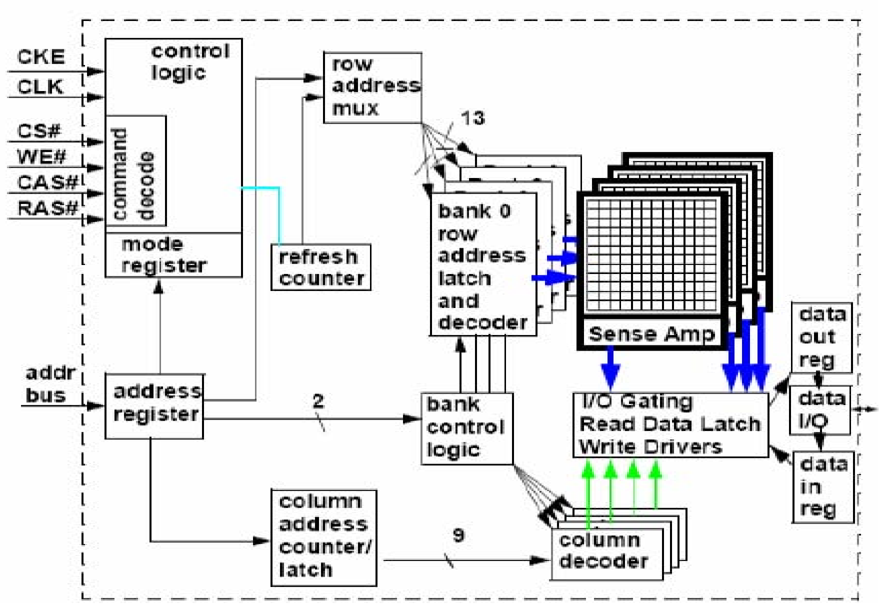

Fig 3. SDRAM Functional Block Diagram

3.2 Commands

The following Truth Table provides a quick reference of several available commands. This is followed by a written description of each command. For each command the LPC24xx SDRAM controller will generate required logic signaling for the connected SDARAM.

Table 3. Truth Table – Commands and DQM Operation

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQs
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X
NO OPERATION (NOP)	L	H	H	H	X	X	X
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/row	X
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H8	Bank/col	X
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H8	Bank/col	Valid
BURST TERMINATE	L	H	H	L	X	X	Active
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X

3.3 Mode Register

The mode register is used to define the specific operation mode of the SDRAM. This definition includes the selection of burst length, burst type, CAS latency, operating mode, and write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power. At SDRAM initialization, mode register should be set.

The following simple figure describes the mode register.

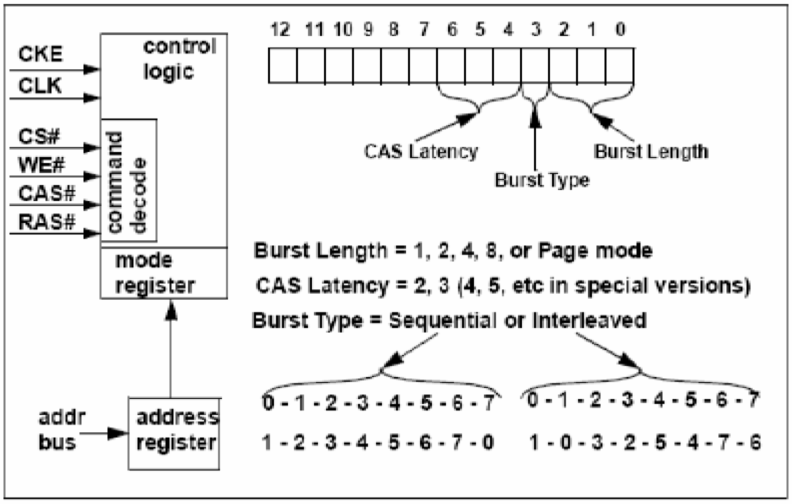

Fig 4. Mode register description

CAS Latency, CL, is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

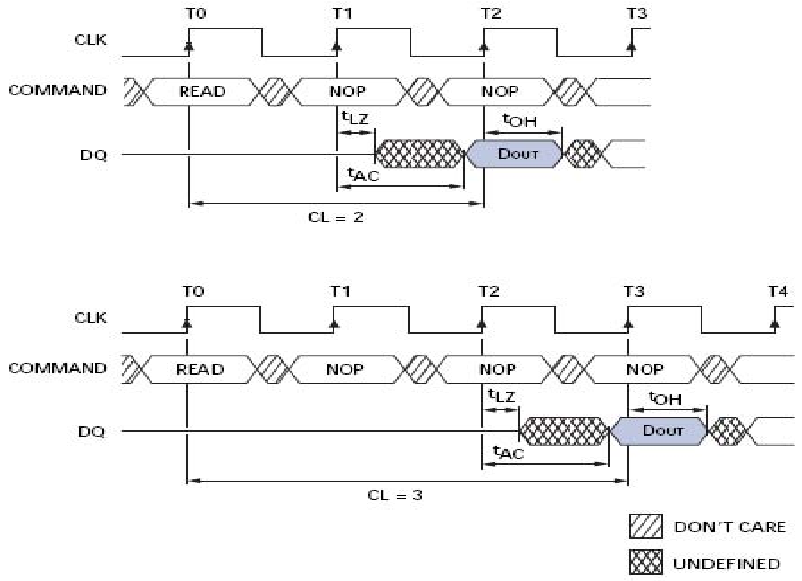

Fig 5. CAS Latency

3.4 SDRAM initialization

The SDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

The recommended power-up sequence for SDRAM is as follows:

1. Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
   - Apply VDD before or at the same time as VDDQ.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
6. Issue a extended mode register set command to define DS or PASR operating type of the device after normal MRS.

More detail about initialization process will be described in the demo introduction.

3.5 SDRAM timing

In the case where an external SDRAM memory is used, the user has to compute and set the following parameters depending on the information in the memory datasheet.

Table 4. Timing parameters

	Description	K4S561632(75)	Demo setting
CL/ CLK	CAS latency/SDRAM system clock	2(CLK max100MHZ) or 3(CLK max133MHZ)	2/48MHz (72Mhz max supported by LPC24xx)
tRP	precharge command period	20ns(min)	20ns
tRAS	active to precharge command period	45ns(min),100us(max)	45ns
tSREX	self-refresh exit time	___	tXSR
tAPR	last-data-out to active command time	___	1 CLK
tDAL	data-in to active command time	2 CLK + tRP	2 CLK + tRP
tWR	write recovery time	___	2 CLK
tRC	write recovery time	65ns(min)	66 ns
tRFC	auto-refresh period	___	66 ns
tXSR	exit self-refresh to active command time	___	1 CLK
tRRD	active bank A to active bank B latency	15ns(min)	15ns
tMRD	load mode register to active command time	___	2 CLK
SDRAM_REFRESH	Refresh period	64ms(max)/8192	7.813us

These parameters give the EMC the flexibility to access a wide variety of external SDRAM.

4. SDRAM Demo

4.1 Hardware environment

IAR_LPC2468 is the test board for this AN. The code can be downloaded to on chip flash via ISP using Flash Magic software or via JTAG using ULink/JLink.

4.2 Software environment

Kei MDK 3.22a is the IDE and toolchain for the software.

4.3 Demo introduction

With the demo, we try to show how to use LPC24xx External Memory Controller (EMC) peripheral to drive external SDRAM. In this demo, LPC24xx will use EMC peripheral to drive one external SDRAM(K4S561632H).

For driving the SDRAM, the EMC_init() function is defined to initialize EMC peripheral which includes port configuration and SDRAM_Test( ) function is defined for user to write and read SDRAM for test SDRAM.

4.4 EMC initialize steps with external SDRAM

Using EMC_init() to initialize EMC.

Step 1: configure EMC Pin function and Pin mode.

```
 PINSEL5&=0xF0FCFCC0;
 PINSEL5|=0x05010115;
 PINMODE5&=0xF0FCFCC0;
 PINMODE5|=0x0A02022A;
//p2.29(DQMOUT1),28(DQMOUT0),24(CKEOUT0),20(DYCS0),18(CLKOUT0)
//17(RAS),16(CAS)
 // mode=10 (Pin has neither pull-up nor pull-down resistor enabled.)

 PINSEL6  =  0x55555555;
 PINMODE6 =  0xAAAAAAAA;
 //p3.0-15=D0-15,mode=10

 PINSEL8 &= 0xC0000000;
 PINSEL8 |= 0x15555555;
 PINMODE8&= 0xC0000000;
 PINMODE8|= 0x2AAAAAAA;  //p4.0-4.14=A0-14,mode=10
```

Step 2: enable EMC and set EMC parameters.

```
PCONP|=0x800;      //enable EMC power
 EMC_CTRL=1;        // enable EMC

 EMC_DYN_RD_CFG=1;//Configures the dynamic memory read strategy(Command delayed strategy)
 EMC_DYN_RASCAS0|=0x200;EMC_DYN_RASCAS0&=0xFFFFFEFF;//CAS latency=2
 EMC_DYN_RASCAS0|=0x3;    // RAS latency(active to read/write delay)=3
 EMC_DYN_RP= P2C(SDRAM_TRP);
 EMC_DYN_RAS = P2C(SDRAM_TRAS);
 EMC_DYN_SREX = SDRAM_TXSR;
 EMC_DYN_APR = SDRAM_TAPR;
 EMC_DYN_DAL =SDRAM_TDAL ;
 EMC_DYN_WR = SDRAM_TWR;
```

```
  EMC_DYN_RC = P2C(SDRAM_TRC);
  EMC_DYN_RFC = P2C(SDRAM_TRFC);
  EMC_DYN_XSR = SDRAM_TXSR;
  EMC_DYN_RRD = P2C(SDRAM_TRRD);
  EMC_DYN_MRD = SDRAM_TMRD;
  EMC_DYN_CFG0 = 0x0000680;
   // 16 bit external bus, 256 MB (16Mx16), 4 banks, row length = 13, column length = 9
```

NOTE: Before all EMC timing parameters are configured, their unit should be in ‘CCLK’. The P2C macro is defined to transfer timing parameters from ‘ns’ to ‘CCLK’.

```
if SYS_FREQ == (48)
#define EMC_PERIOD          20.8  // 48MHz
#endif
#define P2C(Period)     (((Period<EMC_PERIOD)?0:(unsigned
int)((float)Period/EMC_PERIOD))+1)
```

Step 3: perform SDRAM initialization.

```
  EMC_DYN_CTRL = 0x0183;   // NOP
  //Issue SDRAM NOP (no operation) command ; CLKOUT runs continuously; All clock
//enables are driven HIGH continuously


  for(i = 200*30; i;i--);
  EMC_DYN_CTRL|=0x100; EMC_DYN_CTRL&=0xFFFFFF7F;
// Issue SDRAM PALL (precharge all) command.
  EMC_DYN_RFSH = 1;  //Indicates 1X16 CCLKs between SDRAM refresh cycles.
  for(i= 128; i; --i); // > 128 clk
  EMC_DYN_RFSH = P2C(SDRAM_REFRESH) >> 4;
 // Indicates SDRAM_REFRESH time between SDRAM refresh cycles.


  EMC_DYN_CTRL|=0x80; EMC_DYN_CTRL&=0xFFFFFEFF;
//Issue SDRAM MODE command.
  wtemp = *((volatile unsigned short *)(SDRAM_CS0_BASE | 0x00023000));
 /* 8 burst, 2 CAS latency */


  EMC_DYN_CTRL = 0x0000;  //Issue SDRAM norm command ;
//CLKOUT stop; All clock enables low


 EMC_DYN_CFG0|=0x80000; //Buffer enabled for accesses to DCS0 chip
```

4.5 SDRAM test

Using the SDRAM_Test() function to write SDRAM and read back from SDRAM. If the data read from the SDRAM is the same as the data written to SDRAM, the function will return ‘TRUE’, else it will return ‘FALSE’:

```
unsigned int  SDRAM_Test (void)
{
  unsigned int i;
  // 32 bits access
  for (i = 0; i < 0x2000000; i+=sizeof(unsigned int))
  {
    *(unsigned int *)((unsigned int )&SDRAM_BASE_ADDR+i) = i;
  }
  for (i = 0; i < 0x2000000; i+=sizeof(unsigned int ))
  {
    if (*(unsigned int *)((unsigned int )&SDRAM_BASE_ADDR+i) != i)
    {
      return(FALSE);
    }
  }

  // 16 bits access
  for (i = 0; i < 0x10000; i+=sizeof(unsigned short))
  {
    *(unsigned short*)((unsigned int)&SDRAM_BASE_ADDR+i) = i;
  }
  for (i = 0; i < 0x10000; i+=sizeof(unsigned short))
  {
    if (*(unsigned short*)((unsigned int)&SDRAM_BASE_ADDR+i) != i)
    {
      return(FALSE);
    }
  }

  // 8 bits access
  for ( i = 0; i < 0x100; i+=sizeof(unsigned char))
  {
    *(unsigned char*)((unsigned int)&SDRAM_BASE_ADDR+i) = i;
  }
  for (i = 0; i < 0x100; i+=sizeof(unsigned char))
  {
    if (*(unsigned char*)((unsigned int)&SDRAM_BASE_ADDR+i) != i)
    {
      return(FALSE);
    }
  }
  return(TRUE);
}
```

5. Reference

[1] UM10237, LPC24xx User manual, Rev 01

[2] K4S56xx32h datasheet, Rev 1.0, Samsung electronics

[3] Micron 256SDRAM_1.fm, Rev. L10/07 EN

[4] ’SDRAM Device Operation’, Samsung electronics.

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Date of release: 1 December 2008
Document identifier: AN10771_1