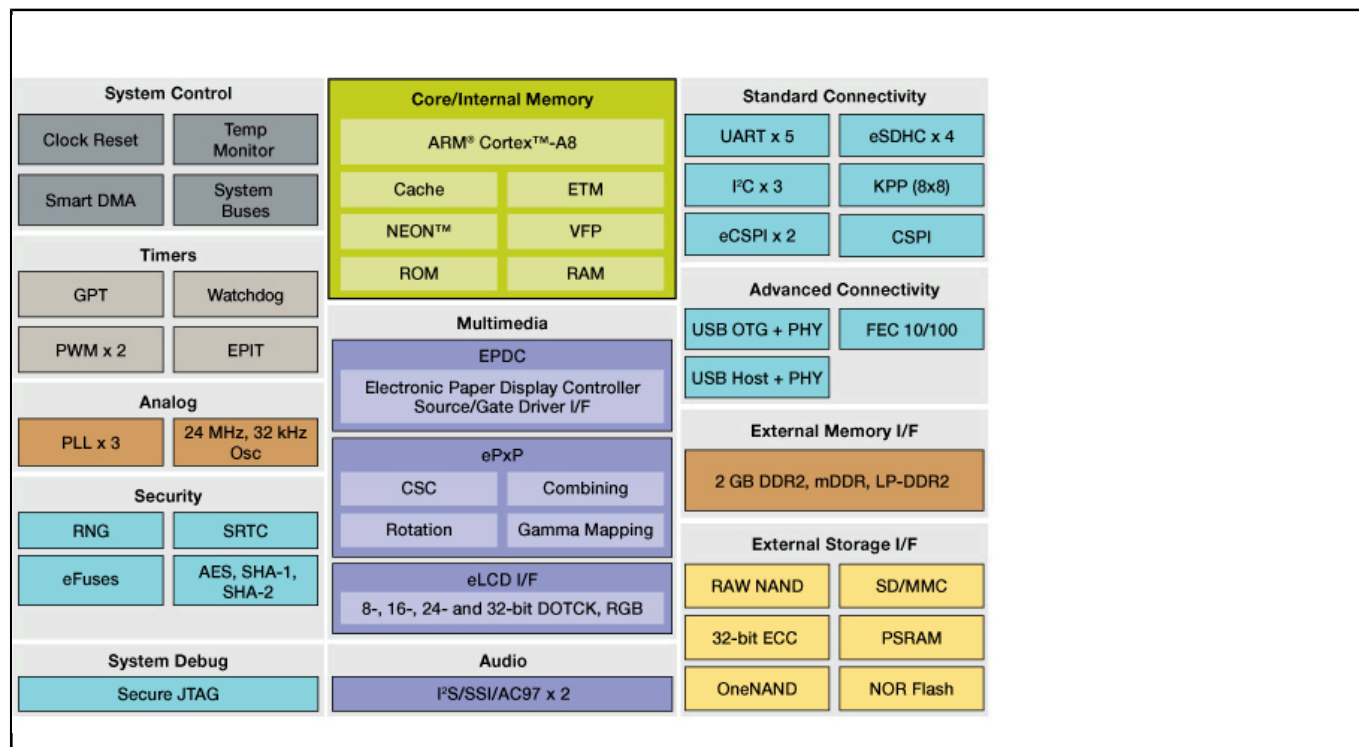# Multimedia Applications Processors - Low Power Optimization, Integrated Electronic Paper Display (EPD), Arm® Cortex®-A8 Core

i.MX507

Last Updated: Mar 4, 2025

Building on the market-leading i.MX508 applications processor for eReaders, the i.MX507 processor is the latest addition to Our Arm® Cortex®-A8 product portfolio. The i.MX507 combines a Cortex A8 and an integrated hardware Electronic Paper Display (EPD) controller to drive next generation low power display applications including outdoor signage and kiosks. Together with the companion NXP® power management ICs (PMIC) MC34708 and MMPF0100, customers can drive their next generation EPD designs with the i.MX507 processor.

i.MX507 Multimedia Applications Processor Block Diagram Block Diagram

System Control

| Clock Reset | Temp Monitor |
| Smart DMA | System Buses |

Timers

| GPT | Watchdog |
| PWM x 2 | EPIT |

Analog

| PLL x 3 | 24 MHz, 32 kHz Osc |

Security

| RNG | SRTC |
| eFuses | AES, SHA-1, SHA-2 |

System Debug

| Secure JTAG |

Core/Internal Memory

ARM® Cortex™-A8

Cache	ETM
NEON™	VFP
ROM	RAM

Multimedia

EPDC
Electronic Paper Display Controller Source/Gate Driver I/F

ePxP

| CSC | Combining |
| Rotation | Gamma Mapping |

eLCD I/F
8-, 16-, 24- and 32-bit DOTCK, RGB

Audio

I²S/SSI/AC97 x 2

Standard Connectivity

UART x 5	eSDHC x 4
I²C x 3	KPP (8x8)
eCSPI x 2	CSPI

Advanced Connectivity

| USB OTG + PHY | FEC 10/100 |
| USB Host + PHY | |

External Memory I/F

2 GB DDR2, mDDR, LP-DDR2

External Storage I/F

RAW NAND	SD/MMC
32-bit ECC	PSRAM
OneNAND	NOR Flash

View additional information for Multimedia Applications Processors - Low Power Optimization, Integrated Electronic Paper Display (EPD), Arm® Cortex®-A8 Core.

Note: The information on this document is subject to change without notice.