



完全集成的**77Ghz RFCMOS**汽车雷达收发器

TEF82xx

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TEF82xx RFCMOS汽车雷达收发器是一款高性能单芯片、低功耗汽车FMCW雷达收发器，涵盖了从76 GHz到81GHz的整个汽车雷达频段。这款第二代可扩展收发器支持入门级NCAP传感器，直至自动驾驶L2+传感器及以后的版本，支持短程、中程和远程雷达应用，包括级联高分辨率成像雷达。这种完全集成的RFCMOS芯片包含3个发射器、4个接收器、ADC转换、相位旋转器和一个低相位噪声VCO。

TEF82xx是符合ASIL B级的ISO26262的设备，它针对快速线性调频进行了优化，并且与恩智浦S32R29x、S32R41x和S32R45x雷达微控制器和处理器完全兼容。

The diagram illustrates the internal architecture of the TEF82xx MMIC. It is organized into several functional blocks:

- RF Front-End:** Four input ports (represented by Y-symbols) are connected to Rx 1, Rx 2, Rx 3, and Rx 4.
- Baseband Processor:** Each Rx block is paired with an ADC (ADC 1 to ADC 4). These are connected to a central PDC (Programmable Data Converter) block.
- Transmit Path:** Three output ports are connected to Tx 1, Tx 2, and Tx 3. These are connected to a Phase Rotator and a Waveform Generator.
- Control and Interface:** The device includes a Serializer (supporting LVDS and CSI2), an Xtal Osc. (Crystal Oscillator), a Timing Engine, Functional Safety, and an SPI interface.
- Expansion Interface:** A dedicated block for future or optional features.

The diagram illustrates the system architecture for the TEF82xx MMIC and S32R MCU. It is divided into two main sections: the TEF82xx MMIC on the left and the S32R MCU on the right, both powered by their own Power Supply blocks.

TEF82xx MMIC Section:

- Inputs:** Four antenna inputs (Y) are connected to Rx 1, Rx 2, Rx 3, and Rx 4.
- Processing:** Each Rx channel is followed by an ADC (ADC 1 to ADC 4). The outputs of the ADCs feed into the PDC (Programmable Data Converter).
- Transmit Path:** Tx 1, Tx 2, and Tx 3 are connected to a Phase Rotator and a Waveform Generator.
- Interfaces:** The MMIC includes an Expansion Interface, a Serializer LVDS CSI2, an Xtal Osc., a Timing Engine, Functional Safety, and an SPI interface.
- Outputs:** LO-in and LO-out signals are provided at the bottom, and an Xtal (Crystal) is connected to the SPI interface.

S32R MCU Section:

- Inputs:** Receives Radar Data, RESET_N, Error Reset, ErrorN, ChirpStart, and MCU_Int from the MMIC.
- Processing:** Contains a Radar Processing Platform and Radar Algorithms Tracking.
- Memory & Connectivity:** Includes Emb Memory SRAM, Connectivity, and Safety blocks.
- Outputs:** Sends SPI, QPS Tx 1, QPS Tx 2, QPS Tx 3, and Clock signals back to the MMIC.
- External Interfaces:** Connects to an Ethernet TJA1101 and a CAN TJA1462A via the Car Secure Network.
- Other Features:** Includes FlexRay, Ethernet, CAN FD, and Support blocks.

System Integration:

- The MMIC and MCU are connected via a series of bidirectional and unidirectional signals: Radar Data, RESET_N, Error Reset, ErrorN, ChirpStart, MCU_Int, SPI, QPS Tx 1, QPS Tx 2, QPS Tx 3, and Clock.
- The entire system is connected to a Car IVN (In-Vehicle Network) through the Ethernet and CAN interfaces.

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Note: The information on this document is subject to change without notice.

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