24-bit General Embedded DSP

DSP56321

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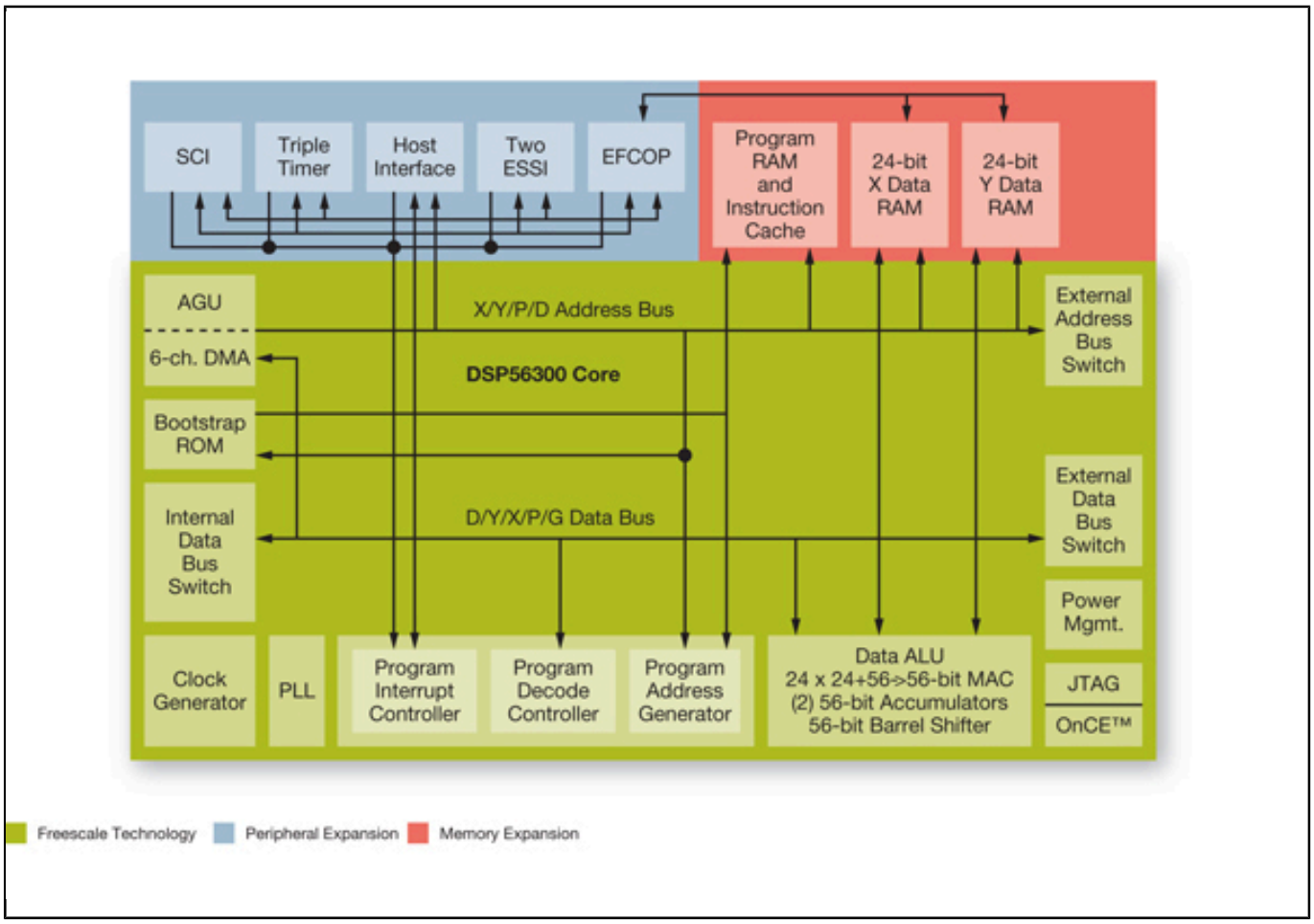
The DSP56321, a member of the DSP56300 family of programmable DSPs, supports network applications with general filtering operations. The on-chip enhanced filter coprocessor (EFCOP) executes filter algorithms in parallel with core operations to provide enhanced signal quality without affecting channel throughput or total number of channels supported, resulting in increased overall performance. Like the other family members, the DSP56321 uses a high-performance, single clock cycle per instruction engine, a barrel shifter, 24-bit addressing, instruction cache, and direct memory access (DMA) controller. The DSP56321 offers 275 million multiply accumulates per second (MMACS) performance (550 MMACS using the EFCOP in filtering applications) using an internal 275 MHz clock, a 1.6-volt core and independent 3.3-volt input/output (I/O).

DSP56321 Block Diagram Block Diagram



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Note: The information on this document is subject to change without notice.